IM8G08D4GBB
8Gbit DDR4 SDRAM
16 BANKS X 64Mbit X 8

Ordering Speed Code	-075	-062
	DDR4-2666	DDR4-3200
Clock Cycle Time (t_{CK10}, CWL=9)	1.5 ns	-
Clock Cycle Time (t_{CK11}, CWL=9, 11)	1.25 ns	1.25 ns
Clock Cycle Time (t_{CK12}, CWL=9, 11)	1.25 ns	1.25 ns
Clock Cycle Time (t_{CK13}, CWL=10, 12)	1.071 ns	1.071 ns
Clock Cycle Time (t_{CK14}, CWL=10, 12)	1.071 ns	1.071 ns
Clock Cycle Time (t_{CK15}, CWL=11, 14)	0.937 ns	0.937 ns
Clock Cycle Time (t_{CK16}, CWL=11, 14)	0.937 ns	0.937 ns
Clock Cycle Time (t_{CK17}, CWL=12, 16)	0.833 ns	0.833 ns
Clock Cycle Time (t_{CK18}, CWL=12, 16)	0.833 ns	0.833 ns
Clock Cycle Time (t_{CK19}, CWL=14, 18)	0.75 ns	0.75 ns
Clock Cycle Time (t_{CK20}, CWL=14, 18)	0.75 ns	0.75 ns
Clock Cycle Time (t_{CK22}, CWL=16, 20)	-	0.625 ns
Clock Cycle Time (t_{CK24}, CWL=16, 20)	-	0.625 ns
System Frequency ($f_{ck\ max}$)	1333 MHz	1600 MHz

Specifications

- Density: 8Gbits
- Organization:
  - 16 banks x 64M words x 8 bits
- Package:
  - 78-ball FBGA for x8
- Power supply (JEDEC standard 1.2V)
  - V_{DD} = 1.2 ± 0.06V
  - V_{PP} = 2.5V (2.375V - 2.75V)
- Data rate: 2666Mbps/3200Mbps
- 16 internal banks
  - 16 banks (4 banks x 4 bank groups)
- Interface: Pseudo Open Drain (POD)
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- $\overline{\text{CAS}}$ Latency (CL): 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24
- $\overline{\text{CAS}}$ Write Latency (CWL): 9, 10, 11, 12, 14, 16, 18, 20
- On-Die Termination (ODT): nom. Values of RZQ/7, RZQ/5 (RZQ = 240Ω)
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles:
  - Average refresh period
    Commercial: 7.8 µs at 0°C ≤ Tcase ≤ +85°C
    3.9 µs at +85°C < Tcase ≤ +95°C
    Industrial: 7.8 µs at -40°C ≤ Tcase ≤ +85°C
    3.9 µs at +85°C < Tcase ≤ +95°C
- Operating case temperature range
  - Commercial: 0°C ≤ Tcase ≤ +95°C
  - Industrial: -40°C ≤ Tcase ≤ +95°C

Option	*Marking*
• Configuration	
- 1Gx8 (16 banks x 64Mbit x 8)	8G08
• Package	
- 78-ball FBGA (7.5mm x 12mm)	B
• Leaded/Lead-free	
- Leaded	<blank>
- Lead-free/RoHS	G
• Speed/Cycle Time	
- 0.75 ns @ CL19 (DDR4-2666)	-075
- 0.625 ns @ CL22 (DDR4-3200)	-062
• Temperature	
- Commercial 0°C to +95°C Tcase	<blank>
- Industrial -40°C to +95°C Tcase	I

Example Part Number: IM8G08D4GBBG-062I

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipe-lined architecture
- Bi-directional differential data strobe (DQS and $\overline{DQS}$) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation
- Data Bus Inversion (DBI)
  - Improve the power consumption and signal integrity of the memory interface
- Programmable preamble is supported both of $1t_{CK}$ and $2t_{CK}$ mode
- Command Address (CA) Parity for command/address signal error detect and inform it to controller
- V_{REFDQ} training
  - V_{REFDQ} generate inside DRAM and further train per DRAM
- Per DRAM Addressability (PDA)
  - Each DRAM can be set a different mode register value individually and has individual adjustment
- Fine granularity refresh
  - 2x, 4x mode for smaller t_{RFC}
- Maximum power saving mode for the lowest power consumption with no internal refresh activity
- Programmable Partial Array Self-Refresh (PASR)
- $\overline{RESET}$ pin for Power-up sequence and reset function

Part Number Information

IM 8G 08 D4 G B B G - 062 (I)

Intelligent Memory

IC capacity
8G = 8 Gigabit

DRAM I/O width
8 = x8

Memory Type
D4 = DDR4 SDRAM

Voltage
G = 1.2V

IC Revision
B = Revision B

Temperature range
Blank = Commercial Temp. 0°C to +95°C Tcase
I = Industrial Temp. -40°C to +95°C Tcase
***Note**: The refresh rate nust be doubled when the Tcase operating temepature exceeds 85°C*

Speed Grade
075 = DDR4-2666 CL19-19-19
062 = DDR4-3200 CL22-22-22

RoHS-compliance
G = Green / RoHS
Blank = Leaded

Package
B = FBGA

8Gb DDR4 SDRAM Addressing

Configuration	**1Gb x 8**
# of Bank	16
Bank group address	BG0 ~ BG1
Bank address	BA0 ~ BA1
Row Address	A0 ~ A15
Column Address	A0 ~ A9
Page size	1 KB

Pin Configurations

78-ball FBGA (x8 configuration)

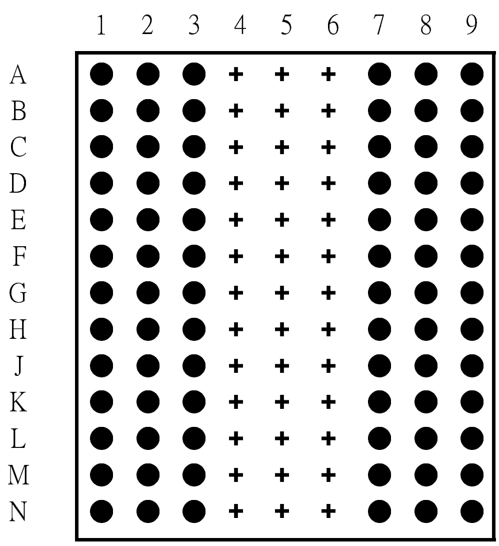
	1	2	3	4	5	6	7	8	9	
A	V_{DD}	V_{SSQ}	$\overline{TDQS}$				$\overline{DM}$, $\overline{DBI}$, TDQS	V_{SSQ}	V_{SS}	A
B	V_{PP}	V_{DDQ}	$\overline{DQS}$				DQ1	V_{DDQ}	ZQ	B
C	V_{DDQ}	DQ0	DQS				V_{DD}	V_{SS}	V_{DDQ}	C
D	V_{SSQ}	DQ4	DQ2				DQ3	DQ5	V_{SSQ}	D
E	V_{SS}	V_{DDQ}	DQ6				DQ7	V_{DDQ}	V_{SS}	E
F	V_{DD}	NC	ODT				CK	$\overline{CK}$	V_{DD}	F
G	V_{SS}	NC	CKE				$\overline{CS}$	NC	TEN	G
H	V_{DD}	$\overline{WE}$ /A14	$\overline{ACT}$				$\overline{CAS}$ /A15	$\overline{RAS}$	V_{SS}	H
J	V_{REFCA}	BG0	A10/AP				A12/$\overline{BC}$	BG1	V_{DD}	J
K	V_{SS}	BA0	A4				A3	BA1	V_{SS}	K
L	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	L
M	V_{DD}	A8	A2				A9	A7	V_{PP}	M
N	V_{SS}	A11	PAR				NC	A13	V_{DD}	N

Ball Location (x8)

● Populated ball

✚ Ball not populated

Top view
(See the balls through the package)

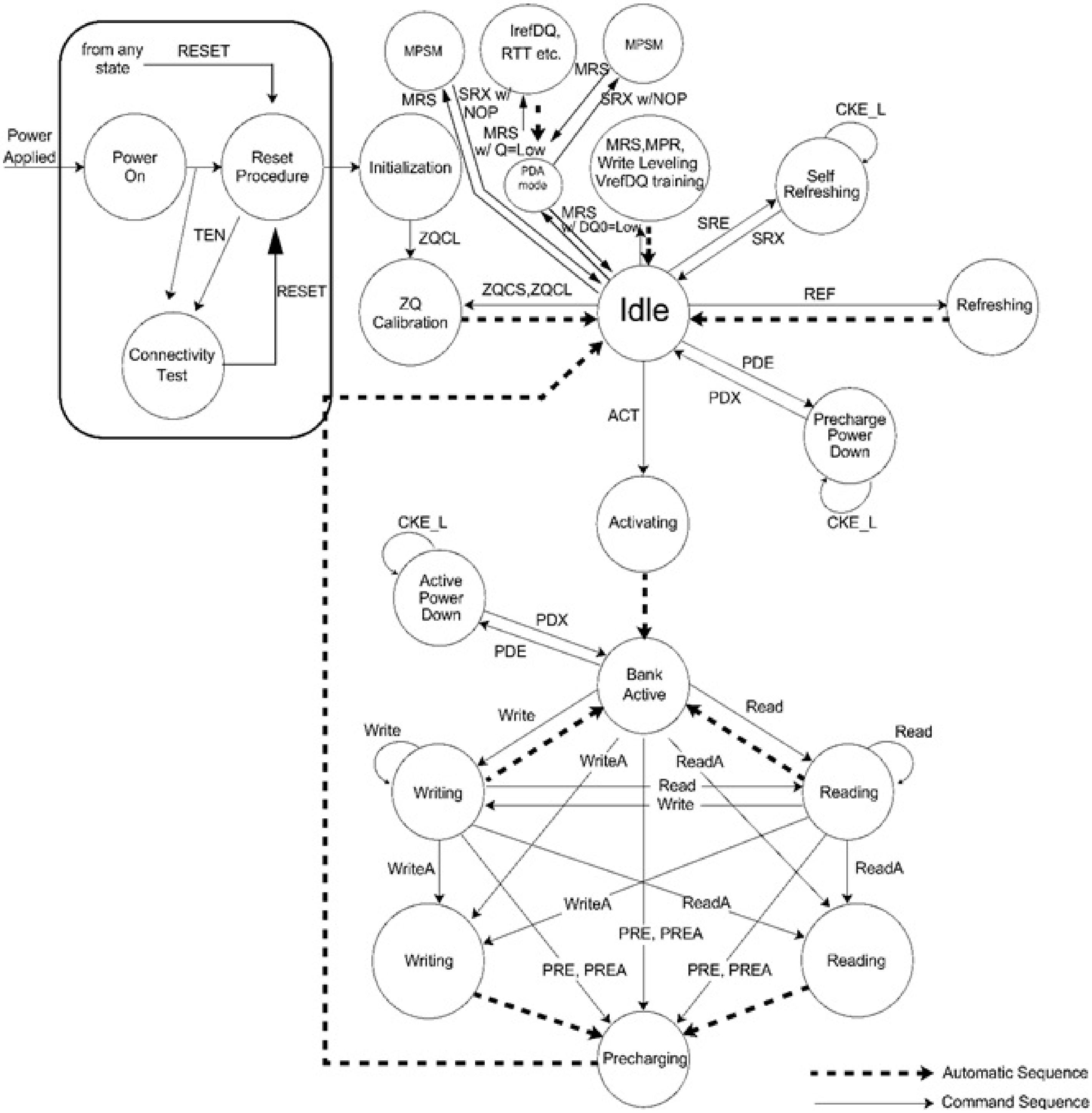


Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh oper-ation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power- down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and $\overline{DM}$/$\overline{DBI}$/TDQS, NU/$\overline{TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
$\overline{ACT}$	Input	**Activation Command Input:** $\overline{ACT}$ defines the Activation command being entered along with $\overline{CS}$. The input into $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 will be considered as Row Address A16, A15 and A14.
$\overline{RAS}$ $\overline{CAS}$/A15 $\overline{WE}$/A14	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$/A15 and $\overline{WE}$/A14 (along with $\overline{CS}$) define the command being entered. Those pins have multi function. For example, for activation with $\overline{ACT}$ Low, those are Addressing like A14 but for non-activation command with $\overline{ACT}$ High, those are Command pins for Read, Write and other command defined in command truth table.
$\overline{DM}$, $\overline{DBI}$	Input/ Output	**Input Data Mask and Data Bus Inversion:** $\overline{DM}$ is an input mask signal for write data. Input data is masked when $\overline{DM}$ is sampled LOW coincident with that input data during a Write access. $\overline{DM}$ is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. $\overline{DBI}$ is an input/output identifying whether to store/output the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if $\overline{DBI}$ is HIGH. TDQS is only supported in X8.
BG0 – BG1	Input	**Bank Group Inputs:** BG0 – BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 – BA1	Input	**Bank Address Inputs:** BA0 – BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 – A15	Input	**Address Inputs:** Provided the row address for ACTIVATE Commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$, $\overline{RAS}$, $\overline{CAS}$/A15, $\overline{WE}$/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Auto-precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: No Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.

Pin	Type	Function
A12 / $\overline{\text{BC}}$	Input	**Burst Chop:** A12/$\overline{\text{BC}}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
$\overline{\text{RESET}}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.
DQ	Input/ Output	**Data Input/ Output:** Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal V_{ref} level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS, $\overline{\text{DQS}}$	Input/ Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals $\overline{\text{DQS}}$ respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, $\overline{\text{TDQS}}$	Output	**Termination Data Strobe:** TDQS/$\overline{\text{TDQS}}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 0 in MR1, the DRAM will enable the same termination resistance function on TDQS/$\overline{\text{TDQS}}$ that is applied to DQS/$\overline{\text{DQS}}$. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, A12, A10 and $\overline{\text{TDQS}}$ is not used.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{\text{ACT}}$, $\overline{\text{RAS}}$/A16, $\overline{\text{CAS}}$/A15, $\overline{\text{WE}}$/A14,BG0-BG1,BA0-BA1 and A16-A0. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and when $\overline{\text{CS}}$ is low.
$\overline{\text{ALERT}}$	Input/ Output	**Alert:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then $\overline{\text{ALERT}}$ goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then $\overline{\text{ALERT}}$ goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, $\overline{\text{ALERT}}$ Pin must be bounded to V_{DD} on board.
TEN	Input	**Connectivity Test Mode Enable:** Optional input on x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of V_{DD}. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to V_{SS}.
NC		No connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.2V +/- 0.06V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.2V +/- 0.06V
V_{SS}	Supply	Ground
V_{PP}	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
Notes: Input only pins (BG0-BG1, BA0-BA1, A0-A15, $\overline{\text{ACT}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$/A15, $\overline{\text{WE}}$/A14, $\overline{\text{CS}}$, CKE, ODT, and $\overline{\text{RESET}}$) do not supply termination.		

Simplified State Diagram



ACT = Activate
PRE = Precharge
PREA = PRECHARGE All
MRS = Mode Register Set
REF = Refresh, Fine granularity Refresh
TEN = Boundary Scan Mode Enable

Read = RD, RDS4, RDS8
Read A = RDA, RDAS4, RDAS8
Write = WR, WRSR, WRS8 with/without CRC
Write A = WRA, WRAS4, WRAS8 with/without CRC
RESET = Start RESET procedure

PDE = Enter Power-down
PDX = Exit Power-down
SRE = Self-Refresh entry
SRX = Self-Refresh exit
MPR = Multi Purpose Register

Basic Functionality

The DDR4 SDRAM is high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.
The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfer at the I/O pins.
Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x8 select the bankgroup; BA0-BA1 select the bank; A0-A14 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.8 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.
Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR settings need to be defined.
Gear down mode (MR3 A[3]) : 0 = 1/2 Rate
Per DRAM Addressability (MR3 A[4]) : 0 = Disable
Max Power Saving Mode (MR4 A[1]) : 0 = Disable
CS to Command/Address Latency (MR4 A[8:6]) : 000 = Disable
CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable
Hard Post Package Repair mode (MR4 A[13]) : 0 = Disable
Soft Post Package Repair mode (MR4 A[5]) : 0 = Disable

Power-up and Initialization Sequence

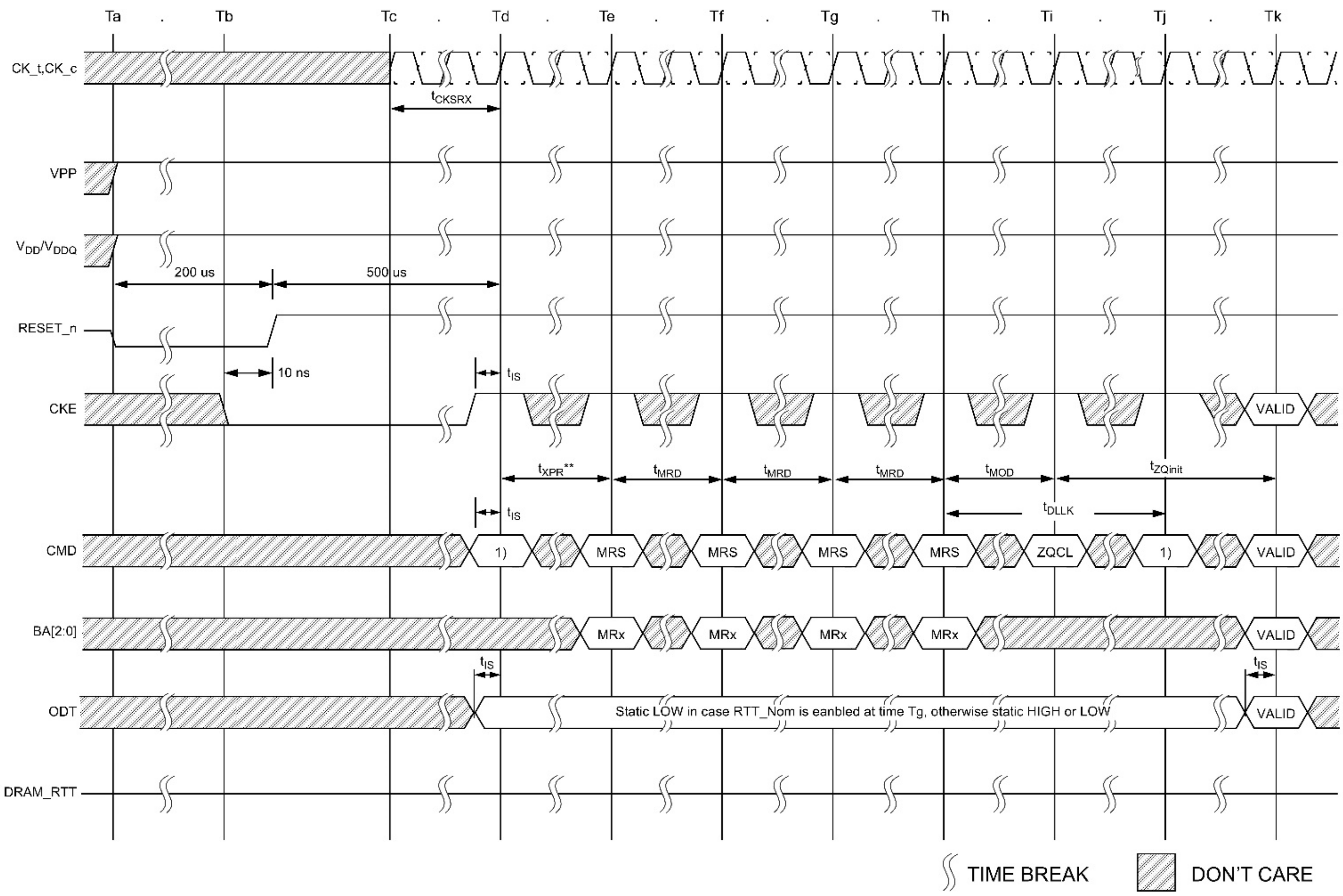
The following sequence is required for POWER UP and Initialization.

1. Apply power ($\overline{\text{RESET}}$ and TEN are recommended to be maintained below 0.2 x V_{DD}; all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained below 0.2 x V_{DD} for minimum 200µs with stable power and TEN needs to be maintained below 0.2 x V_{DD} for minimum 700µs with stable power. CKE is pulled "Low" anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be greater than 200ms; and during the ramp. $V_{DD} \geq V_{DDQ}$ and $(V_{DD}-V_{DDQ}) < 0.3V$. V_{PP} must ramp at the same time or earlier than V_{DD} and V_{PP} must be equal to or higher than V_{DD} at all times.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.76V max once power ramp is finished, AND
   - V_{REFCA} tracks V_{DD}/2.

   Or
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REFCA}.
   - Apply V_{PP} without any slope reversal before or at the same time as V_{DD}.
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After $\overline{\text{RESET}}$ is deasserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or $5t_{CK}$ (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also a Deselect command must be registered (with t_{IS} set up time to clock) at clock edge Td. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequences finished, including expiration of t_{DLLK} and t_{ZQinit}.
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{DLLK} and t_{ZQinit}.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, t_{XPR}, before issuing the first MRS command to load mode register.(t_{XPR}=Max(t_{XS}, $5t_{CK}$))

6. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BG0, “High” to BA1, BA0.)
7. Issue MRS Command to load MR6 with all application settings. (To issue MRS command for MR6, provide “Low” to BA0, “High” to BG0, BA1.)
8. Issue MRS Command to load MR5 with all application settings. (To issue MRS command for MR5, provide “Low” to BA1, “High” to BG0, BA0.)

9. Issue MRS Command to load MR4 with all application settings. (To issue MRS command for MR4, provide “Low” to BA1, BA0, “High” to BG0.)
10. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BG0, BA0, “High” to BA1.)
11. Issue MRS Command to load MR1 with all application settings. (To issue MRS command for MR1, provide “Low” to BG0, BA1, “High” to BA0.)
12. Issue MRS Command to load MR0 with all application settings. (To issue MRS command for MR0, provide “Low” to BG0, BA1, BA0.)
13. Issue ZQCL command to starting ZQ calibration.
14. Wait for both t_{DLLK} and $t_{ZQ\ init}$ completed.
15. The DDR4 SDRAM is now ready for Read/Write training (include V_{ref} training and Write leveling).



NOTE 1 From time point ‘Td’ until ‘Tk’, DES commands must be applied between MRS and ZQCL commands.
NOTE 2 MRS Commands must be issued to all Mode Registers that have defined settings.

RESET and Initialization Sequence at Power-on Ramping

V_{DD} Slew rate at Power-up Initialization Sequence

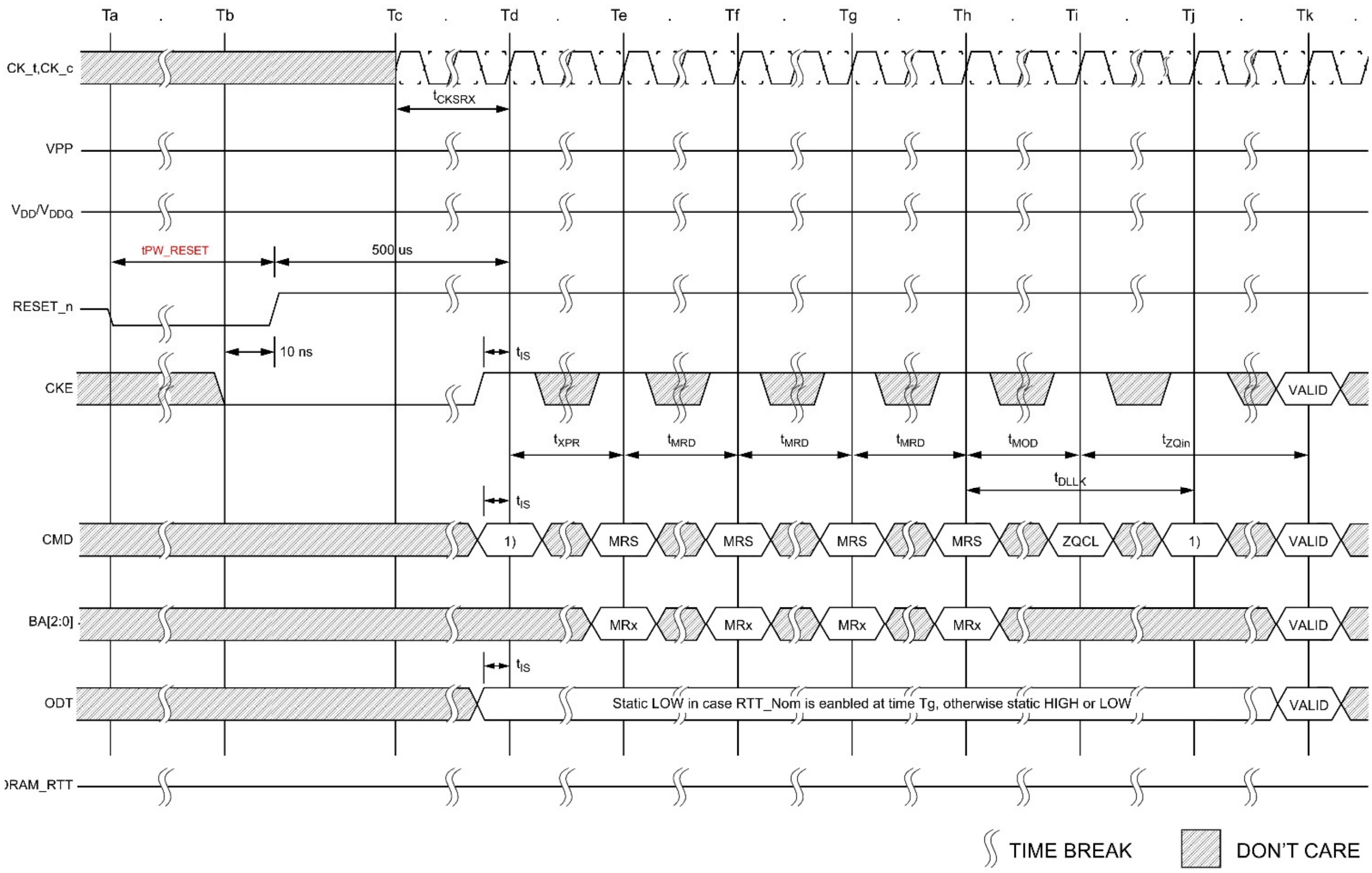
Symbol	Min.	Max.	Units
V_{DD}_sl[1]	0.004	600	V/ms[2]
V_{DD}_on[1]	-	200	ms[3]

1. Measurement made between 300mV and 80% V_{DD} minimum.
2. 20MHz bandlimited measurement.
3. Maximum time to ramp V_{DD} from 300mV to V_{DD} minimum.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption.

1. Asserted $\overline{\text{RESET}}$ below 0.2 * V_{DD} anytime when reset is needed (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum t_{PW_RESET}. CKE is pulled "LOW" before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns).
2. Follow steps 2 to 10 in "Power-up Initialization Sequence".
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include V_{ref} training and Write leveling).



NOTE 1 From time point 'Td' until 'Tk', DES commands must be applied between MRS and ZQCL commands
NOTE 2 MRS Commands must be issued to all Mode Registers that have defined settings.

Reset Procedure at Power Stable

Mode Register MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13[5], A11:A9	WR and RTP[2,3]	Write Recovery and Read to Precharge for auto precharge (see Table Write Recovery and Read to Precharge (cycles))
A8	DLL Reset	0 = No 1 = Yes
A7	TM	0 = Normal 1 = Test
A12, A6:A4, A2	CAS Latency[4]	(see Table CAS Latency)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed), Abbreviated BL8MRS 01 = BC4 or 8 (on the fly), Abbreviated BC4OTF or BL8OTF 10 = BC4 (Fixed), Abbreviated BC4MRS 11 = Reserved

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.
3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to speed bin tables for each frequency. CAS Latency controlled by A12 is optional for 4Gb device.
5. A13 for WR and RTP setting is optional for 4Gb.

Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27 (only 3DS available)
1	0	0	1	1	28
1	0	1	0	0	reserved for 29
1	0	1	0	1	30
1	0	1	1	0	reserved for 31
1	0	1	1	1	32
1	1	0	0	0	reserved

Mode Register MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[3]
A17	RFU	0 = must be programmed to 0 during MRS
A13, A6, A5	Rx CTLE control	000 = Vendor Optimized Setting (default) 001 = vendor defined 010 = vendor defined 011 = vendor defined 100 = vendor defined 101 = vendor defined 110 = vendor defined 111 = vendor defined
A12	Qoff[1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table RTT_NOM)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A4, A3	Additive Latency	00 = 0(AL disabled) 01 = CL-1 10 = CL-2 11 = Reserved
A2, A1	Output Driver Impedance Control	(see Table Output Driver Impedance Control)
A0	DLL Enable	0 = Disable[2] 1 = Enable

Notes:

1. Output disabled – DQs, DQS_ts, DQS_cs.
2. States reserved to “0 as Disable” with respect to DDR4.
3. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn’t respond. When RFU MR mode setting is inputted, DRAM operation is not defined.

RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

Mode Register MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
A11, A10:A9	RTT_WR	(see Table RTT_WR)
A8, A2	RFU	0 = must be programmed to 0 during MRS
A7:A6	Low Power Auto Self Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency (CWL)	(see Table CWL (CAS Write Latency))
A1:A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond. When RFU MR mode setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CWL (CAS Write Latency)

A5	A4	A3	CWL	Operating Data Rate in MT/s for 1 t_{CK} Write Preamble		Operating Data Rate in MT/s for 2 t_{CK} Write Preamble[1]	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	2933/3200	2400	2666	2400
1	1	0	18	-	2666	2933/3200	2666
1	1	1	20	-	2933/3200	-	2933/3200

Notes:

1. The 2 t_{CK} Write Preamble is valid for DDR4-2400/2666/2933/3200 Speed Grade. For the 2nd Set of 2 t_{CK} Write Preamble, no additional CWL is needed.

Mode Register MR3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:11	MPR Read Format	00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table MR3 A<10:9> Write Command Latency when CRC and DM are both enabled)
A8:A6	Fine Granularity Refresh Mode	(see Table Fine Granularity Refresh Mode)
A5	Temperature sensor readout	0 = disabled 1 = enabled
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 01 = Page1 10 = Page2 11 = Page3 (see Table MPR Data Format)

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond. When RFU MR mode setting is inputted, DRAM operation is not defined.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write Command Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866, 2133, 2400, 2666
1	0	6nCK	2933, 3200
1	1	RFU	RFU

MPR Data Format

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Notes
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Notes
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only
	01 = MPR1	$\overline{\text{CAS}}$/A15	$\overline{\text{WE}}$/A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	$\overline{\text{ACT}}$	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	$\overline{\text{RAS}}$/A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[4]			C[2]	C[1]	C[0]	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

Notes:

1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3.
2. For higher density of DRAM, where A[17] is used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.
4. MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Notes
BA1:BA0	00 = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status		CRC Write Enable	Rtt_WR		Read-only
		-	-	MR2	-	-	MR2	MR2		
		-	-	A11	-	-	A12	A10	A9	
	01 = MPR1	V_{REF} DQ Tmg range	V_{REF} DQ training Value						Geardown Enable	
		MR6	MR6						MR3	
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency					CAS Write Latency			
		MR0					MR2			
		A6	A5	A4	A2	A12	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance		
		MR1			MR5			MR1		
		A10	A9	A6	A8	A7	A6	A2	A1	

MR3 bit for Temperature Sensor Readout

MR3 bit A5 = 1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5 = 0: DRAM disables updates to the temperature sensor status in MPR Page2 (MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> t_{REFI})
0	1	1X refresh rate (= t_{REFI})
1	0	2X refresh rate (1/2 * t_{REFI})
1	1	rsvd

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Notes
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	11 = MPR3	don't care	don't care	don't care	don't care	MAC	MAC	MAC	MAC	

Notes:

1. MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

Mode Register MR4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	hPPR	0 = Disable 1 = Enable
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self Refresh Abort	0 = Disable 1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 001 = 3 010 = 4 011 = 5 100 = 6 101 = 8 110 = Reserved 111 = Reserved (see Table CS to CMD / ADDR Latency Mode Setting)
A5	sPPR	0 = Disable 1 = Enable
A4	Internal V_{REF} Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond. When RFU MR mode setting is inputted, DRAM operation is not defined.

CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

Mode Register MR5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent Error	0 = Disable 1 = Enable
A8:A6	RTT_PARK	(see Table RTT_PARK)
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	C/A Parity Latency Mode	(see Table C/A Parity Latency Mode)

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn’t respond. When RFU MR mode setting is inputted, DRAM operation is not defined.
2. When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	-
0	0	1	4	1600, 1866, 2133
0	1	0	5	2400, 2666
0	1	1	6	2933, 3200
1	0	0	8	RFU
1	0	1	Reserved	-
1	1	0	Reserved	-
1	1	1	Reserved	-

Notes:

1. Parity latency must be programmed according to timing parameters by speed grade table.

Mode Register MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13, A9, A8	RFU	-
A12:A10	t_{CCD_L}	(see Table t_{CCD_L} & t_{DLLK})
A7	V_{REFDQ} Training Enable	0 = Disable (Normal operation Mode) 1 = Enable (Training Mode)
A6	V_{REFDQ} Training Range	(see Table V_{REFDQ} Training: Range)
A5:A0	V_{REFDQ} Training Value	(see Table V_{REFDQ} Training: Values)

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond.

C/A Parity Latency Mode

A12	A11	A10	tCCD_L.min (nCK)[1]	tDLLKmin (nCK)[1]	Notes
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate ≤ 2666Mbps (2666Mbps)
1	0	0	8		2666Mbps < Data rate ≤ 3200Mbps (2933/3200Mbps)
1	0	1	Reserved	-	-
1	1	0			-
1	1	1			-

Notes:

1. t_{CCD_L} / t_{DLLK} should be programmed according to the value defined in AC parameter table per operating frequency.

V_{REFDQ} Training: Range

A6	V_{REFDQ} Range
0	Range 1
1	Range 2

V_{REFDQ} Training: Values

A5:A0	Range1	Range2
00 0000	60.00%	45.00%
00 0001	60.65%	45.65%
00 0010	61.30%	46.30%
00 0011	61.95%	46.95%
00 0100	62.60%	47.60%
00 0101	63.25%	48.25%
00 0110	63.90%	48.90%
00 0111	64.55%	49.55%
00 1000	65.20%	50.20%
00 1001	65.85%	50.85%
00 1010	66.50%	51.50%
001011	67.15%	52.15%
00 1100	67.80%	52.80%
00 1101	68.45%	53.45%
00 1110	69.10%	54.10%
00 1111	69.75%	54.75%
01 0000	70.40%	55.40%
01 0001	71.05%	56.05%
01 0010	71.70%	56.70%
01 0011	72.35%	57.35%
01 0100	73.00%	58.00%
01 0101	73.65%	58.65%
01 0110	74.30%	59.30%
01 0111	74.95%	59.95%
01 1000	75.60%	60.60%
01 1001	76.25%	61.25%

A5:A0	Range1	Range2
01 1010	76.90%	61.90%
01 1011	77.55%	62.55%
01 1100	78.20%	63.20%
01 1101	78.85%	63.85%
01 1110	79.50%	64.50%
01 1111	80.15%	65.15%
10 0000	80.80%	65.80%
10 0001	81.45%	66.45%
10 0010	82.10%	67.10%
10 0011	82.75%	67.75%
10 0100	83.40%	68.40%
10 0101	84.05%	69.05%
10 0110	84.70%	69.70%
10 0111	85.35%	70.35%
10 1000	86.00%	71.00%
10 1001	86.65%	71.65%
10 1010	87.30%	72.30%
10 1011	87.95%	72.95%
10 1100	88.60%	73.60%
10 1101	89.25%	74.25%
10 1110	89.90%	74.90%
10 1111	90.55%	75.55%
11 0000	91.20%	76.20%
11 0001	91.85%	76.85%
11 0010	92.50%	77.50%
11 0011 to 11 1111	Reserved	Reserved

Mode Register MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM. Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

Burst Length, Type and Order

Burst Length	Read/Write	Starting Column Address (A2, A1, A0)	Burst type = Sequential (decimal) A3=0	Burst type = Interleave (decimal) A3=1	Notes
4 Chop	READ	0 0 0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	1,2,3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	1,2,3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	1,2,3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	1,2,3
		1 0 0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	1,2,3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	1,2,3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	1,2,3
		1 1 1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	1,2,3
	WRITE	0,V,V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1,2,4,5
		1,V,V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1,2,4,5
8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	2
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	2
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	2
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	2
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	2
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	2
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	2
	WRITE	V,V,V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2,4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8. This means that the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/$\overline{BC}$, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks.
2. 0…7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.
3. Output driver for data and strobes are in high impedance.
4. V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don’t Care.

Command Truth Table

(a) Note 1,2,3,4 apply to the entire Command truth table.

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{\text{BC}}$=Burst Chop, X=Don't care, V=Valid]

Function	Abbreviation	CKE		$\overline{\text{CS}}$	$\overline{\text{ACT}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$ /A15	$\overline{\text{WE}}$ /A14	BG0 - BG1	BA0 - BA1	C2 - C0	A12 / $\overline{\text{BC}}$	A17, A13, A11	A10 / AP	A0 - A9	Notes
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	V	
Vsingle Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address(RA)			BG	BA	V	Row Address(RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	

Function	Abbreviation	CKE		CS	ACT	RAS	CAS /A15	WE /A14	BG0 - BG1	BA0 - BA1	C2 - C0	A12 / BC	A17, A13, A11	A10 / AP	A0 - A9	Notes
		Previous Cycle	Current Cycle													
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6

Notes:

1. All DDR4 SDRAM commands are defined by states of CS, ACT, RAS/A16, CAS/A15, WE/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA, and CA are device density and configuration dependent. When ACT = H; pins RAS/A16, CAS/A15 and WE/A14 are used as command pins RAS, CAS and WE respectively. When ACT = L; pins RAS/A16, CAS/A15 and WE/A14 are used as address pins A16, A15, and A14 respectively.
2. RESET is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank Group addresses (BG) and Banka addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operations.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Controller guarantees self refresh exit to be synchronous.
9. V_{PP} and V_{REF}(V_{REFCA}) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit.
11. Refer to the CKE Truth Table for more detail with CKE transition.
12. During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State[2]	CKE		Command (N) [3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See "Command Truth Table," on previous page					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to t_{CKEmin} being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command truth table.
8. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are DESELECT only.
12. Valid commands for Self-Refresh Exit are DESELECT only expect for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.
13. Self-Refresh can not be entered during Read or Write operations. See 'Self-Refresh Operation" and 'Power-Down Modes" on later section for a detailed list of restrictions.
14. The Power-Down does not perform any refresh operations.
15. "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. It also applies to Address pins.
16. V_{PP} and V_{REF} (V_{REFCA}) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. 'Idle state' is defined as all banks are closed(t_{RP},t_{DAL},etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, etc.).

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.3 ~ 1.5	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.3 ~ 1.5	V	1,3
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin expect V_{REFCA} relative to V_{SS}	-0.3 ~ 1.5	V	1,3
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REFCA} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; VREFCA may be equal to or less than 300mV.
4. V_{PP} must be equal or greater than V_{DD}/V_{DDQ} at all times.

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	1.14	1.2	1.26	V	1,2,3
V_{DDQ}	Supply voltage for Output	1.14	1.2	1.26	V	1,2,3
V_{PP}	DRAM activation power supply	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 20MHz.

Operating Temperature Conditions

Symbol	Parameter	Rating		Units
		Min.	Max.	
Tcase	Case operating temperature for Commercial temperature product	0	95	°C
Tcase	Case operating temperature for Industrial temperature product	-40	95	°C

Notes:

1. The operating temperature is the case surface temperature on the center-top side of the DDR4 device.

AC and DC Input Measurement Levels

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR4-2666/3200		Units	Notes
		Min.	Max.		
V_{IHCA} (DC75)	DC input logic high	-	-	V	
V_{ILCA} (DC75)	DC input logic low	-	-	V	
V_{IHCA} (DC65)	DC input logic high	V_{REFCA} + 0.065	V_{DD}		
V_{ILCA} (DC65)	DC input logic low	V_{SS}	V_{REFCA} - 0.065		
V_{IHCA} (AC100)	AC input logic high	-	-	V	
V_{ILCA} (AC100)	AC input logic low	-	-	V	
V_{IHCA} (AC90)	AC input logic high	V_{REF} + 0.09	Note2		
V_{ILCA} (AC90)	AC input logic low	Note2	V_{REF} - 0.09		
V_{REFCA} (DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	V	1,2

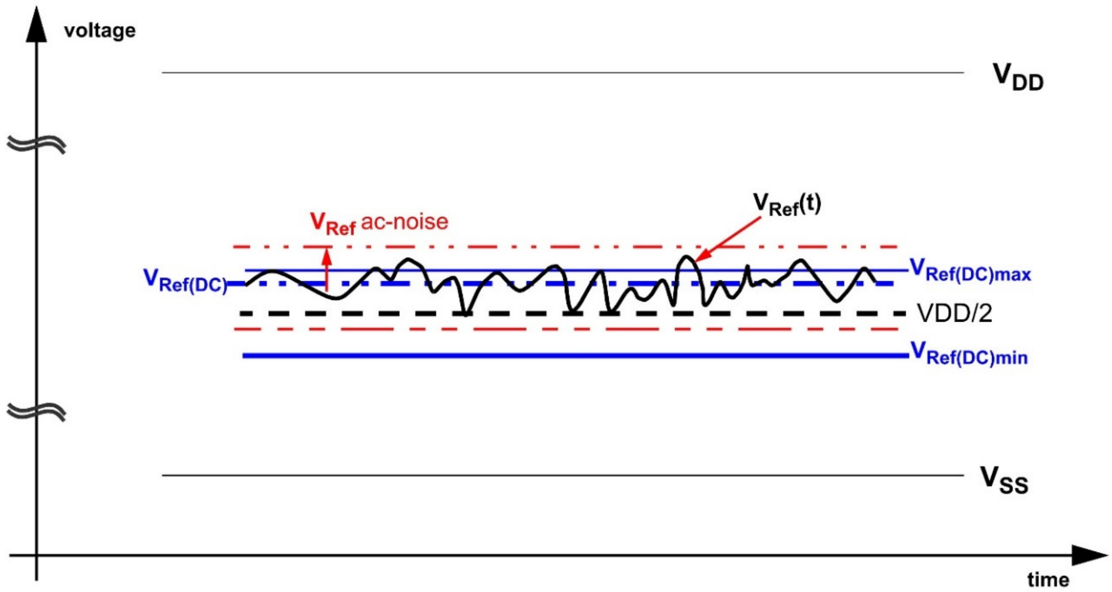
Notes:

1. The AC peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from V_{REFCA}(DC) by more than ± 1% V_{DD} (for reference: approx. ± 12mV).
2. For reference: approx. V_{DD}/2 ± 12mV

V_{REF} Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} is illustrated in figure V_{REF}(DC) tolerance and V_{REF} AC-noise limits. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA}).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table of "Single-Ended AC and DC Input Levels for Command and Address". Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% V_{DD}.



V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

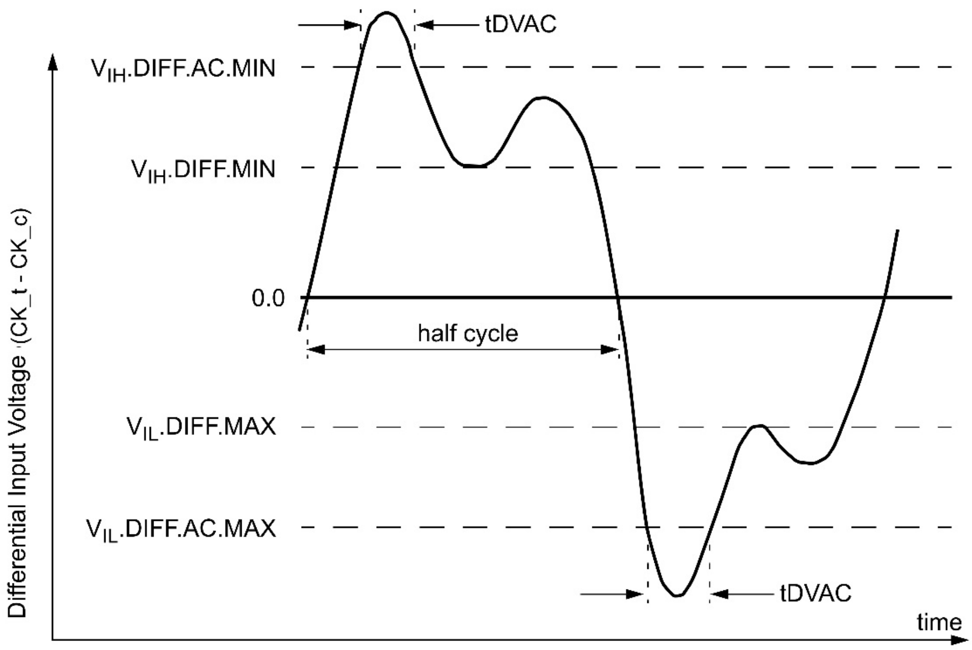
"V_{REF}" shall be understood as V_{REF}(DC), as defined in figure V_{REF}(DC) tolerance and V_{REF} AC-noise limits.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (± 1% of V_{DD}) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signals definition



Definition of differential ac-swing and “time above ac-level” t_{DVAC}

Notes:

1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

Differential swing requirements for clock (CK – $\overline{CK}$)

Differential AC and DC Input Levels

Symbol	Parameter	DDR4-2666		DDR4-3200		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IHdiff}	Differential input high	135	NOTE 3	110	NOTE 3	mV	1
V_{ILdiff}	Differential input low	NOTE3	-135	NOTE3	-110	mV	1
V_{IHdiff}(AC)	Differential input high AC	2 x (V_{IH}(AC) – V_{REF})	NOTE 3	2 x (V_{IH}(AC) – V_{REF})	NOTE 3	V	2
V_{ILdiff}(AC)	Differential input low AC	NOTE 3	2 x (V_{IL}(AC) – V_{REF})	NOTE 3	2 x (V_{IL}(AC) – V_{REF})	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use V_{IHCA}/V_{ILCA}(AC) of ADD/CMD and V_{REFCA}.
3. These values are not defined; however, the differential signals CK - $\overline{CK}$, need to be within the respective limits (V_{IHCA}(DC) max, V_{ILCA}(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (t_{DVAC}) for CK-$\overline{CK}$

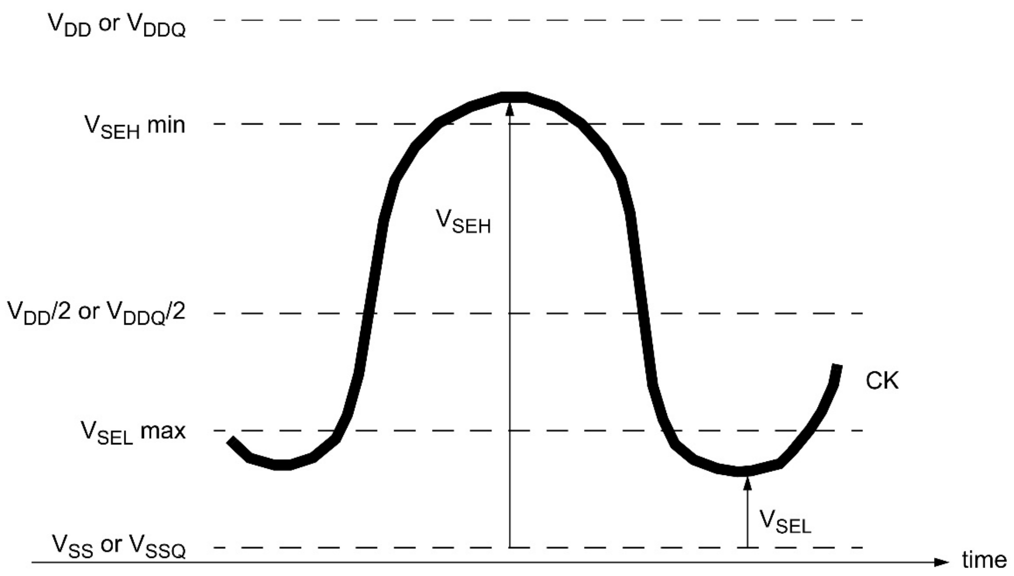
Slew Rate [V/ns]	t_{DVAC} [ps] @ |$V_{IH/Ldiff}$(AC)| = 200mV	
	Min.	Max.
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

Single-ended requirements for differential signals

Each individual component of a differential signal (CK, $\overline{CK}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ have to approximately reach V_{SEH} min / V_{SEL} max (approximately equal to the AC-levels (V_{IHCA}(AC) / V_{ILCA}(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable AC-levels for ADD/CMD might be different per speed-bin etc. E.g. if Different value than V_{IHCA}(AC100) / V_{ILCA}(AC100) is used for ADD/CMD signals, then these AC-levels apply also for the single-ended signals CK and $\overline{CK}$.



Single-ended requirement for differential signals

Note that while ADD/CMD signal requirements are with respect to V_{REFCA}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single- ended components of differential signals the requirement to reach V_{SEL} max, V_{SEH} min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, $\overline{CK}$

Symbol	Parameter	DDR4-2666		DDR4-3200		Units	Notes
		Min.	Max.	Min.	Max.		
V_{SEH}	Single-ended high-level for CK, $\overline{CK}$	$(V_{DD}/2) + 0.095$	NOTE 3	$(V_{DD}/2) + 0.085$	NOTE 3	V	1,2
V_{SEL}	Single-ended low-level for CK, $\overline{CK}$	NOTE 3	$(V_{DD}/2) - 0.095$	NOTE 3	$(V_{DD}/2) - 0.085$	V	1,2

Notes:

1. For CK-$\overline{CK}$ use V_{IHCA}/V_{ILCA}(AC) of ADD/CMD.
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA}.
3. These values are not defined, however the single-ended signals CK-$\overline{CK}$ need to be within the respective limits (V_{IHCA}(DC) max, V_{ILCA}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

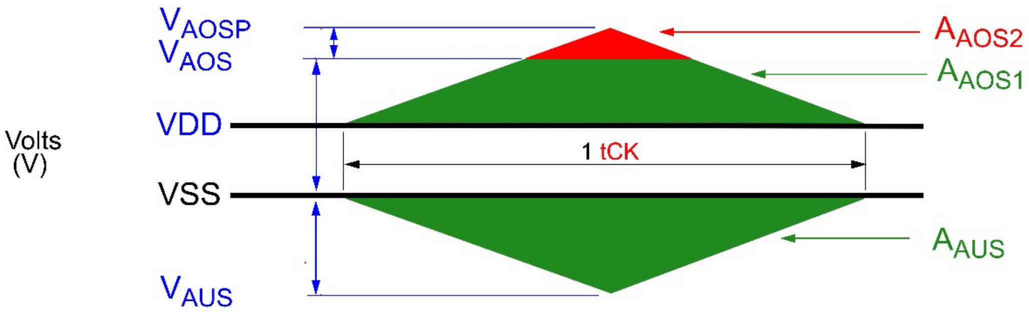
Address, Command and Control Overshoot and Undershoot specifications

AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Symbol	DDR4-2666/3200	Units	Notes
Maximum peak amplitude above V_{AOS}	V_{AOSP}	0.06	V	
Upper boundary of overshoot area A_{AOS1}	V_{AOS}	V_{DD} + 0.24	V	1
Maximum peak amplitude allowed for undershoot	V_{AUS}	0.30	V	
Maximum overshoot area per 1 t_{CK} above V_{AOS}	A_{AOS2}	0.0055	V-ns	
Maximum overshoot area per 1 t_{CK} between V_{DD} and V_{AOS}	A_{AOS1}	0.1699	V-ns	
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{AUS}	0.1762	V-ns	

Notes:

1. The value of V_{AOS} matches V_{DD} absolute max as defined in Table Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in Table Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{AOS} remains at V_{DD} absolute max.



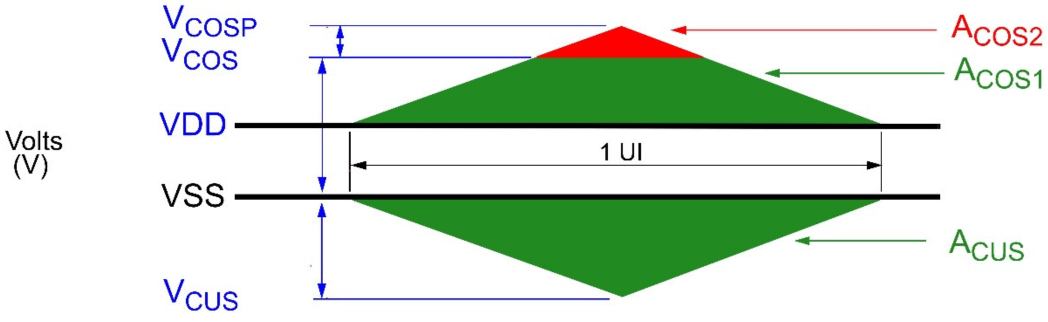
Address, Command and Control Overshoot and Undershoot Definition

AC overshoot/undershoot specification for Clock

Parameter	Symbol	DDR4-2666/3200	Units	Notes
Maximum peak amplitude above V_{COS}	V_{COSP}	0.06	V	
Upper boundary of overshoot area A_{DOS1}	V_{COS}	V_{DD} + 0.24	V	1
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.30	V	
Maximum overshoot area per 1 UI above V_{COS}	A_{COS2}	0.0025	V-ns	
Maximum overshoot area per 1 UI between V_{DD} and V_{DOS}	A_{COS1}	0.0750	V-ns	
Maximum undershoot area per 1 UI below V_{SS}	A_{CUS}	0.0762	V-ns	

Notes:

1. The value of V_{COS} matches V_{DD} absolute max as defined in Table Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in Table Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{COS} remains at V_{DD} absolute max.



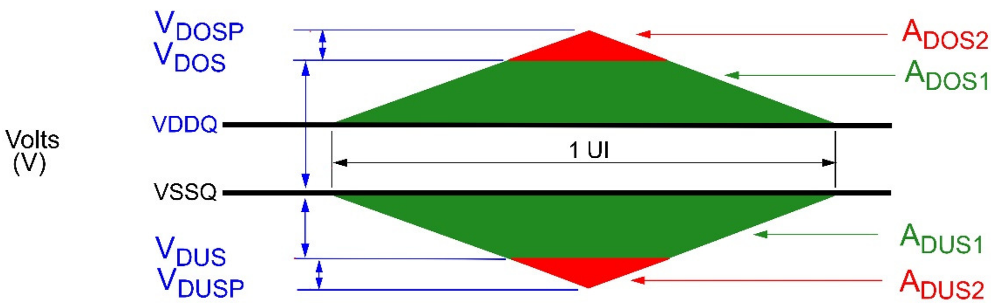
Clock Overshoot and Undershoot Definition

AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Symbol	DDR4-2666/3200	Units	Notes
Maximum peak amplitude above V_{DOS}	V_{DOSP}	0.16	V	
Upper boundary of overshoot area A_{DOS1}	V_{DOS}	V_{DDQ} + 0.24	V	1
Lower boundary of undershoot area A_{DUS1}	V_{DUS}	0.30	V	2
Maximum peak amplitude below V_{DUS}	V_{DUSP}	0.10	V	
Maximum overshoot area per 1 UI above V_{DOS}	A_{DOS2}	0.0100	V-ns	
Maximum overshoot area per 1 UI between V_{DDQ} and V_{DOS}	A_{DOS1}	0.0700	V-ns	
Maximum undershoot area per 1 UI below V_{SSQ} and V_{DUS1}	A_{DUS1}	0.0700	V-ns	
Maximum undershoot area per 1 UI below V_{DUS}	A_{DUS2}	0.0100	V-ns	

Notes:

1. The value of V_{DOS} matches (V_{IN}, V_{OUT}) max as defined in Table Absolute Maximum DC Ratings if V_{DDQ} equals V_{DDQ} max as defined in Table Recommended DC Operating Conditions. If V_{DDQ} is above the recommended operating conditions, V_{DOS} remains at (V_{IN}, V_{OUT}) max.
2. The value of V_{DUS} matches (V_{IN}, V_{OUT}) min as defined in Table Absolute Maximum DC Ratings.



Data, Strobe and Mask Overshoot and Undershoot Definition

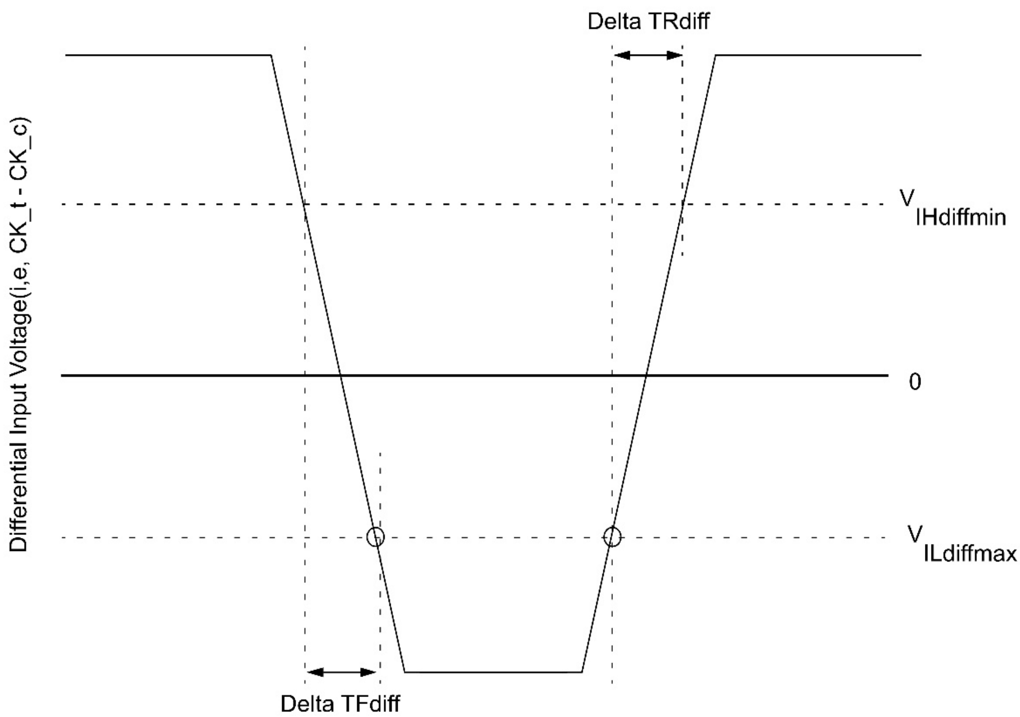
Slew Rate Definitions for Differential Input Signals (CK)

Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK – $\overline{CK}$)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$(V_{IHdiffmin} - V_{ILdiffmax})$ / Delta TRdiff
Differential input slew rate for falling edge (CK – $\overline{CK}$)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$(V_{IHdiffmin} - V_{ILdiffmax})$ / Delta TFdiff

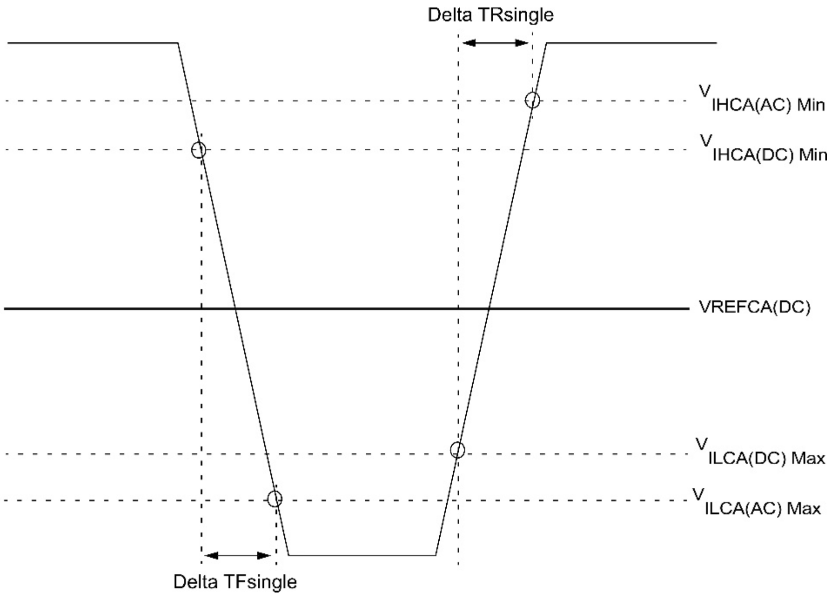
Notes:

1. The differential signal (i.e. CK – $\overline{CK}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for CK, $\overline{CK}$

Slew Rate Definition for Single-ended Input Signals (CMD/ADD)



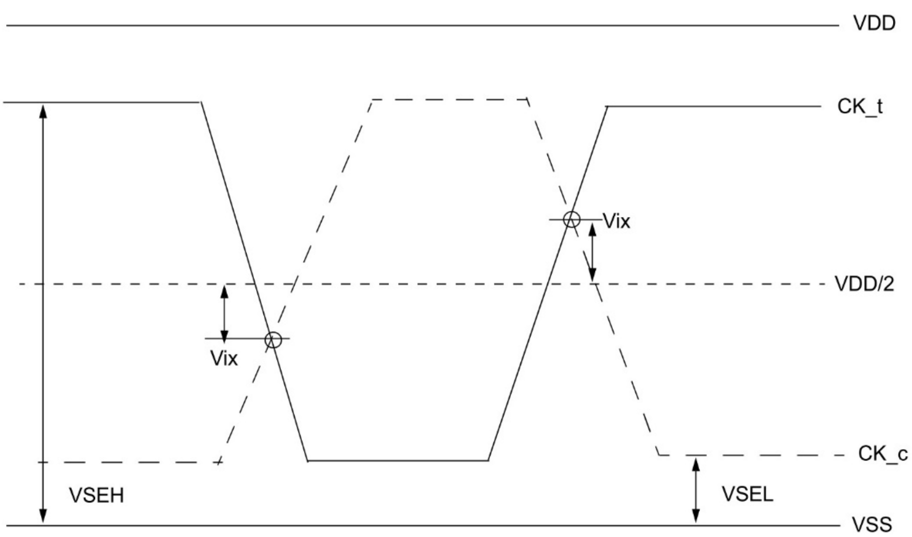
Single-ended Input Slew Rate definition for CMD and ADD

Notes:

1. Single-ended input slew rate for rising edge = { $V_{IHCA(AC)}$ Min – $V_{ILCA(DC)}$ Max } / Delta TR single
2. Single-ended input slew rate for falling edge = { $V_{IHCA(DC)}$ Min – $V_{ILCA(AC)}$ Max } / Delta TF single
3. Single-ended signal rising edge from $V_{ILCA(DC)}$ Max to $V_{IHCA(DC)}$ Min must be monotonic slope.
4. Single-ended signal falling edge from $V_{IHCA(DC)}$ Min to $V_{ILCA(DC)}$ Max must be monotonic slope.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK, $\overline{CK}$) must meet the requirements in Table Cross point voltage for differential input signals (CK). The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.



V_{IX} Definition (CK)

Cross point voltage for differential input signals (CK)

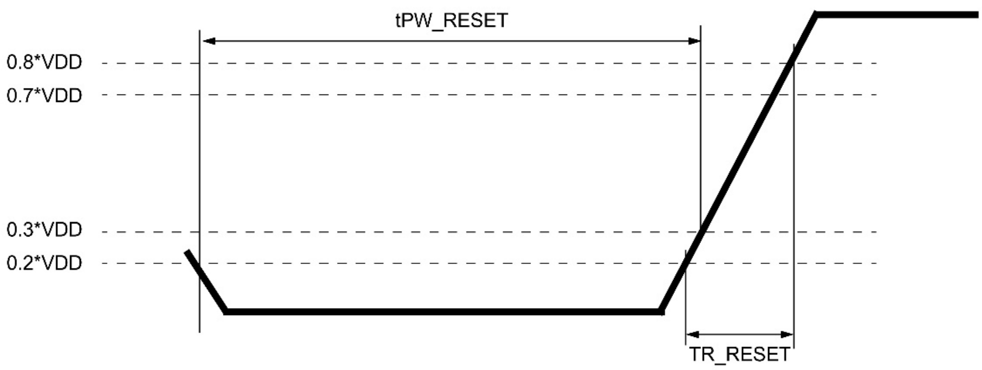
Symbol	Parameter	DDR4-2666/3200			
		Min.		Max.	
-	Area of V_{SEH}, V_{SEL}	V_{SEL} < V_{DD}/2 - 145 mV	V_{DD}/2 - 145 mV =< V_{SEL} =< V_{DD}/2 - 100 mV	V_{DD}/2 + 100 mV =< V_{SEL} =< V_{DD}/2 + 145 mV	V_{DD}/2 + 145mV < V_{SEH}
V_{IX}(CK)	Differential Input Cross Point Voltage relative to V_{DD}/2 for CK, $\overline{CK}$	-110 mV	- (V_{DD}/2 - V_{SEL}) + 30 mV	(V_{SEH} – V_{DD}/2) – 30 mV	110 mV

CMOS rail to rail Input Levels for $\overline{RESET}$

Parameter	Symbol	Min.	Max.	Units	Notes
AC Input High Voltage	$V_{IH(AC)}$_RESET	0.8*V_{DD}	V_{DD}	V	6
DC Input High Voltage	$V_{IH(DC)}$_RESET	0.7*V_{DD}	V_{DD}	V	2
DC Input Low Voltage	$V_{IL(DC)}$_RESET	VSS	0.3*V_{DD}	V	1
AC Input Low Voltage	$V_{IL(AC)}$_RESET	VSS	0.2*V_{DD}	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	t_{PW}_RESET	1.0	-	us	3,5

Notes:

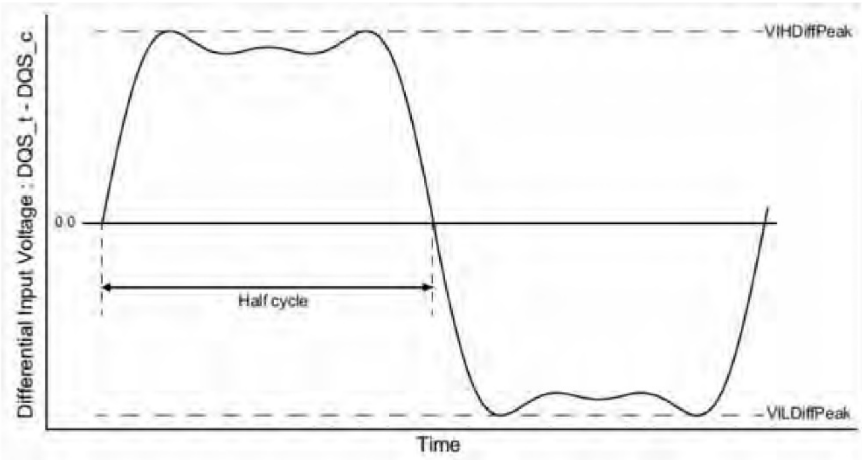
1. After $\overline{RESET}$ is registered LOW, $\overline{RESET}$ level shall be maintained below $V_{IL(DC)}$_RESET during t_{PW}_RESET, otherwise, SDRAM may not be reset.
2. Once $\overline{RESET}$ is registered HIGH, $\overline{RESET}$ level must be maintained above $V_{IH(DC)}$_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting $\overline{RESET}$ signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal (ringback) requirement during its level transition from Low to High.
5. This definition is applied only "RESET Procedure at Power Stable".
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.



$\overline{RESET}$ Input Slew Rating Definition

AC and DC Logic Input Levels for DQS Signals

Differential signal definition



Definition of differential DQS Signal AC-swing Level

Differential swing requirements for DQS (DQS - $\overline{DQS}$)

Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-2666		DDR4-3200		Units	Notes
		Min.	Max.	Min.	Max.		
$V_{IHDiffPeak}$	VIH.DIFF.Peak Voltage	150	Note2	140	Note2	mV	1
$V_{ILDiffPeak}$	VIL.DIFF.Peak Voltage	Note2	-150	Note2	-140	mV	1

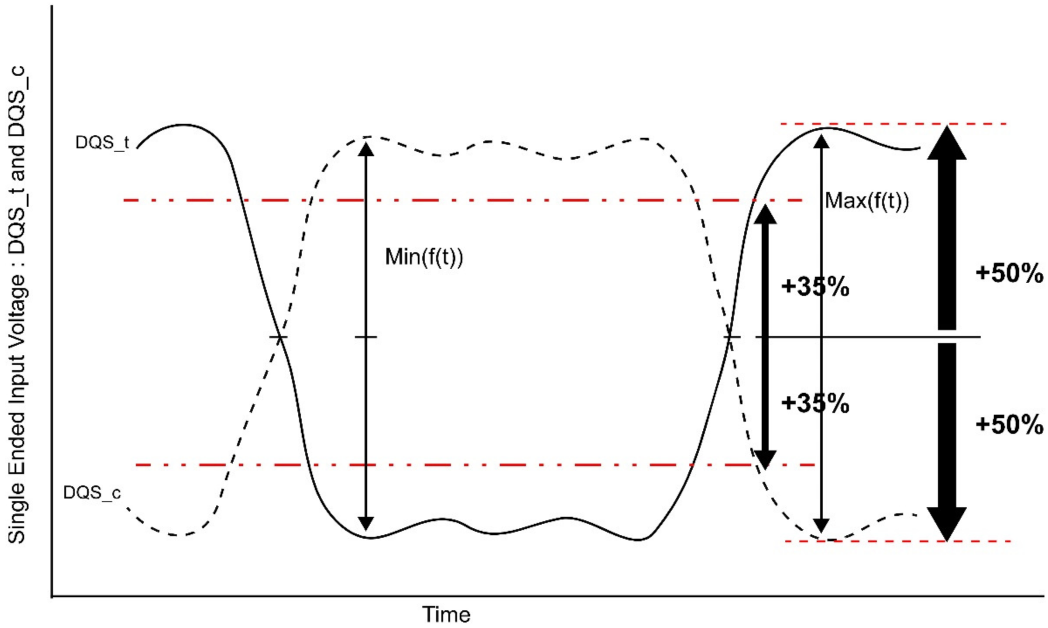
Notes:

1. Used to define a differential signal slew-rate.
2. These values are not defined; however, the differential signals DQS - $\overline{DQS}$, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.
VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Mix(f(t))
f(t) = $V_{DQS\_t} - V_{DQS\_c}$

The Max((f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.



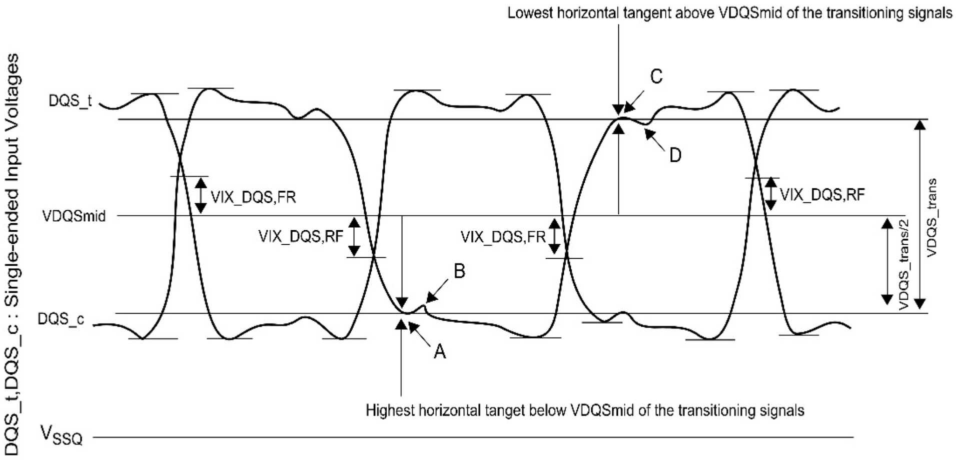
Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling

Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS, $\overline{DQS}$) must meet the requirements in Table Cross point voltage for DQS differential Input signals. The differential input cross point voltage V_{IX_DQS} (V_{IX}_DQS_FR and V_{IX}_DQS_RF) is measured from the actual cross point of DQS, $\overline{DQS}$ relative to the V_{DQSmid} of the DQS and $\overline{DQS}$ signals.

V_{DQSmid} is the midpoint of the minimum levels achieved by the transitioning DQS and $\overline{DQS}$ signals, and noted by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above V_{DQSmid} of the transitioning DQS signals and the highest horizontal tangent below V_{DQSmid} of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS rising) or VIL.DIFF.Peak Voltage ($\overline{DQS}$ rising), refer to Figure Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure V_{IX} Definition (DQS)) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure V_{IX} Definition (DQS)) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure V_{IX} Definition (DQS)) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure V_{IX} Definition (DQS)) is not a valid horizontal tangent.



V_{IX} Definition (DQS)

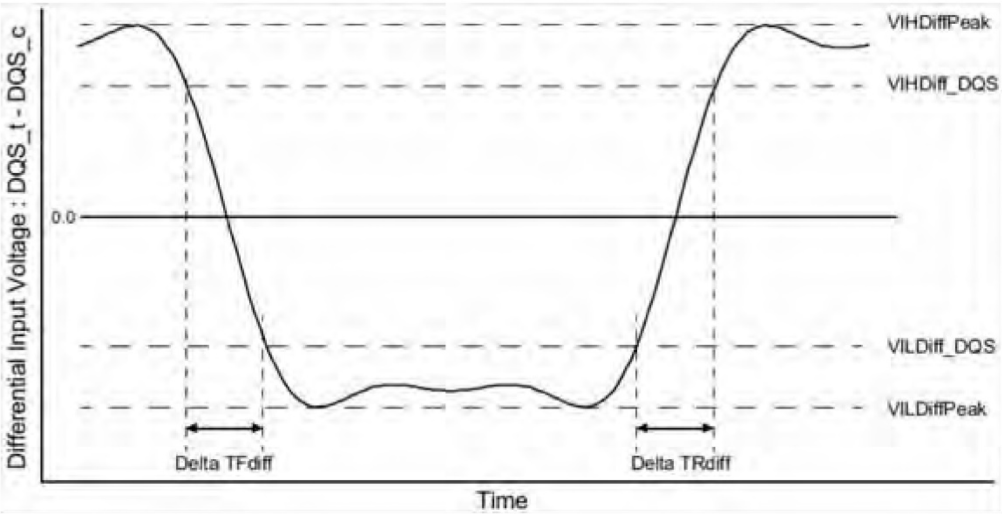
Cross point voltage for DQS differential Input signals

Symbol	Parameter	DDR4-2666/3200		Units	Notes
		Min.	Max.		
V_{IX}_DQS_Ratio	DQS and $\overline{DQS}$ crossing relative to the midpoint of the DQS and $\overline{DQS}$ signal swings	-	25	%	1,2,3
V_{DQSmid}_to_V_{cent}	V_{DQSmid} offset relative to V_{cent}_DQ(midpoint)	-	min(V_{IHdiff},50)	mV	3,4,5

Notes:

1. V_{IX}_DQS_Ratio is DQS V_{IX} crossing (V_{IX}_DQS_FR or V_{IX}_DQS_RF) divided by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above V_{DQSmid} of the transitioning DQS signals and the highest horizontal tangent below V_{DQSmid} of the transitioning DQS signals.
2. V_{DQSmid} will be similar to the V_{REFDQ} internal setting value obtained during V_{REF} Training if the DQS and DQs drivers and the paths are matched.
3. The maximum limit shall not exceed the smaller of V_{IHdiff} minimum limit or 50 mV.
4. V_{IX} measurements are only applicable for transitioning DQS and $\overline{DQS}$ signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter V_{DQSmid} is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

Differential Input Slew Rate Definition



Differential Input Slew Rate Definition for DQS, $\overline{DQS}$

Differential Input Slew Rate Definition for DQS, $\overline{DQS}$

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS to $\overline{DQS}$)	V_{ILDiff}_DQS	V_{IHDiff}_DQS	|V_{ILDiff}_DQS – V_{IHDiff}_DQS| / Delta TRdiff
Differential input slew rate for falling edge (DQS to $\overline{DQS}$)	V_{IHDiff}_DQS	V_{ILDiff}_DQS	|V_{ILDiff}_DQS – V_{IHDiff}_DQS| / Delta TFdiff

Differential Input Level for DQS, $\overline{DQS}$

Symbol	Parameter	DDR4-2666		DDR4-3200		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IHDiff}_DQS	Differential Input High	130	-	110	-	mV	
V_{ILDiff}_DQS	Differential Input Low	-	-130	-	-110	mV	

Differential Input Slew Rate for DQS, $\overline{DQS}$

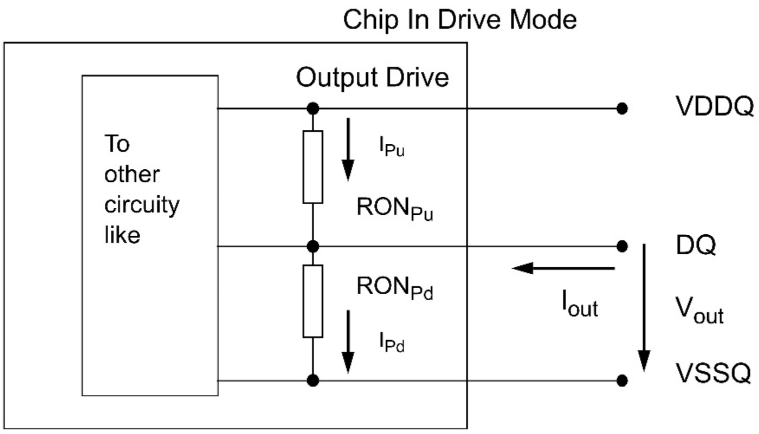
Symbol	Parameter	DDR4-2666/3200		Units	Notes
		Min.	Max.		
SRIdiff	Differential Input Slew Rate	2.5	18	V/ns	

Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong (low Ron) and weak mode (high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$RON_{Pu} = (V_{DDQ} - V_{out}) / | I_{out} |$
$RON_{Pd} = V_{out} / | I_{out} |$



Output driver

Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min.	Nom.	Max.	Units	Notes
34Ω	RON34Pd	$V_{OLdc} = 0.5*V_{DDQ}$	0.73	1	1.1	RZQ/7	1,2,6
		$V_{OMdc} = 0.8*V_{DDQ}$	0.83	1	1.1	RZQ/7	1,2,6
		$V_{OHdc} = 1.1*V_{DDQ}$	0.83	1	1.25	RZQ/7	1,2,6
	RON34Pu	$V_{OLdc} = 0.5*V_{DDQ}$	0.9	1	1.25	RZQ/7	1,2,6
		$V_{OMdc} = 0.8*V_{DDQ}$	0.9	1	1.1	RZQ/7	1,2,6
		$V_{OHdc} = 1.1*V_{DDQ}$	0.8	1	1.1	RZQ/7	1,2,6
48Ω	RON48Pd	$V_{OLdc} = 0.5*V_{DDQ}$	0.73	1	1.1	RZQ/7	1,2,6
		$V_{OMdc} = 0.8*V_{DDQ}$	0.83	1	1.1	RZQ/7	1,2,6
		$V_{OHdc} = 1.1*V_{DDQ}$	0.83	1	1.25	RZQ/7	1,2,6
	RON48Pu	$V_{OLdc} = 0.5*V_{DDQ}$	0.9	1	1.25	RZQ/7	1,2,6
		$V_{OMdc} = 0.8*V_{DDQ}$	0.9	1	1.1	RZQ/7	1,2,6
		$V_{OHdc} = 1.1*V_{DDQ}$	0.8	1	1.1	RZQ/7	1,2,6
Mismatch between pull-up and pull-down, MMPuPd		$V_{OMdc} = 0.8*V_{DDQ}$	-10	-	17	%	1,2,4,3
Mismatch DQ-DQ within byte variation pull-up, MMPudd		$V_{OMdc} = 0.8*V_{DDQ}$	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		$V_{OMdc} = 0.8*V_{DDQ}$	-	-	10	%	1,2,4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity (TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8*V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*V_{DDQ} and 1.1*V_{DDQ}.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd: Measure RONPu and RONPd both at 0.8*V_{DD} separately; RONNOM is the norminal Ron value

   MMPuPd = (RON_{Pu} – RON_{Pd}) / (RONNOM) *100
4. RON variance range ratio to RON Nominal value in a given component, including DQS and $\overline{DQS}$.

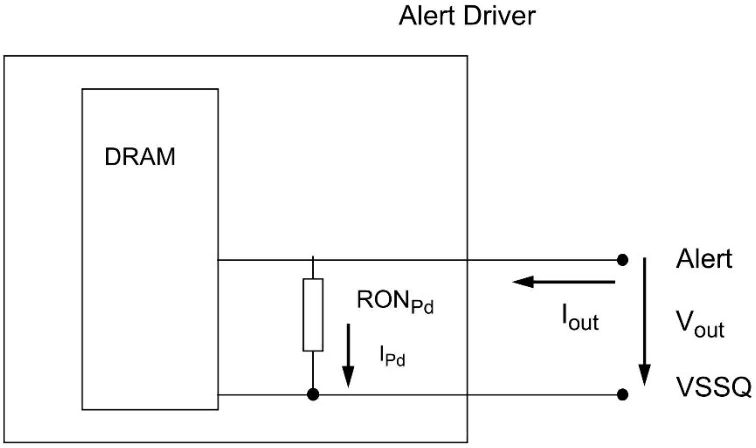
   MMPudd = (RON_{Pu} Max – RON_{Pu} Min) / (RONNOM) *100

   MMPddd = (RON_{Pd} Max – RON_{Pd} Min) / (RONNOM) *100
5. This parameter of x16 device is specified for Upper byte and Lower byte.
6. For IT device, the minimum values are reduced by TBD%.

$\overline{ALERT}$ output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |} \text{ under the condition that } RON_{Pu} \text{ is off}$$



Functional Representation of the Output Buffer

Output Driver Impedance

Resistor	V_{out}	Min.	Max.	Units	Notes
RON_{Pd}	V_{OLdc} = 0.1*V_{DDQ}	0.3	1.2	34Ω	1
	V_{OMdc} = 0.8*V_{DDQ}	0.4	1.2	34Ω	1
	V_{OHdc} = 1.1*V_{DDQ}	0.4	1.4	34Ω	1

Notes:

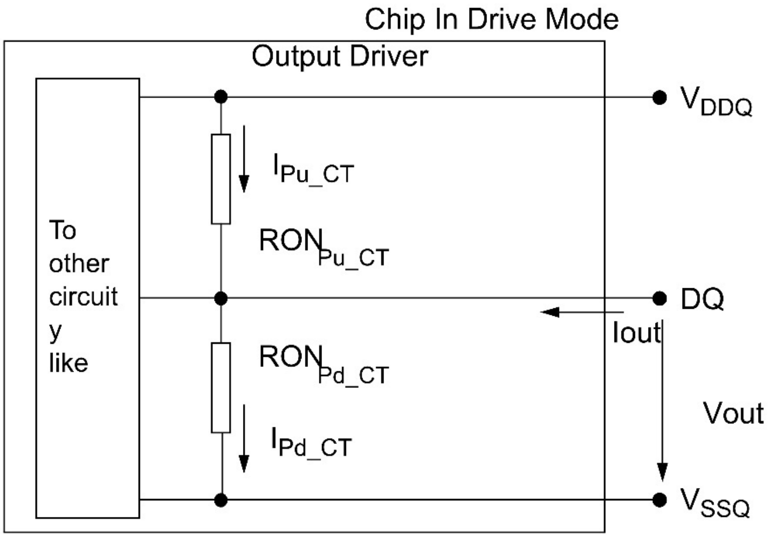
1. V_{DDQ} voltage is at V_{DDQ} DC. V_{DDQ} DC definition is TBD.

Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode.
The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ} - V_{OUT}}{|\,Iout\,|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|\,Iout\,|}$$



Output Driver

RONPu_CT and RONPd_CT

RON_{NOM_CT}	Resistor	Vout	Max.	Units	Notes
34Ω	RON_{Pd_CT}	$VOB_{dc} = 0.2 \times V_{DDQ}$	1.9	34Ω	1
		$VOL_{dc} = 0.5 \times V_{DDQ}$	2.0	34Ω	1
		$VOM_{dc} = 0.8 \times V_{DDQ}$	2.2	34Ω	1
		$VOH_{dc} = 1.1 \times V_{DDQ}$	2.5	34Ω	1
	RON_{Pu_CT}	$VOB_{dc} = 0.2 \times V_{DDQ}$	2.5	34Ω	1
		$VOL_{dc} = 0.5 \times V_{DDQ}$	2.2	34Ω	1
		$VOM_{dc} = 0.8 \times V_{DDQ}$	2.0	34Ω	1
		$VOH_{dc} = 1.1 \times V_{DDQ}$	1.9	34Ω	1

Notes:
1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-2666/3200	Units	Notes
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 – 0.15) x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.15 x V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

Differential AC & DC output levels

Symbol	Parameter	DDR4-2666/3200	Units	Notes
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.3 x V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

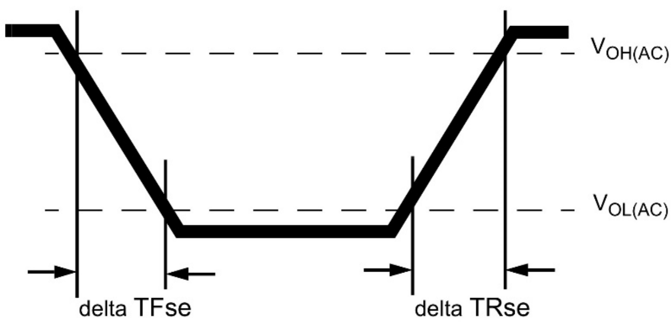
Single-ended Output Slew Rate

Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)]/ Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)]/ Delta TFse

Notes:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Single-ended Output Slew Rate Definition

Single-ended output slew rate

Parameter	Symbol	DDR4-2666/3200		Units
Single ended output slew rate	SRQse	4	9	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
Se: Single-ended Signals
For Ron = RZQ/7 setting

Notes:
1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
- Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
- Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies.

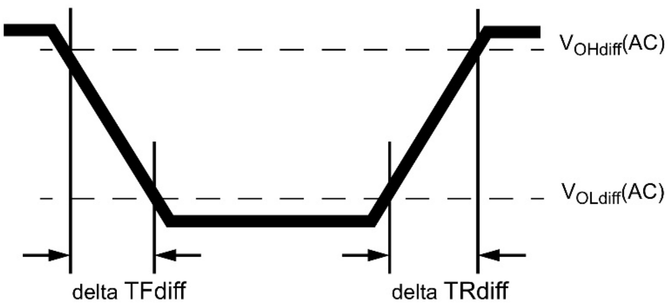
Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OLdiff}(AC) and V_{OHdiff}(AC) for differential signals as shown in Table and Figure of Differential output slew rate definition.

Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{Odiff}(AC)	V_{OHdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)]/ Delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)]/ Delta TFdiff

Notes:
1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate Definition

Differential output slew rate

Parameter	Symbol	DDR4-2666/3200		Units
		Min.	Max.	
Differential output slew rate	SRQdiff	8	18	V/ns

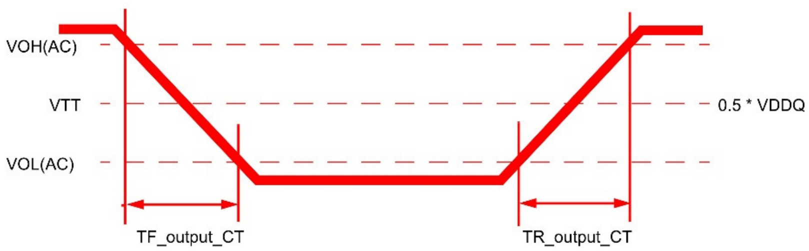
Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Symbol	Parameter	DDR4-2666/3200	Units	Notes
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OB}(DC)	DC output below measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	V_{TT} + (0.1 x V_{DDQ})	V	1
V_{OL}(AC)	AC output below measurement level (for output SR)	V_{TT} - (0.1 x V_{DDQ})	V	1

Notes:
1. The effective test load is 50Ω terminated by V_{TT} = 0.5 * V_{DDQ}



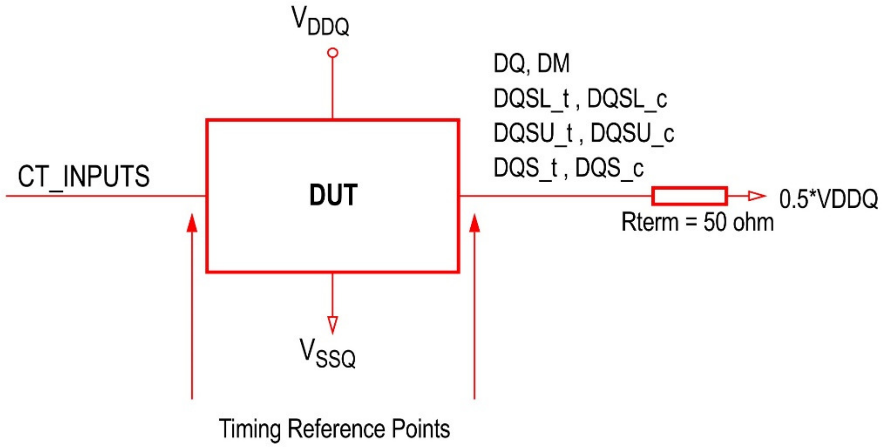
Output Slew Rate Definition of Connectivity Test Mode

Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-2666/3200		Units	Notes
		Min.	Max.		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure Connectivity Test Mode Timing Reference Load.



Connectivity Test Mode Timing Reference Load

I_{DD} Specification

Conditions	Symbol	Data rate (Mbps)	I_{DD} max X8	Unit
Operating One Bank Active-to-Precharge Current (AL=0); CKE: High; External clock: On; t_{CK}, nRC, nRAS, CL: see timing used table; BL: 8[1]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: V_{DDQ}; $\overline{DM}$: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,…; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD0}	3200 2666	99 84	mA
Operating One Bank Active-Read-Precharge Current (AL=0); CKE: High; External clock: On; t_{CK}, nRC, nRAS, CL: see timing used table; BL: 8[1]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; $\overline{DM}$: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,…; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD1}	3200 2666	114 102	mA
Precharge Standby Current (AL=0); CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: V_{DDQ}; $\overline{DM}$: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD2N}	3200 2666	65 55	mA
Precharge Standby ODT Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: V_{SSQ}; $\overline{DM}$: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: toggling	I_{DD2NT}	3200 2666	85 74	mA
Precharge Power-Down Current; CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: V_{DDQ}; $\overline{DM}$: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD2P}	3200 2666	29 29	mA
Precharge Quiet Standby Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: V_{DDQ}; $\overline{DM}$: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD2Q}	3200 2666	37 35	mA
Active Standby Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: V_{DDQ}; $\overline{DM}$: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD3N}	3200 2666	114 103	mA
Active Power-Down Current; CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: V_{DDQ}; $\overline{DM}$: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD3P}	3200 2666	70 64	mA
Operating Burst Read Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; $\overline{DM}$: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,…; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD4R}	3200 2666	212 189	mA

Conditions	Symbol	Data rate (Mbps)	I_{DD} max	Unit
			X8	
Operating Burst Write Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; $\overline{DM}$: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,…; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at High	I_{DD4W}	3200 2666	253 208	mA
Burst Refresh Current (1X REF); CKE: High; External clock: On; t_{CK}, CL, nRFC: see timing used table; BL: 8[1]; AL:0; $\overline{CS}$: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: V_{DDQ}; $\overline{DM}$: stable at 1; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD5B}	3200 2666	204 204	mA
Self Refresh Current: Normal Temperature Range; Tcase: 0-85°C; Low Power Auto Self Refresh (LP ASR): Normal[3]; CKE: Low; External clock: Off; CK and $\overline{CK}$: Low; CL: see timing used table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: Mid-level	I_{DD6N}	3200 2666	26 26	mA
Self Refresh Current: Extended Temperature Range; Tcase: 0-95°C; Low Power Auto Self Refresh (LP ASR): Extended[3]; CKE: Low; External clock: Off; CK and $\overline{CK}$: Low; CL: see timing used table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: Mid-level	I_{DD6E}	3200 2666	38 38	mA
Self Refresh Current: Reduced Temperature Range; Tcase: 0-45°C; Low Power Auto Self Refresh (LP ASR): Reduced[3]; CKE: Low; External clock: Off; CK and $\overline{CK}$: Low; CL: see timing used table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: Mid-level	I_{DD6R}	3200 2666	12 12	mA
Auto Self Refresh Current; Tcase: 0-95°C; Low Power Auto Self Refresh (LP ASR): Auto[3]; CKE: Low; External clock: Off; CK and $\overline{CK}$: Low; CL: see timing used table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$: stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: Mid-level	I_{DD6A}	3200 2666	38 38	mA
Operating Bank Interleave Read Current; CKE: High; External clock: On; t_{CK}, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8[1]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one; $\overline{DM}$: stable at 1; Bank Activity: two times interleaved cycling through banks (0,1,…7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	I_{DD7}	3200 2666	212 212	mA
Maximum Power-Down Current	I_{DD8}	3200 2666	23 22	mA

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0 = 00].
2. Output Buffer Enable
   - set MR1 [A12=0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
   RTT_NOM enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal Temperature range
   [A7:6 = 01] : Reduced Temperature range
   [A7:6 = 10] : Extended Temperature range
   [A7:6 = 11] : Auto Self Refresh

Timing used for I_{DD} and I_{DDQ} Measured – Loop Patterns

Symbol	DDR4-2666	DDR4-3200	Unit
	19-19-19	22-22-22	
t_{CK}	0.75	0.625	ns
CL	19	22	nCK
CWL	18	20	nCK
nRCD	19	22	nCK
nRC	62	74	nCK
nRAS	43	52	nCK
nRP	19	22	nCK
nFAW	28	34	nCK
nRRDS	4	4	nCK
nRRDL	7	8	nCK
t_{CCD_S}	4	4	nCK
t_{CCD_L}	7	8	nCK
t_{WTR_S}	4	4	nCK
t_{WTR_L}	10	12	nCK
nRFC 8Gb	467	560	nCK

DDR4-2666 Speed Bins

Speed Bin				- 075 (DDR4-2666)		Units	Notes
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	Min.	Max.		
Internal read command to first data			t_{AA}	14.25 (13.75)[5,10]	18.00	ns	9
Internal read command to first data with read DBI enabled			t_{AA_DBI}	t_{AA}(min) + 3nCK	t_{AA}(max) + 3nCK	ns	9
ACT to internal read or write delay time			t_{RCD}	14.25 (13.75)[5,10]	-	ns	9
PRE command period			t_{RP}	14.25 (13.75)[5,10]	-	ns	9
ACT to PRE command period			t_{RAS}	32	9 x t_{REFI}	ns	9
ACT to ACT or REF command time			t_{RC}	46.25 (45.75)[5,10]	-	ns	9
	Normal	Read DBI					
CWL=9	CL=9	CL=11	t_{CK}(AVG)	Reserved		ns	4
	CL=10	CL=12	t_{CK}(AVG)	1.5	1.6	ns	1,2,3,6,8
CWL=9,11	CL=10	CL=12	t_{CK}(AVG)	Reserved		ns	4
	CL=11	CL=13	t_{CK}(AVG)	1.25	<1.5	ns	1,2,3,6
				(Optional)[5,10]			
	CL=12	CL=14	t_{CK}(AVG)	1.25	<1.5	ns	1,2,3,6
CWL=10,12	CL=12	CL=14	t_{CK}(AVG)	Reserved		ns	4
	CL=13	CL=15	t_{CK}(AVG)	1.071	<1.25	ns	1,2,3,6
				(Optional)[5,10]			
	CL=14	CL=16	t_{CK}(AVG)	1.071	<1.25	ns	1,2,3,6
CWL=11,14	CL=14	CL=17	t_{CK}(AVG)	Reserved		ns	4
	CL=15	CL=18	t_{CK}(AVG)	0.937	<1.071	ns	1,2,3,6
				(Optional)[5,10]			
	CL=16	CL=19	t_{CK}(AVG)	0.937	<1.071	ns	1,2,3,6
CWL=12,16	CL=15	CL=18	t_{CK}(AVG)	Reserved		ns	4
	CL=16	CL=19	t_{CK}(AVG)	Reserved		ns	4
	CL=17	CL=20	t_{CK}(AVG)	0.833	<0.937	ns	1,2,3,6
				(Optional)[5,10]			1,2,3,6
	CL=18	CL=21	t_{CK}(AVG)	0.833	<0.937	ns	1,2,3,6
CWL=14,18	CL=17	CL=20	t_{CK}(AVG)	Reserved		ns	4
	CL=18	CL=21	t_{CK}(AVG)	Reserved		ns	4
	CL=19	CL=22	t_{CK}(AVG)	0.75	<0.833	ns	1,2,3
	CL=20	CL=23	t_{CK}(AVG)	0.75	<0.833	ns	1,2,3
Supported CL setting				10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20		nCK	10
Supported CWL setting				9, 10, 11, 12, 14, 16, 18		nCK	

DDR4-3200 Speed Bins

Speed Bin				- 062 (DDR4-3200)		Units	Notes
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	Min.	Max.		
Internal read command to first data			t_{AA}	13.75	18.00	ns	9
Internal read command to first data with read DBI enabled			t_{AA_DBI}	t_{AA}(min) + 4nCK	t_{AA}(max) + 4nCK	ns	9
ACT to internal read or write delay time			t_{RCD}	13.75	-	ns	9
PRE command period			t_{RP}	13.75	-	ns	9
ACT to PRE command period			t_{RAS}	32	9 x t_{REFI}	ns	9
ACT to ACT or REF command time			t_{RC}	45.75	-	ns	9
	Normal	Read DBI					
CWL=9	CL=9	CL=11	t_{CK}(AVG)	Reserved		ns	4
	CL=10	CL=12	t_{CK}(AVG)	1.5	1.6	ns	1,2,3,7,8
CWL=9,11	CL=10	CL=12	t_{CK}(AVG)	Reserved		ns	4
	CL=11	CL=13	t_{CK}(AVG)	1.25	<1.5	ns	1,2,3,7
	CL=12	CL=14	t_{CK}(AVG)	1.25	<1.5	ns	1,2,3,7
CWL=10,12	CL=12	CL=14	t_{CK}(AVG)	Reserved		ns	4
	CL=13	CL=15	t_{CK}(AVG)	1.071	<1.25	ns	1,2,3,7
	CL=14	CL=16	t_{CK}(AVG)	1.071	<1.25	ns	1,2,3,7
CWL=11,14	CL=14	CL=17	t_{CK}(AVG)	Reserved		ns	4
	CL=15	CL=18	t_{CK}(AVG)	0.937	<1.071	ns	1,2,3,7
	CL=16	CL=19	t_{CK}(AVG)	0.937	<1.071	ns	1,2,3,7
CWL=12,16	CL=15	CL=18	t_{CK}(AVG)	Reserved		ns	4
	CL=16	CL=19	t_{CK}(AVG)	Reserved		ns	4
	CL=17	CL=20	t_{CK}(AVG)	0.833	<0.937	ns	1,2,3,7
	CL=18	CL=21	t_{CK}(AVG)	0.833	<0.937	ns	1,2,3,7
CWL=14,18	CL=17	CL=20	t_{CK}(AVG)	Reserved		ns	4
	CL=18	CL=21	t_{CK}(AVG)	Reserved		ns	4
	CL=19	CL=22	t_{CK}(AVG)	0.75	<0.833	ns	1,2,3,7
	CL=20	CL=23	t_{CK}(AVG)	0.75	<0.833	ns	1,2,3,7
CWL=16,20	CL=20	CL=24	t_{CK}(AVG)	Reserved		ns	4
	CL=21	CL=25	t_{CK}(AVG)	0.682	<0.75	ns	1,2,3,7
	CL=22	CL=26	t_{CK}(AVG)	0.682	<0.75	ns	1,2,3,7
	CL=24	CL=28	t_{CK}(AVG)	0.682	<0.75	ns	1,2,3,7
CWL=16,20	CL=20	CL=24	t_{CK}(AVG)	Reserved		ns	4
	CL=22	CL=26	t_{CK}(AVG)	0.625	<0.682	ns	1,2,3
	CL=24	CL=28	t_{CK}(AVG)	0.625	<0.682	ns	1,2,3
Supported CL setting				10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24		nCK	
Supported CWL setting				9, 10, 11, 12, 14, 16, 18, 20		nCK	

Speed Bin Table Note

Absoulte Specification
- V_{DDQ} = V_{DD} = 1.20V ± 0.06V
- V_{PP} = 2.5V +0.25/-0.125V
-The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in t_{CK}(avg).MIN and t_{CK}(avg).MAX requirements. When making a selection of t_{CK}(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. t_{CK}(avg).MIN limits: Since CAS Latency is not purely analog – data and strobe output are synchronized by the DLL – all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm.
3. t_{CK}(avg).MAX limits: Calculate t_{CK}(avg) = t_{AA}.MAX / CL SELECTED and round the resulting t_{CK}(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.701ns or 0.937ns or 0.833ns). This result is t_{CK}(avg).MAX corresponding to CL SELECTED.
4. ‘Reserved‘ settings are not allowed. User must program a different value.
5. ‘Optional‘ settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier’s data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
9. Parameters apply from t_{CK}(avg)min to t_{CK}(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
10. CL number in parentheses, it means that these numbers are optional.

AC Characteristics

Parameter	Symbol	- 075 (DDR4-2666)		Units	Notes
		Min.	Max.		
Minimum Clock Cycle Time (DLL off mode)	t_{CK} (DLL_OFF)	8	20	ns	
Average Clock Period	t_{CK}(avg)	0.750	<0.833	ns	35,36
Average high pulse width	t_{CH}(avg)	0.48	0.52	t_{CK}(avg)	
Average low pulse width	t_{CL}(avg)	0.48	0.52	t_{CK}(avg)	
Absolute Clock Period	t_{CK}(abs)	t_{CK}(avg)min + T_{jit}(per)min_tot	t_{CK}(avg)max + T_{jit}(per)max_tot	t_{CK}(avg)	
Absolute clock HIGH pulse width	t_{CH}(abs)	0.45	-	t_{CK}(avg)	23
Absolute clock LOW pulse width	t_{CL}(abs)	0.45	-	t_{CK}(avg)	24
Clock Period Jitter – total	JIT(per)_tot	-38	38	ps	25
Clock Period Jitter – deterministic	JIT(per)_dj	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per,lck)	-30	30	ps	
Cycle to Cycle Period Jitter	t_{JIT}(cc)	-	75	ps	
Cycle to Cycle Period Jitter during DLL locking period	t_{JIT}(cc,lck)	-	60	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-55	55	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-66	66	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-73	73	ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-78	78	ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-83	83	ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-87	87	ps	
Cumulative error across 8 cycles	t_{ERR}(8per)	-91	91	ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-94	94	ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-96	96	ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-99	99	ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-101	101	ps	
Cumulative error across 13 cycles	t_{ERR}(13per)	-103	103	ps	
Cumulative error across 14 cycles	t_{ERR}(14per)	-104	104	ps	
Cumulative error across 15 cycles	t_{ERR}(15per)	-106	106	ps	
Cumulative error across 16 cycles	t_{ERR}(16per)	-108	108	ps	

Parameter	Symbol	- 075 (DDR4-2666)		Units	Notes
		Min.	Max.		
Cumulative error across 17 cycles	t_{ERR}(17per)	-110	110	ps	
Cumulative error across 18 cycles	t_{ERR}(18per)	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	t_{ERR}(nper)	t_{ERR}(nper)min = ((1 + 0.68ln(n)) * t_{JIT}(per)_total min) t_{ERR}(nper)max = ((1 + 0.68ln(n)) * t_{JIT}(per)_total max)		ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{ih}(ac) / V_{il}(ac) levels	t_{IS}(base)	55	-	ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{ref} levels	$t_{IS}(V_{ref})$	145	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to V_{ih}(dc) / V_{il}(dc) levels	t_{IH}(base)	80	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to V_{ref} levels	t_{IH}(Vref)	145	-	ps	
Control and Address Input pulse width for each input	t_{IPW}	385	-	ps	
Command and Address Timing					
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	t_{CCD_L}	max(5nCK,5ns)	-	nCK	34
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	t_{CCD_S}	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	t_{RRD_S}(2K)	max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	t_{RRD_S}(1K)	max(4nCK,3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	t_{RRD_S}(1/2K)	max(4nCK,3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	t_{RRD_L}(2K)	max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	t_{RRD_L}(1K)	max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	t_{RRD_L}(1/2K)	max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	t_{FAW}_2K	max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	t_{FAW}_1K	max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	t_{FAW}_1/2K	max(16nCK,12ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	t_{WTR_S}	max(2nCK,2.5ns)	-	ns	1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	t_{WTR_L}	max(4nCK,7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	t_{RTP}	max(4nCK,7.5ns)	-		34
WRITE recovery time	t_{WR}	15	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR} + max(5nCK,3.75ns)	-	ns	1,28

Parameter	Symbol	- 075 (DDR4-2666)		Units	Notes
		Min.	Max.		
Delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S} + max (5nCK,3.75ns)	-	ns	2,29, 34
Delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L} + max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	t_{DLLK}	1024	-	nCK	
Mode Register Set command cycle time	t_{MRD}	8	-	nCK	
Mode Register Set command update delay	t_{MOD}	max(24nCK,15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	nCK	33
Multi-Purpose Register Write Recovery Time	t_{WR_MPR}	t_{MOD}(min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	t_{DAL}(min)	Programmed WR + roundup (t_{RP} / t_{CK}(avg))		nCK	
DQ0 or DQL0 driven to 0 setup time to first DQS rising edge	t_{PDA_S}	0.5	-		45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	t_{PDA_H}	0.5	-		46,47
CS_n to Command Address Latency					
$\overline{CS}$ to Command Address Latency	t_{CAL}	max(3nCK,3.748ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	$t_{MRD\_}t_{CAL}$	t_{MOD} + t_{CAL}	-	nCK	
Mode Register Set update delay in CAL mode	$t_{MOD\_}t_{CAL}$	t_{MOD} + t_{CAL}	-	nCK	
DRAM Data Timing					
DQS, $\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	0.18	t_{CK}(avg) /2	13,18, 39,49
DQ output hold time per group, per access from DQS, $\overline{DQS}$	t_{QH}	0.74	-	t_{CK}(avg) /2	13,17, 18,39, 49
Data Valid Window per device per UI: (t_{QH} - t_{DQSQ}) of each UI on a given DRAM	t_{DVWd}	0.64	-	UI	17,18, 39,49
Data Valid Window per pin per UI: (t_{QH} - t_{DQSQ}) each UI on a pin of a given DRAM	t_{DVWp}	0.72	-	UI	17,18, 39,49
DQ low impedance time from CK, $\overline{CK}$	t_{LZ}(DQ)	-310	170	ps	39
DQ high impedance time from CK, $\overline{CK}$	t_{HZ}(DQ)	-	170	ps	39
Data Strobe Timing					
DQS, $\overline{DQS}$ differential READ Preamble (1 clock preamble)	t_{RPRE}	0.9	NOTE 44	t_{CK}	39,40
DQS, $\overline{DQS}$ differential READ Preamble (2 clock preamble)	t_{RPRE2}	1.8	NOTE 44	t_{CK}	39,41

Parameter	Symbol	- 075 (DDR4-2666)		Units	Notes
		Min.	Max.		
DQS, $\overline{DQS}$ differential READ Postamble	t_{RPST}	0.33	NOTE 45	t_{CK}	39
DQS, $\overline{DQS}$ differential output high time	t_{QSH}	0.4	-	t_{CK}	21,39
DQS, $\overline{DQS}$ differential output low time	t_{QSL}	0.4	-	t_{CK}	20,39
DQS, $\overline{DQS}$ differential WRITE Preamble (1 clock preamble)	t_{WPRE}	0.9	-	t_{CK}	42
DQS, $\overline{DQS}$ differential WRITE Preamble (2 clock preamble)	t_{WPRE2}	1.8	-	t_{CK}	43
DQS, $\overline{DQS}$ differential WRITE Postamble	t_{WPST}	0.33	-	t_{CK}	
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	t_{LZ}(DQS)	-310	170	ps	39
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	t_{HZ}(DQS)	-	170	ps	39
DQS, $\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.46	0.54	t_{CK}	
DQS, $\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.46	0.54	t_{CK}	
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	t_{CK}	42
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge (2 clock preamble)	t_{DQSS2}	-0.50	0.50	t_{CK}	43
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	t_{DSS}	0.18	-	t_{CK}	
DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge	t_{DSH}	0.18	-	t_{CK}	
DQS, $\overline{DQS}$ rising edge output timing location from rising CK, $\overline{CK}$ with DLL On mode	t_{DQSCK} (DLL On)	-170	170	ps	37,38, 39
DQS, $\overline{DQS}$ rising edge output variance window per DRAM	t_{DQSCKI} (DLL On)	-	270	ps	37,38, 39
MPSM Timing					
Command path disable delay upon MPSM entry	t_{MPED}	t_{MOD}(min) + t_{CPDED}(min)	-		
Valid clock requirement after MPSM entry	t_{CKMPE}	t_{MOD}(min) + t_{CPDED}(min)	-		
Valid clock requirement before MPSM exit	t_{CKMPX}	t_{CKSRX}(min)	-		
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	t_{XS}(min)	-		
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	t_{XMP}(min) + t_{XSDLL}(min)	-		
CS setup time to CKE	t_{MPX_S}	t_{IS}(min) + t_{IH}(min)	-		
Calibration Timing					
Power-up and RESET calibration time	t_{ZQinit}	1024	-	nCK	

Parameter	Symbol	- 075 (DDR4-2666)		Units	Notes
		Min.	Max.		
Normal operation Full calibration time	t_{ZQoper}	512	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	128	-	nCK	
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	t_{XPR}	max(5nCK,t_{RFC}(min) + 10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min) + 10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	t_{XS_ABORT} (min)	t_{RFC4}(min) + 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	t_{XS_FAST} (min)	t_{RFC4}(min) + 10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) + 1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	t_{CKE}(min) + 1nCK + PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	max(5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) when CA Parity is enabled	t_{CKSRE_PAR}	max(5nCK,10ns) + PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	max(5nCK,10ns)	-	nCK	
Power Down Timing					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max(4nCK,6ns)	-	nCK	
CKE minimum pulse width	t_{CKE}	max(3nCK,5ns)	-	nCK	31,32
Command pass disable delay	t_{CPDED}	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	9*t_{REFI}		6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4+(t_{WR} / t_{CK}(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	nCK	5

Parameter	Symbol	- 075 (DDR4-2666)		Units	Notes
		Min.	Max.		
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPBC4DEN}$	WL + 2 + (t_{WR} / t_{CK}(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL + 2 + WR + 1	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	2	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MOD}(min)	-	nCK	
PDA Timing					
Mode Register Set command cycle time in PDA mode	t_{MRD_PDA}	max(16nCK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	t_{MOD_PDA}	t_{MOD}		nCK	
ODT Timing					
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1.0	9.0	ns	
RTT dynamic change skew	t_{ADC}	0.28	0.72	t_{CK}(avg)	
Write Leveling Timing					
First DQS, $\overline{DQS}$ rising edge after write leveling mode is promgrammed	t_{WLMRD}	40	-	nCK	12
DQS, $\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	nCK	12
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	0.13	-	t_{CK}(avg)	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	0.13	-	t_{CK}(avg)	
Write leveling output delay	t_{WLO}	0	9.5	ns	
Write leveling output error	t_{WLOE}	0	2	ns	
CA Parity Timing					
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	nCK	
Delay from errant command to $\overline{ALERT}$ assertion	$t_{PAR\_ALERT\_ON}$	-	PL + 6ns	nCK	
Pulse width of $\overline{ALERT}$ signal when asserted	$t_{PAR\_ALERT\_PW}$	80	160	nCK	
Timing from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	71	nCK	
Parity Latency	PL	5		nCK	
CRC Error Reporting					

Parameter	Symbol	- 075 (DDR4-2666)		Units	Notes
		Min.	Max.		
CRC error to $\overline{\text{ALERT}}$ laterncy	t_{CRC_ALERT}	3	13	ns	
CRC $\overline{\text{ALERT}}$ pulse width	CRC_ ALERT_PW	6	10	nCK	
Geardown Timing					
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	t_{XPR}	-		
CKE High Assert to Gear Down Enable time (T2/CKE)	t_{XS_GEAR}	t_{XS}	-		
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	t_{MOD} + 4nCK	-		27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	t_{MOD}	-		27
Geardown setup time	t_{GEAR_setup}	2	-	nCK	
Geardown hold time	t_{GEAR_hold}	2	-	nCK	
t_{REFI}					
t_{RFC1} (min)	8Gb	350	-	ns	34
t_{RFC2} (min)	8Gb	260	-	ns	34
t_{RFC4} (min)	8Gb	160	-	ns	34

Parameter	Symbol	- 062 (DDR4-3200)		Units	Notes
		Min.	Max.		
Minimum Clock Cycle Time (DLL off mode)	t_{CK} (DLL_OFF)	8	20	ns	
Average Clock Period	t_{CK}(avg)	0.625	<0.682	ns	35,36
Average high pulse width	t_{CH}(avg)	0.48	0.52	t_{CK}(avg)	
Average low pulse width	t_{CL}(avg)	0.48	0.52	t_{CK}(avg)	
Absolute Clock Period	t_{CK}(abs)	t_{CK}(avg)min + T_{jit}(per)min_tot	t_{CK}(avg)max + T_{jit}(per)max_tot	t_{CK}(avg)	
Absolute clock HIGH pulse width	t_{CH}(abs)	0.45	-	t_{CK}(avg)	23
Absolute clock LOW pulse width	t_{CL}(abs)	0.45	-	t_{CK}(avg)	24
Clock Period Jitter – total	JIT(per)_tot	-32	32	ps	25
Clock Period Jitter – deterministic	JIT(per)_dj	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per,lck)	-25	25	ps	
Cycle to Cycle Period Jitter	t_{JIT}(cc)	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	t_{JIT}(cc,lck)	-	50	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-46	46	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-55	55	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-61	61	ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-65	65	ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-69	69	ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-73	73	ps	
Cumulative error across 8 cycles	t_{ERR}(8per)	-76	76	ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-78	78	ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-80	80	ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-83	83	ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-84	84	ps	
Cumulative error across 13 cycles	t_{ERR}(13per)	-86	86	ps	
Cumulative error across 14 cycles	t_{ERR}(14per)	-87	87	ps	
Cumulative error across 15 cycles	t_{ERR}(15per)	-89	89	ps	
Cumulative error across 16 cycles	t_{ERR}(16per)	-90	90	ps	

Parameter	Symbol	- 062 (DDR4-3200)		Units	Notes
		Min.	Max.		
Cumulative error across 17 cycles	t_{ERR}(17per)	-92	92	ps	
Cumulative error across 18 cycles	t_{ERR}(18per)	-93	93	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	t_{ERR}(nper)	t_{ERR}(nper)min = ((1 + 0.68ln(n)) * t_{JIT}(per)_total min) t_{ERR}(nper)max = ((1 + 0.68ln(n)) * t_{JIT}(per)_total max)		ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{ih}(ac) / V_{il}(ac) levels	t_{IS}(base)	40	-	ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{ref} levels	$t_{IS}(V_{ref})$	130	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to V_{ih}(dc) / V_{il}(dc) levels	t_{IH}(base)	65	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to V_{ref} levels	t_{IH}(Vref)	130	-	ps	
Control and Address Input pulse width for each input	t_{IPW}	340	-	ps	
Command and Address Timing					
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	t_{CCD_L}	max(5nCK,5ns)	-	nCK	34
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	t_{CCD_S}	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	t_{RRD_S}(2K)	max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	t_{RRD_S}(1K)	max(4nCK,2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	t_{RRD_S}(1/2K)	max(4nCK,2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	t_{RRD_L}(2K)	max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	t_{RRD_L}(1K)	max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	t_{RRD_L}(1/2K)	max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	t_{FAW}_2K	max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	t_{FAW}_1K	max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	t_{FAW}_1/2K	max(16nCK,10ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	t_{WTR_S}	max(2nCK,2.5ns)	-	ns	1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	t_{WTR_L}	max(4nCK,7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	t_{RTP}	max(4nCK,7.5ns)	-		34
WRITE recovery time	t_{WR}	15	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR} + max(5nCK,3.75ns)	-	ns	1,28

Parameter	Symbol	- 062 (DDR4-3200)		Units	Notes
		Min.	Max.		
Delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S} + max (5nCK,3.75ns)	-	ns	2,29, 34
Delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L} + max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	t_{DLLK}	1024	-	nCK	
Mode Register Set command cycle time	t_{MRD}	8	-	nCK	
Mode Register Set command update delay	t_{MOD}	max(24nCK,15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	nCK	33
Multi-Purpose Register Write Recovery Time	t_{WR_MPR}	t_{MOD}(min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	t_{DAL}(min)	Programmed WR + roundup (t_{RP} / t_{CK}(avg))		nCK	
DQ0 or DQL0 driven to 0 setup time to first DQS rising edge	t_{PDA_S}	0.5	-		45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	t_{PDA_H}	0.5	-		46,47
CS_n to Command Address Latency					
$\overline{CS}$ to Command Address Latency	t_{CAL}	max(3nCK,3.748ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	t_{MRD_tCAL}	t_{MOD} + t_{CAL}	-	nCK	
Mode Register Set update delay in CAL mode	t_{MOD_tCAL}	t_{MOD} + t_{CAL}	-	nCK	
DRAM Data Timing					
DQS, $\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	0.20	t_{CK}(avg) /2	13,18, 39,49
DQ output hold time per group, per access from DQS, $\overline{DQS}$	t_{QH}	0.70	-	t_{CK}(avg) /2	13,17, 18,39, 49
Data Valid Window per device per UI: (t_{QH} - t_{DQSQ}) of each UI on a given DRAM	t_{DVWd}	0.64	-	UI	17,18, 39,49
Data Valid Window per pin per UI: (t_{QH} - t_{DQSQ}) each UI on a pin of a given DRAM	t_{DVWp}	0.72	-	UI	17,18, 39,49
DQ low impedance time from CK, $\overline{CK}$	t_{LZ}(DQ)	-250	160	ps	39
DQ high impedance time from CK, $\overline{CK}$	t_{HZ}(DQ)	-	160	ps	39
Data Strobe Timing					
DQS, $\overline{DQS}$ differential READ Preamble (1 clock preamble)	t_{RPRE}	0.9	NOTE 44	t_{CK}	39,40
DQS, $\overline{DQS}$ differential READ Preamble (2 clock preamble)	t_{RPRE2}	1.8	NOTE 44	t_{CK}	39,41

Parameter	Symbol	- 062 (DDR4-3200)		Units	Notes
		Min.	Max.		
DQS, $\overline{DQS}$ differential READ Postamble	t_{RPST}	0.33	NOTE 45	t_{CK}	39
DQS, $\overline{DQS}$ differential output high time	t_{QSH}	0.4	-	t_{CK}	21,39
DQS, $\overline{DQS}$ differential output low time	t_{QSL}	0.4	-	t_{CK}	20,39
DQS, $\overline{DQS}$ differential WRITE Preamble (1 clock preamble)	t_{WPRE}	0.9	-	t_{CK}	42
DQS, $\overline{DQS}$ differential WRITE Preamble (2 clock preamble)	t_{WPRE2}	1.8	-	t_{CK}	43
DQS, $\overline{DQS}$ differential WRITE Postamble	t_{WPST}	0.33	-	t_{CK}	
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	t_{LZ}(DQS)	-250	160	ps	39
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	t_{HZ}(DQS)	-	160	ps	39
DQS, $\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.46	0.54	t_{CK}	
DQS, $\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.46	0.54	t_{CK}	
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	t_{CK}	42
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge (2 clock preamble)	t_{DQSS2}	-0.50	0.50	t_{CK}	43
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	t_{DSS}	0.18	-	t_{CK}	
DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge	t_{DSH}	0.18	-	t_{CK}	
DQS, $\overline{DQS}$ rising edge output timing location from rising CK, $\overline{CK}$ with DLL On mode	t_{DQSCK} (DLL On)	-160	160	ps	37,38, 39
DQS, $\overline{DQS}$ rising edge output variance window per DRAM	t_{DQSCKI} (DLL On)	-	260	ps	37,38, 39
MPSM Timing					
Command path disable delay upon MPSM entry	t_{MPED}	t_{MOD}(min) + t_{CPDED}(min)	-		
Valid clock requirement after MPSM entry	t_{CKMPE}	t_{MOD}(min) + t_{CPDED}(min)	-		
Valid clock requirement before MPSM exit	t_{CKMPX}	t_{CKSRX}(min)	-		
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	t_{XS}(min)	-		
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	t_{XMP}(min) + t_{XSDLL}(min)	-		
CS setup time to CKE	t_{MPX_S}	t_{IS}(min) + t_{IH}(min)	-		
Calibration Timing					
Power-up and RESET calibration time	t_{ZQinit}	1024	-	nCK	

Parameter	Symbol	- 062 (DDR4-3200)		Units	Notes
		Min.	Max.		
Normal operation Full calibration time	t_{ZQoper}	512	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	128	-	nCK	
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	t_{XPR}	max(5nCK,t_{RFC}(min) + 10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min) + 10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	t_{XS_ABORT} (min)	t_{RFC4}(min) + 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	t_{XS_FAST} (min)	t_{RFC4}(min) + 10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) + 1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	t_{CKE}(min) + 1nCK + PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	max(5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) when CA Parity is enabled	t_{CKSRE_PAR}	max(5nCK,10ns) + PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	max(5nCK,10ns)	-	nCK	
Power Down Timing					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max(4nCK,6ns)	-	nCK	
CKE minimum pulse width	t_{CKE}	max(3nCK,5ns)	-	nCK	31,32
Command pass disable delay	t_{CPDED}	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	9*t_{REFI}		6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4+(t_{WR} / t_{CK}(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPBC4DEN}$	WL + 2 + (t_{WR} / t_{CK}(avg))	-	nCK	4

Parameter	Symbol	- 062 (DDR4-3200)		Units	Notes
		Min.	Max.		
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL + 2 + WR + 1	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	2	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MOD}(min)	-	nCK	
PDA Timing					
Mode Register Set command cycle time in PDA mode	t_{MRD_PDA}	max(16nCK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	t_{MOD_PDA}	t_{MOD}		nCK	
ODT Timing					
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1.0	9.0	ns	
RTT dynamic change skew	t_{ADC}	0.26	0.74	t_{CK}(avg)	
Write Leveling Timing					
First DQS, $\overline{DQS}$ rising edge after write leveling mode is promgrammed	t_{WLMRD}	40	-	nCK	12
DQS, $\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	nCK	12
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	0.13	-	t_{CK}(avg)	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	0.13	-	t_{CK}(avg)	
Write leveling output delay	t_{WLO}	0	9.5	ns	
Write leveling output error	t_{WLOE}	0	2	ns	
CA Parity Timing					
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	nCK	
Delay from errant command to $\overline{ALERT}$ assertion	$t_{PAR\_ALERT\_ON}$	-	PL + 6ns	nCK	
Pulse width of $\overline{ALERT}$ signal when asserted	$t_{PAR\_ALERT\_PW}$	96	192	nCK	
Timing from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	85	nCK	
Parity Latency	PL	6		nCK	
CRC Error Reporting					
CRC error to $\overline{ALERT}$ laterncy	t_{CRC_ALERT}	3	13	ns	

Parameter	Symbol	- 062 (DDR4-3200)		Units	Notes
		Min.	Max.		
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	nCK	
Geardown Timing					
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	t_{XPR}	-		
CKE High Assert to Gear Down Enable time (T2/CKE)	t_{XS_GEAR}	t_{XS}	-		
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	t_{MOD} + 4nCK	-		27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	t_{MOD}	-		27
Geardown setup time	t_{GEAR_setup}	2	-	nCK	
Geardown hold time	t_{GEAR_hold}	2	-	nCK	
t_{REFI}					
t_{RFC1} (min)	8Gb	350	-	ns	34
t_{RFC2} (min)	8Gb	260	-	ns	34
t_{RFC4} (min)	8Gb	160	-	ns	34

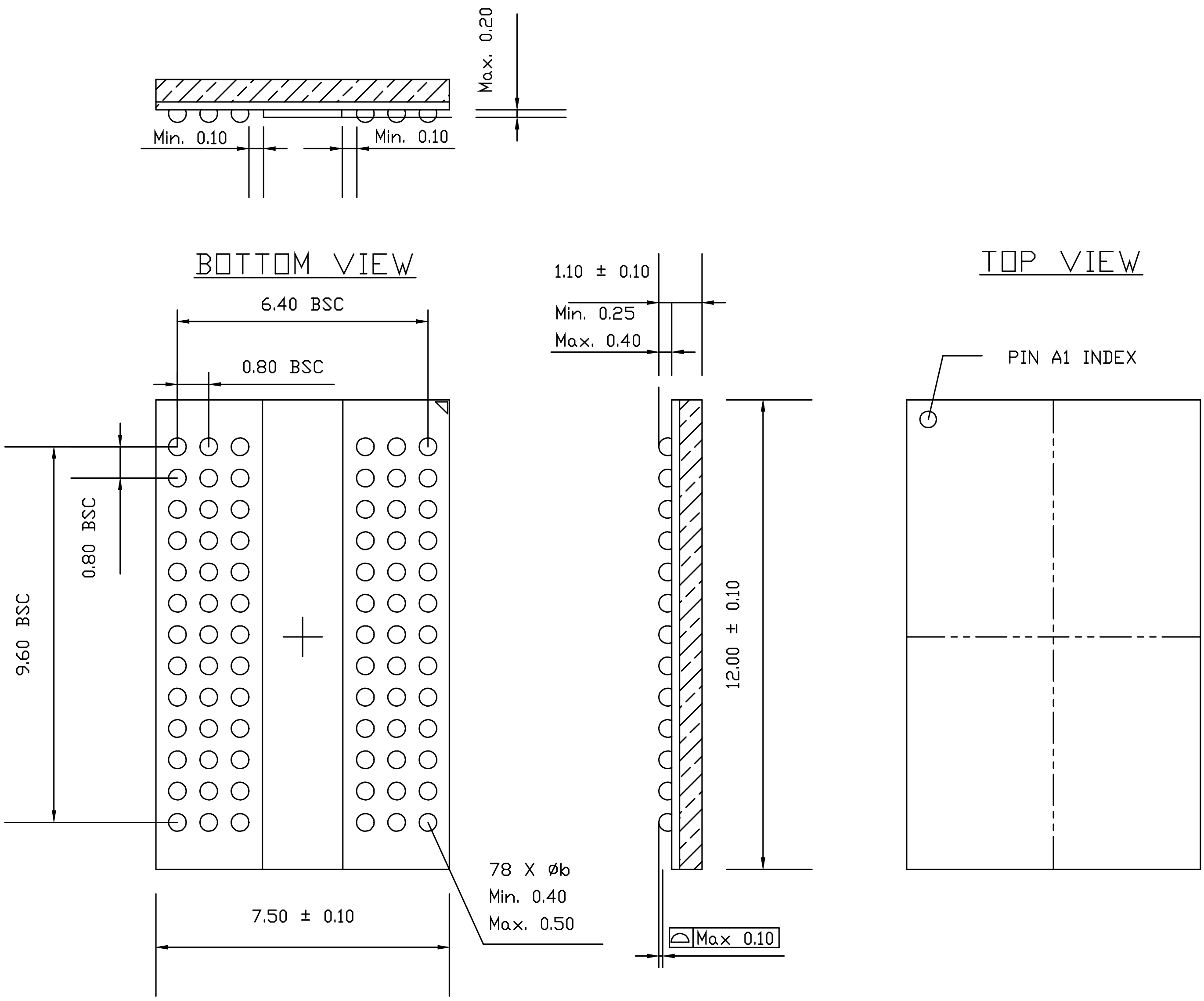
Notes for AC Electrical Characteristics

1. Start of internal write transaction is defined as follows:
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}/t_{CK} following rounding algorithm.
5. WR in clock cycles as programmed in MR0.
6. t_{REFI} depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down.
8. For these parameters, the DDR4 SDRAM device supports t_{nPARAM}[nCK]=RU{t_{PARAM}[ns]/t_{CK}(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.
10. When CRC and DM are both enabled, $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.
11. When CRC and DM are both enabled, $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual t_{jit}(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 DRAM only.
20. t_{QSL} describes the instantaneous differential output low pulse width on DQS –$\overline{DQS}$, as measured from on falling edge to the next consecutive rising edge.
21. t_{QSH} describes the instantaneous differential output high pulse width on DQS –$\overline{DQS}$, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval t_{REFI}.
23. t_{CH}(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. t_{CL}(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks.
28. When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.
29. When CRC and DM are both enabled, $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.
30. When CRC and DM are both enabled, $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for t_{CKE} specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for t_{CKE} specification (High pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from t_{CK}(avg)min to t_{CK}(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed Bin Tables.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=t_{CK}(avg).min/2
37. Applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RONNOM = 34 ohms.
40. 1t_{CK} toggle mode with setting MR4:A11 to 0.
41. 2t_{CK} toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2666/3200 speed grade.
42. 1t_{CK} mode with setting MR4:A12 to 0.
43. 2t_{CK} mode with setting MR4:A12 to 1, which is valid for DDR4-2666/3200 speed grade.
44. The maximum read preamble is bounded by t_{LZ}(DQS)min on the left side and t_{DQSCK}(max) on the right side. Boundary of DQS Low-Z occur one cycle earlier in 2t_{CK} toggle mode.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.

46. Last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High.
47. V_{refDQ} value must be set to either its midpoint or V_{cent_DQ}(midpoint) in order to capture DQ or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by t_{DQSCK}(min) plus t_{QSH}(min) on the left side and t_{HZ}(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7*V_{DDQ} as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to V_{TT} = V_{DDQ}.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

Package Diagram (x8)

78-Ball Fine Pitch Ball Grid Array Outline



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Revision History

Rev	History	Release Date	Remarks
1.0	Formal release	Jun. 2022	