IM4G(04/08)D3FDB
4Gbit DDR3 SDRAM
8 BANKS X 128Mbit X 4
8 BANKS X 64Mbit X 8

Ordering Speed Code	-107	-093
	DDR3-1866	DDR3-2133
Clock Cycle Time (t_{CK5}, CWL=5)	3.0ns	3.0ns
Clock Cycle Time (t_{CK6}, CWL=5)	2.5 ns	2.5 ns
Clock Cycle Time (t_{CK7}, CWL=6)	1.875 ns	1.875 ns
Clock Cycle Time (t_{CK8}, CWL=6)	1.875 ns	1.875 ns
Clock Cycle Time (t_{CK9}, CWL=7)	1.5 ns	1.5 ns
Clock Cycle Time (t_{CK10}, CWL=7)	1.5 ns	1.5 ns
Clock Cycle Time (t_{CK11}, CWL=8)	1.25 ns	1.25 ns
Clock Cycle Time (t_{CK13}, CWL=9)	1.07 ns	1.07 ns
Clock Cycle Time (t_{CK14}, CWL=10)	-	0.938 ns
System Frequency ($f_{ck\ max}$)	933 MHz	1066 MHz

Specifications

- Density: 4Gbits
- Organization:
  - 128M words x 4 bits x 8 banks (IM4G04D3FDB)
  - 64M words x 8 bits x 8 banks (IM4G08D3FDB)
- Package:
  - 78-ball FBGA for x4/x8
  - Lead-free (RoHS complaint) and Halogen-free
- Power supply: V_{DD}, V_{DDQ} = 1.35V (1.283V to 1.45V)
  - Backward compatible to V_{DD}, V_{DDQ} = 1.5V ± 0.075V
- Data rate: 1866Mbps/2133Mbps
- 1KB page size for x4/x8
  - Row address: A0 to A15
  - Column address: A0 to A9, A11 (IM4G04D3FDB)
  - Column address: A0 to A9 (IM4G08D3FDB)
- Eight internal banks for concurrent operation
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT)
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- $\overline{\text{CAS}}$ Latency (CL): 5, 6, 7, 8, 9 ,10, 11, 12, 13, 14
- $\overline{\text{CAS}}$ Write Latency (CWL): 5, 6, 7, 8, 9, 10
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Refresh: auto-refresh, self-refresh
- Refresh cycles:
  - Average refresh period
    7.8 µs at 0°C ≤ Tcase ≤ +85°C
    3.9 µs at +85°C < Tcase ≤ +105°C
- Operating case temperature range
  - Commercial: 0 °C ≤ Tcase ≤ +95°C
  - Industrial: -40 °C ≤ Tcase ≤ +95°C

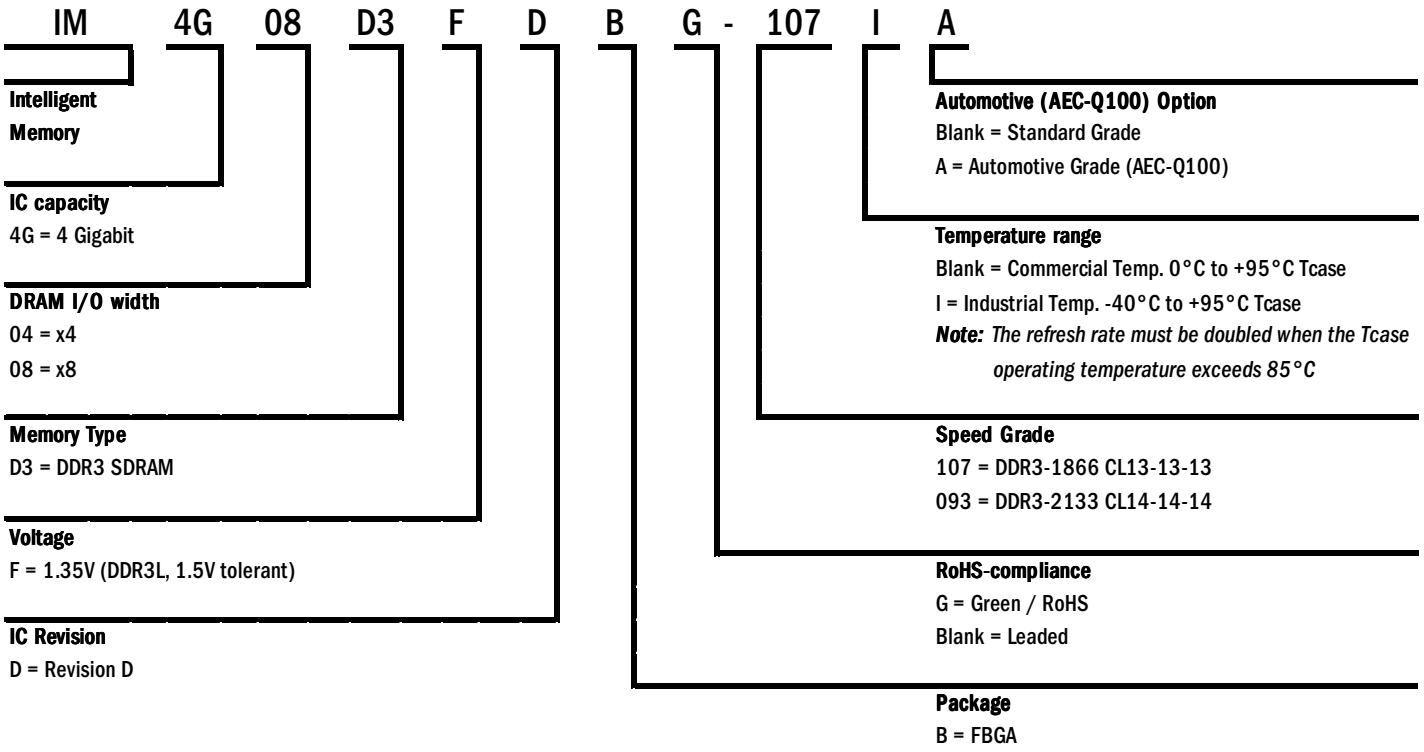
Option	*Marking*
• Configuration	
- 1Gx4 (8 Banks x 128Mbit x 4)	4G04
- 512Mx8 (8 Banks x 64Mbit x 8)	4G08
• Package	
- 78-ball FBGA (7.5mm x 10.6mm) for x4/x8	B
• Leaded/Lead-free	
- Leaded	<blank>
- Lead-free/RoHS	G
• Speed/Cycle Time	
- 1.07 ns @ CL13 (DDR3-1866)	-107
- 0.938 ns @ CL14 (DDR3-2133)	-093
• Temperature	
- Commercial 0°C to +95°C Tcase	<blank>
- Industrial -40°C to +95°C Tcase	I
• Automotive Grade	
- Non-Automotive	<blank>
- Automotive AEC-Q100	A

Example Part Number: IM4G08D3FDBG-107IA

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipe-lined architecture
- Bi-directional differential data strobe (DQS and $\overline{\text{DQS}}$) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted $\overline{\text{CAS}}$ by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- $\overline{\text{RESET}}$ pin for Power-up sequence and reset function
- SRT range: Normal/extended
- Programmable Output driver impedance control

Part Number Information



4Gb DDR3 SDRAM Addressing

Configuration	1Gb x 4	512Mb x 8
# of Bank	8	8
Bank address	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP
Row Address	A0 ~ A15	A0 ~ A15
Column Address	A0 ~ A9, A11	A0 ~ A9
BC switch on the fly	A12/$\overline{BC}$	A12/$\overline{BC}$
Page size	1 KB	1 KB

Pin Configurations

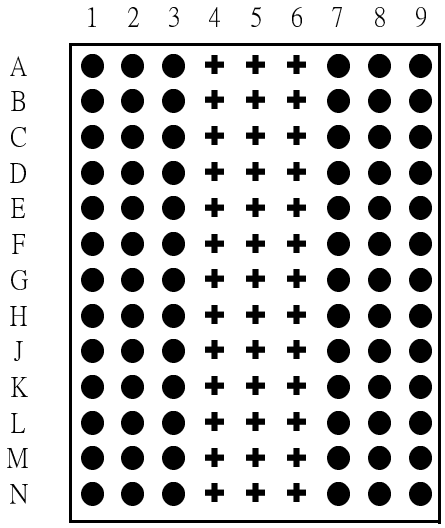
78-ball FBGA (x4 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{SS}	V_{DD}	NC				NC	V_{SS}	V_{DD}	A
B	V_{SS}	V_{SSQ}	DQ0				DM	V_{SSQ}	V_{DDQ}	B
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}	C
D	V_{SSQ}	NC	$\overline{DQS}$				V_{DD}	V_{SS}	V_{SSQ}	D
E	V_{REFDQ}	V_{DDQ}	NC				NC	NC	V_{DDQ}	E
F	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	F
G	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	G
H	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	H
J	V_{SS}	BA0	BA2				A15	V_{REFCA}	V_{SS}	J
K	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	K
L	V_{SS}	A5	A2				A1	A4	V_{SS}	L
M	V_{DD}	A7	A9				A11	A6	V_{DD}	M
N	V_{SS}	$\overline{RESET}$	A13				A14	A8	V_{SS}	N

Ball Location (x4)

- ● Populated ball
- ✚ Ball not populated

Top view
(See the balls through the package)



Pin Configurations

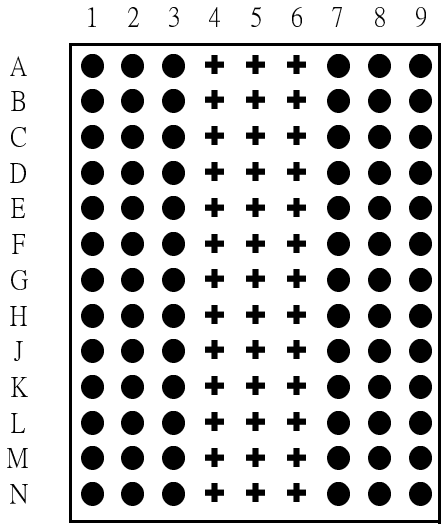
78-ball FBGA (x8 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{SS}	V_{DD}	NC				NU/$\overline{TDQS}$	V_{SS}	V_{DD}	A
B	V_{SS}	V_{SSQ}	DQ0				DM/TDQS	V_{SSQ}	V_{DDQ}	B
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}	C
D	V_{SSQ}	DQ6	$\overline{DQS}$				V_{DD}	V_{SS}	V_{SSQ}	D
E	V_{REFDQ}	V_{DDQ}	DQ4				DQ7	DQ5	V_{DDQ}	E
F	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	F
G	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	G
H	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	H
J	V_{SS}	BA0	BA2				A15	V_{REFCA}	V_{SS}	J
K	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	K
L	V_{SS}	A5	A2				A1	A4	V_{SS}	L
M	V_{DD}	A7	A9				A11	A6	V_{DD}	M
N	V_{SS}	$\overline{RESET}$	A13				A14	A8	V_{SS}	N

Ball Location (x8)

- ● Populated ball
- ✚ Ball not populated

Top view
(See the balls through the package)

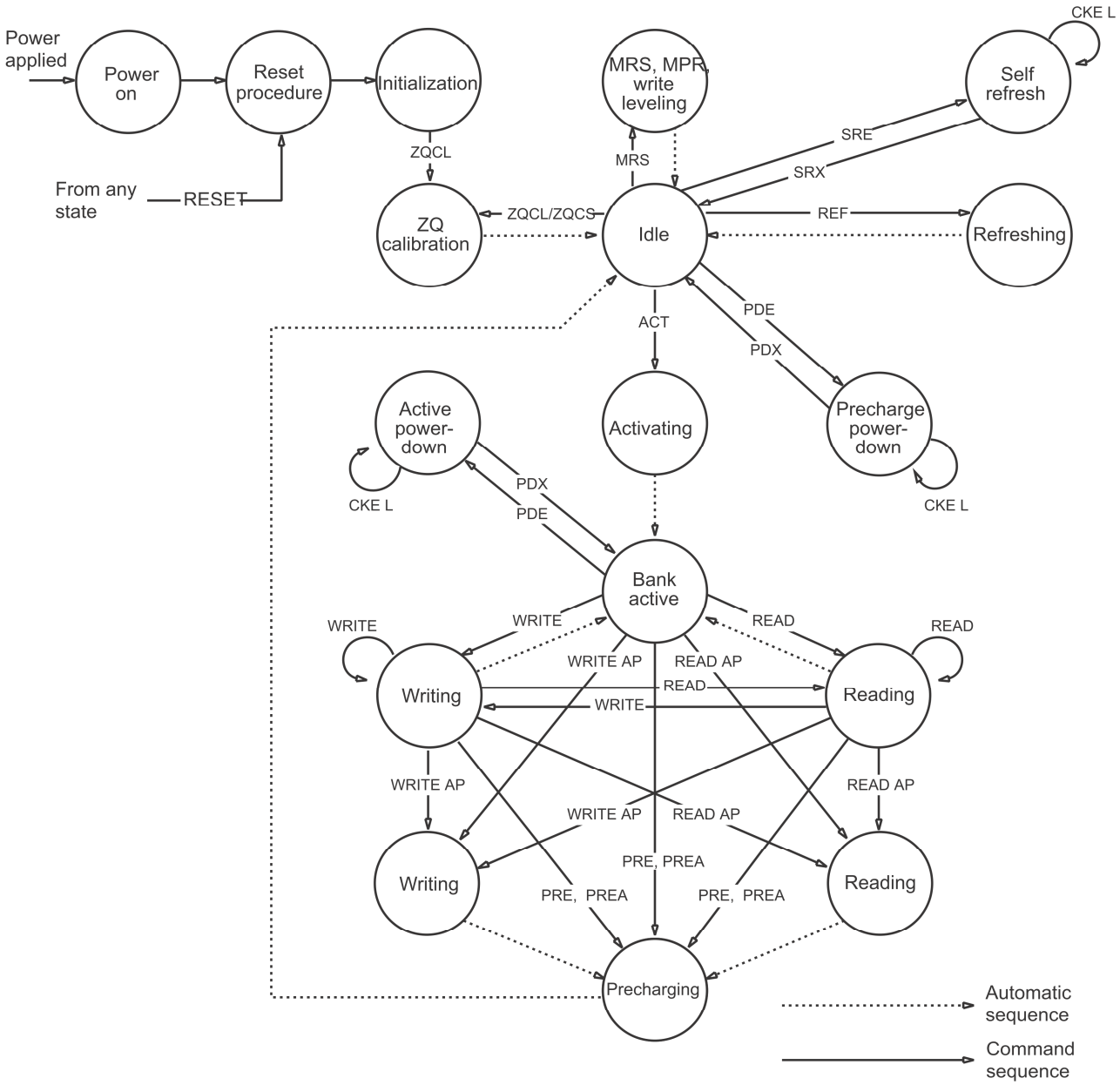


Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power- down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable RTT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/$\overline{TDQS}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Autoprecharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be per-formed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: No Autoprecharge) A10 is sampled during a Precharge command to determine whether the Pre- charge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	**Burst Chop:** A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be per-formed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/ Output	**Data Input/ Output:** Bi-directional data bus
DQS, $\overline{DQS}$	Input/ Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals $\overline{DQS}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

Pin	Type	Function
TDQS, $\overline{TDQS}$	Output	**Termination Data Strobe :** TDQS/$\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and $\overline{TDQS}$ is not used.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ power supply: 1.35V, 1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.35V, 1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation.
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference Voltage for DQ
V_{REFCA}	Supply	Reference Voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE : Input only pins (BA0-BA2, A0-A15, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT and $\overline{RESET}$) do not supply termination.		

Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE
PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry
SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Basic Functionality

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row).The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode “on the fly” (via A12) if enabled in the mode register.

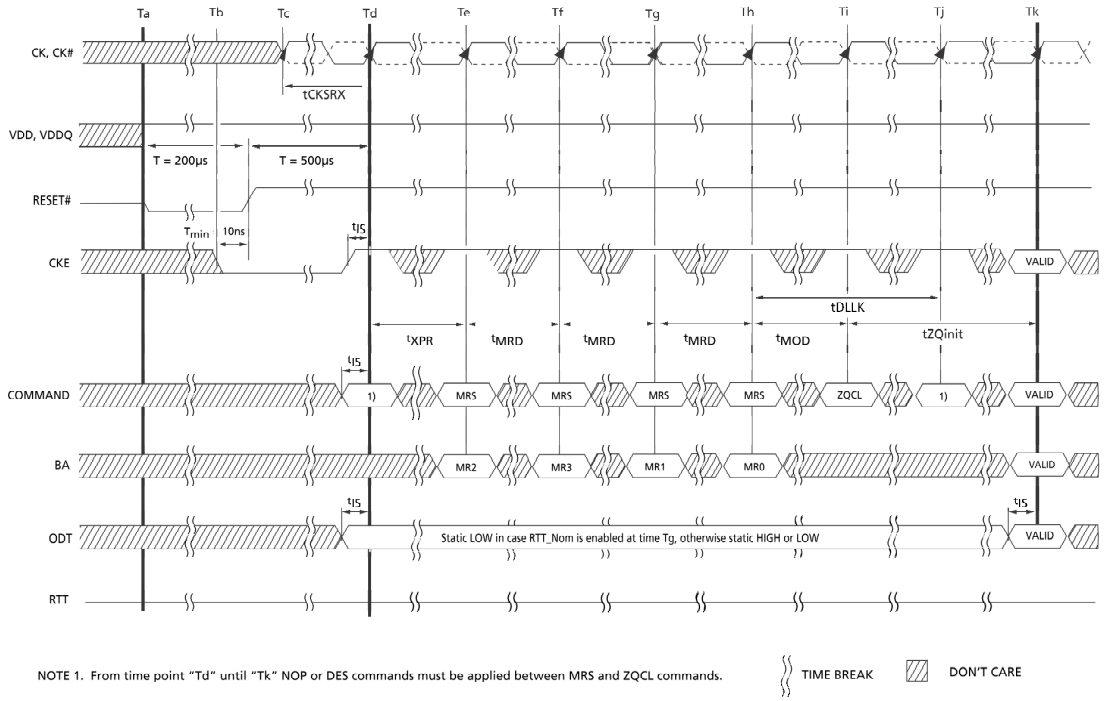
Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain $\overline{\text{RESET}}$ below 0.2 x V_{DD} (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200µs with stable power. CKE is pulled “Low” anytime before $\overline{\text{RESET}}$ being de-asserted (min time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no longer than 200ms; and during the ramp, $V_{DD} > V_{DDQ}$ and $V_{DD} - V_{DDQ} < 0.3$ volts.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95V max once power ramp is finished, AND
   - V_{REF} tracks $V_{DDQ}/2$.

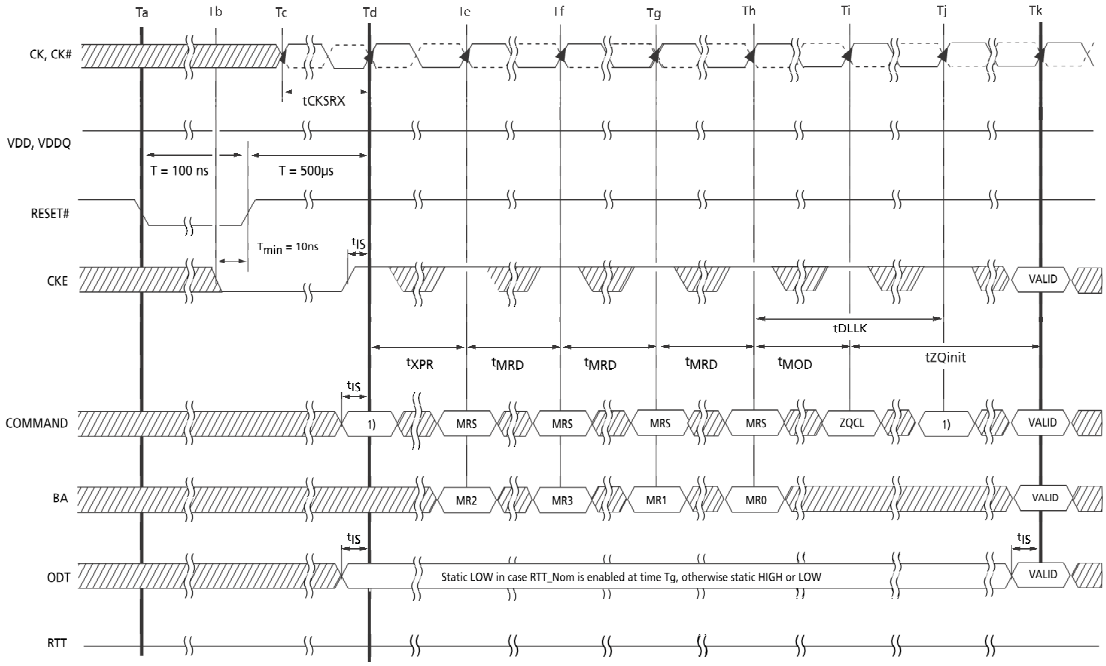
   or
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REF}.
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or $5t_{CK}$ (which is larger) before CKE goes active.
   Since CKE is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequences finished, including expiration of t_{DLLK} and t_{ZQinit}.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{DLLK} and t_{ZQinit}.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, t_{XPR}, before issuing the first MRS command to load mode register.(t_{XPR}=Max(t_{XS}, $5t_{CK}$)]
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue ”DLL Enable” command, provide “Low” to A0, ”High” to BA0 and “Low” to BA1-BA2)
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both t_{DLLK} and t_{ZQ} init completed.
12. The DDR3 SDRAM is now ready for normal operation.



Reset and Initialization with Stable Power

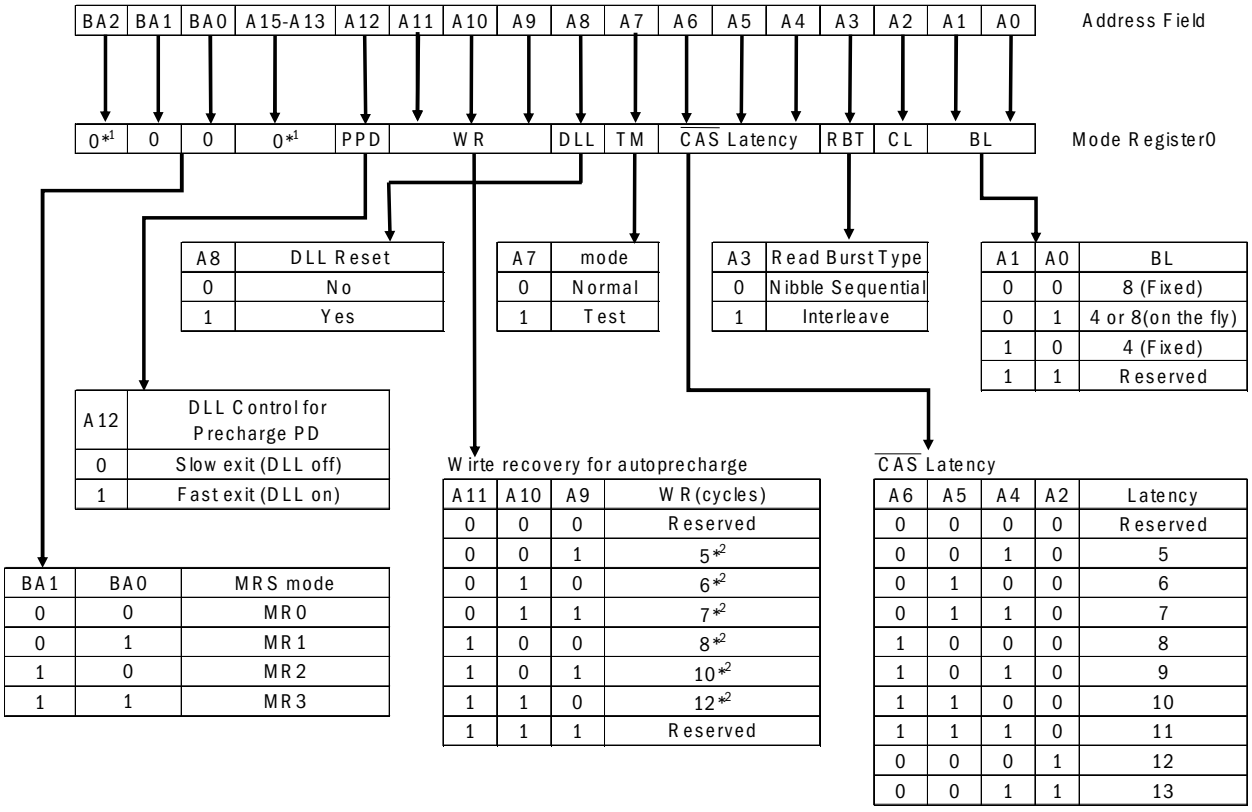
The following sequence is required for $\overline{\text{RESET}}$ at no power interruption initialization.

1. Assert RESET below 0.2 x V_{DD} anytime when reset is needed (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 100ns. CKE is pulled low before RESET being de-asserted (minimum time 10ns).
2. Follow Power-Up initialization Sequence steps 2 to 11.
3. The reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



Mode Register MR0

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, $\overline{\text{CAS}}$ latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	4 or 8(on the fly)
1	0	4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Wirte recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	Reserved

$\overline{\text{CAS}}$ Latency

A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13

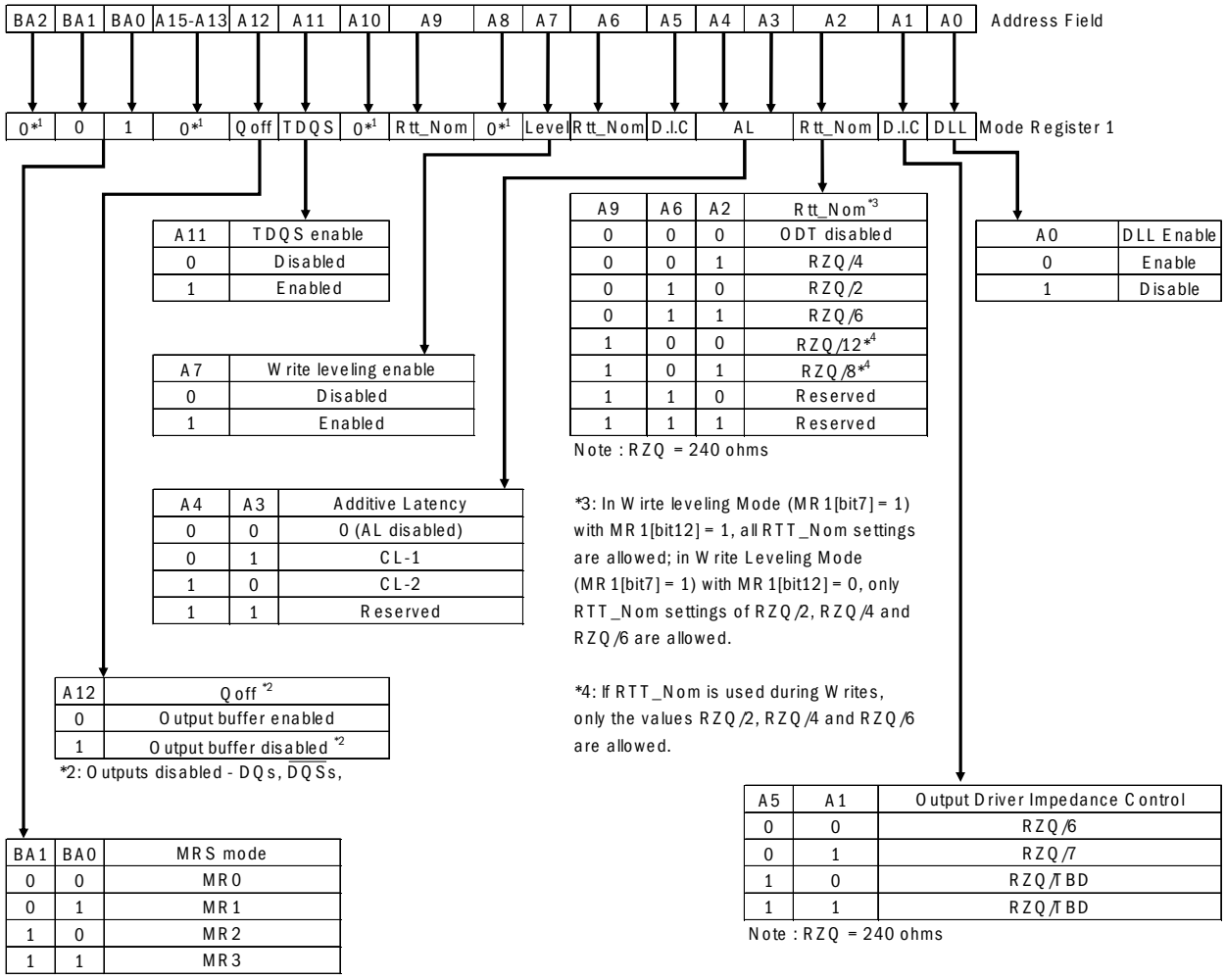
*1: BA2 and A13-A15 are reserved for future use and must be programmed to 0 during MRS.

*2: WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing t_{WR}(in ns) by t_{CK}(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[ns]/t_{CK}[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin The programmed WR value is used with t_{RP} to determine t_{DAL}.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff.

The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.



A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, $\overline{DQS}$s,

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A9	A6	A2	Rtt_Nom *3
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note : RZQ = 240 ohms

*3: In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

*4: If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

A0	DLL Enable
0	Enable
1	Disable

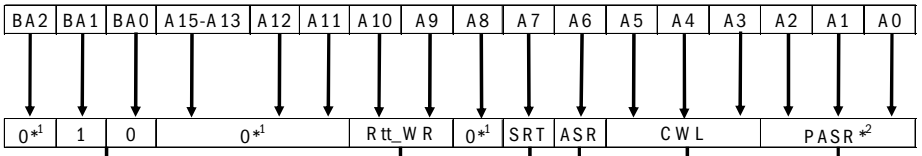
A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note : RZQ = 240 ohms

*1: BA2, A8, A10, A13-A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, RTT_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.



A7	Self-refresh temperature range (SRT)
0	Normal operating temperature range
1	Extend temperature self-refresh (Optional)

A6	Auto Self-refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A2	A1	A0	Partial Array Self Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111
1	0	1	HalfArray (BA[2:0]= 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR *2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥2.5ns)
0	0	1	6(2.5ns >tCK(avg) ≥1.875ns)
0	1	0	7(1.875ns >tCK(avg) ≥1.5ns)
0	1	1	8(1.5ns >tCK(avg) ≥1.25ns)
1	0	0	9(1.25ns >tCK(avg) ≥1.07ns)
1	0	1	10(1.07ns >tCK(avg) ≥0.938ns)
1	1	0	Reserved
1	1	1	Reserved

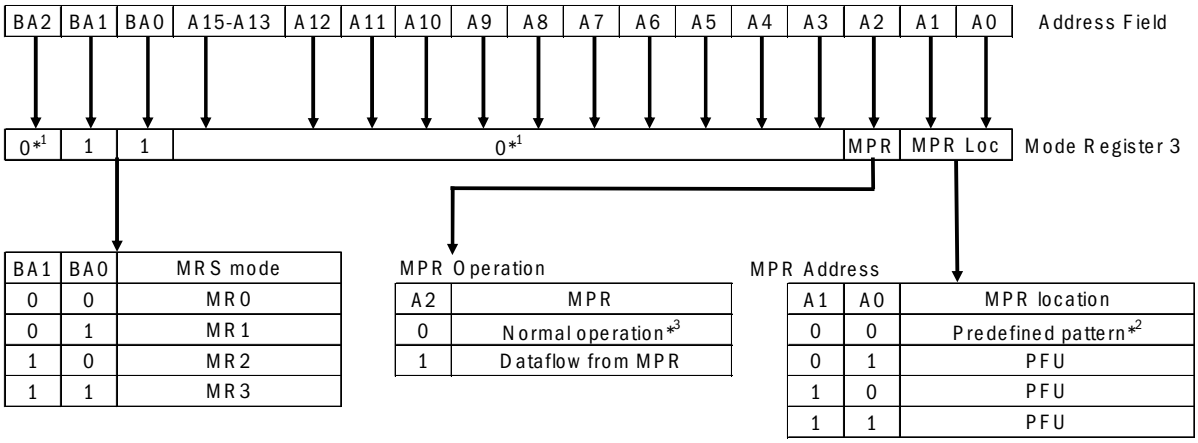
BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1: BA2, A8, A11-A15 are RFU and must be programmed to 0 during MRS.

*2: The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Mode Register MR3

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	PFU
1	0	PFU
1	1	PFU

*1: BA2, A3-A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.
*2: The predefined pattern will be used for read synchronization.
*3: When MPR control is set for normal operation, MP3 A[2] = 0, MR3 A[1:0] will be ignored.

Burst Length (MR0)

Read and write accesses to the DDR3 are burst oriented, with the burst length being programmable, as shown in the figure MR0 Programming. The burst length determines the maximum number of column locations that can be accessed for a given read or write command. Burst length options include fixed BC4, fixed BL8, and on the fly which allows BC4 or BL8 to be selected coincident with the registration of a read on write command Via A12 ($\overline{BC}$). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Burst Chop

In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. In case of burst length being selected on the fly via A12($\overline{BC}$), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks.

Burst Type (MR0)

[Burst Length and Sequence]

Burst length	Operation	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4 (Burst chop)	READ	000	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T
		001	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T
		010	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T
		011	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T
		100	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T
		101	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T
		110	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T
		111	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T
	WRITE	0VV	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X
		1VV	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X
8	READ	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
		010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
		011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
		100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
		110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
		111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0
	WRITE	VVV	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7

Remark: T: Output driver for data and strobes are in high impedance.

V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

X: Don't Care.

Notes: 1. Page length is a function of I/O organization and column addressing

2. 0...7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.

Command Truth Table

(a) Note 1,2,3,4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{BC}$=Burst Chop, X=Don't care, V=Valid]

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 - BA2	A13 - A15	A12 / $\overline{BC}$	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

Notes:
1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
6. The Power Down Mode does not perform any refresh operations.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self refresh exit is asynchronous.
9. V_{REF}(Both $V_{REFDQ}$and V_{REFCA}) must be maintained during Self Refresh operation.
10. The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as a No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition

CKE Truth Table

(a) Note 1~7 apply to the entire Command truth table

(b) CKE low is allowed only if t_{MRD} and t_{MOD} are satisfied

Current State 2	CKE		Command (N) 3	Action (N) 3	Notes
	Previous Cycle 1 (N-1)	Current Cycle 1 (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See “Command Truth Table,” on previous page					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
6. CKE must be registered with the same value on t_{CKEmin} consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the t_{CKEmin} clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + t_{CKEmin} + t_{IH}.
7. DESELECT and NOP are defined in the Command truth table
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self Refresh Exit are NOP and DESELECT only.
13. Self Refresh can not be entered while Read or Write operations. See ‘Self-Refresh Operation” and ‘Power-Down Modes” on later section for a detailed list of restrictions.
14. The Power Down does not perform any refresh operations.
15. “X” means “don’t care (including floating around V_{REF})” in Self Refresh and Power Down. It also applies to Address pins
16. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
18. ‘Idle state’ means that all banks are closed(t_{RP},t_{DAL},etc. satisfied) and CKE is high and all timings from previous operations are satisfied (t_{MRD},t_{MOD},t_{RFC},t_{ZQinit},t_{ZQoper},t_{ZQCS},etc)as well as all SRF exit and Power Down exit parameters are satisfied (t_{XS},t_{XP},t_{XPDLL},etc)

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 ~ 1.8	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 ~ 1.8	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.8	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

Operating Temperature Condition

Temp. Grade	Temperature range	Rating		Unit	Notes
		Min	Max		
Blank	Case operating temperature commercial type	0	95	°C	1,2,3
I	Case operating temperature industrial type	-40	95	°C	1,2,3

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation this temperature range must be maintained under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions applies:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval t_{REFI} to 3.9µs. (This double refresh requirement may not apply for some devices.)
   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions

Symbol	Parameter	Operation Voltage	Rating			Units	Notes
			Min	Typ	Max		
V_{DD}	Supply voltage	1.35	1.283	1.35	1.45	V	1,2,3
		1.5	1.425	1.5	1.575	V	1,2,3
V_{DDQ}	Supply voltage for Output	1.35	1.283	1.35	1.45	V	1,2,3
		1.5	1.425	1.5	1.575	V	1,2,3

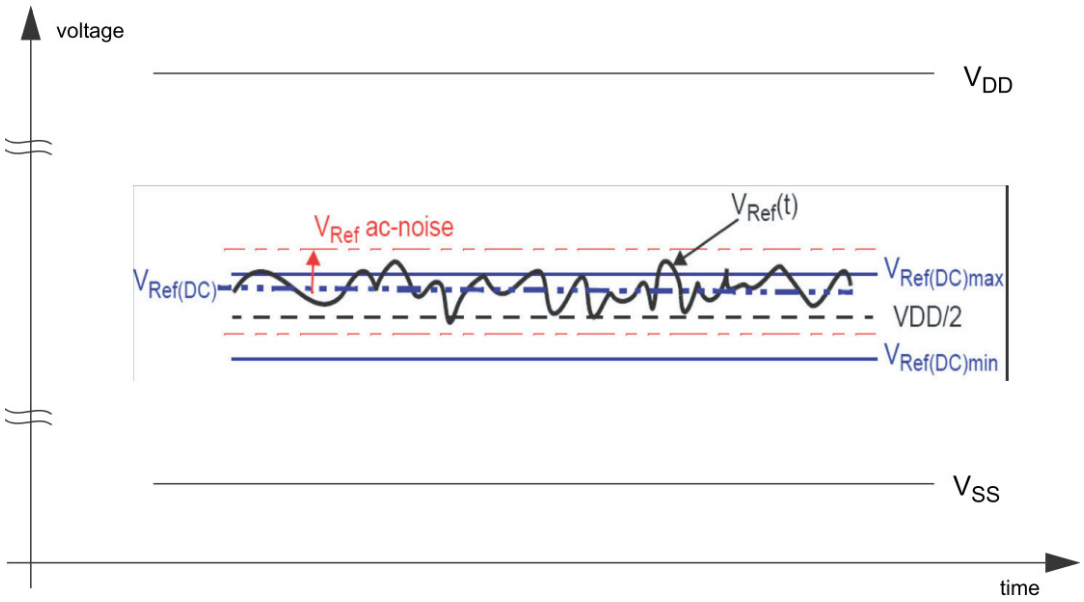
Notes:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. V_{DD} and V_{DDQ} rating are determinated by operation voltage.

V_{REF} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in figure V_{REF}(DC) tolerance and V_{REF} AC-Noise limits. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table of “Single-Ended AC and DC Input Levels for Command and Address”. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than +/- 1% V_{DD}.



V_{REF}(DC) tolerance and V_{REF} AC-Noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

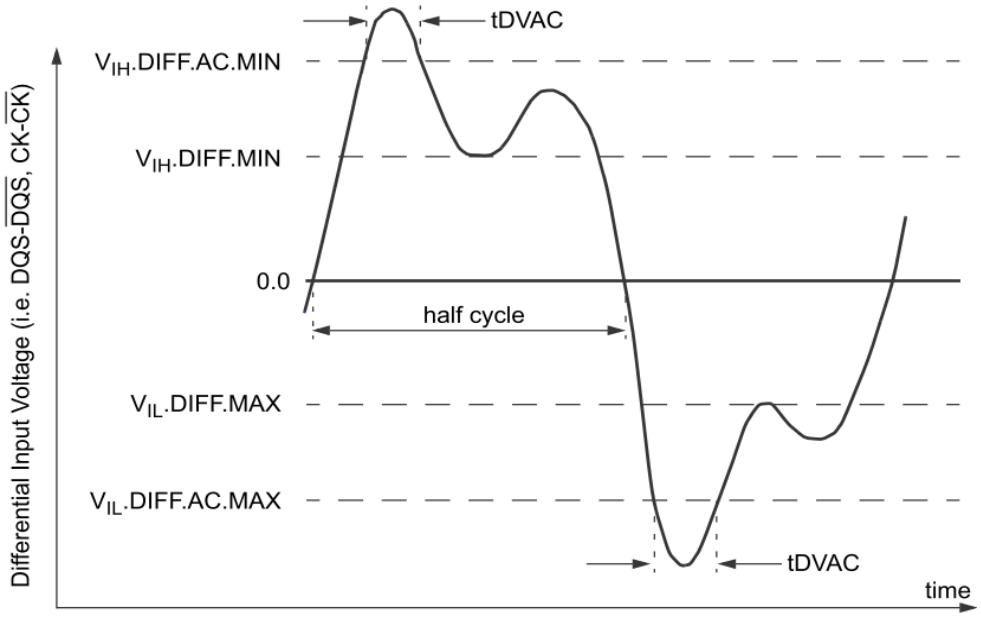
"V_{REF}" shall be understood as V_{REF}(DC), as defined in figure above, V_{REF}(DC) tolerance and V_{REF} AC- Noise limits.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and volt- age associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/- 1% of V_{DD}) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signals definition



Definition of differential ac-swing and "time above ac level" t_{DVAC}

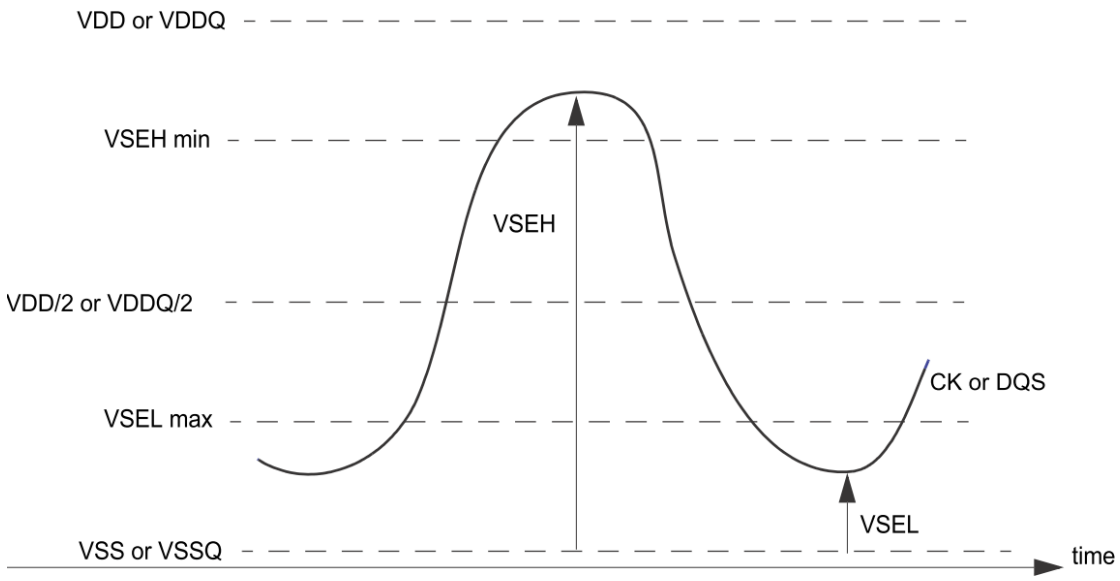
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ have to approximately reach V_{SEH} min / V_{SEL} max [approximately equal to the AC-levels (V_{IH}(AC) / V_{IL}(AC)) for Address/command signals] in every half-cycle.

DQS, $\overline{DQS}$ have to reach V_{SEH} min / V_{SEL} max [approximately the ac-levels (V_{IH}(AC) / V_{IL}(AC)) for DQ signals] in every half-cycle proceeding and following a valid transition.

Note that the applicable AC-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if V_{IH150}(AC) / V_{IL150}(AC) is used for Address/command signals, then these AC-levels apply also for the single-ended components of differential CK and $\overline{CK}$



Single-ended requirement for differential signals

Note that while Address/command and DQ signal requirements are with respect to V_{REF}, the single-ended components of differential signals have a requirement with respect to V_{DD}/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single- ended components of differential signals the requirement to reach V_{SEL} max, V_{SEH} min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

I_{DD} Specification

V_{DD}, V_{DDQ} = 1.35V (1.283V to 1.45V)

Conditions	Symbol	Data rate (Mbps)	I_{DD} max		Unit
			X4	X8	
Operating One Bank Active-Precharge Current; CKE: High; External clock: On; t_{CK}, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; : High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD0}	2133 1866	51 49	51 49	mA
Operating One Bank Active-Read-Precharge Current; CKE: High; External clock: On; t_{CK}, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; : High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD1}	2133 1866	67 64	67 64	mA
Precharge Power-Down Current Slow Exit; CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit	I_{DD2P0}	2133 1866	8 8	8 8	mA
Precharge Power-Down Current Fast Exit; CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit	I_{DD2P1}	2133 1866	18 16	18 16	mA
Precharge Standby Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD2N}	2133 1866	28 26	28 26	mA
Precharge Quiet Standby Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOAT- ING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD2Q}	2133 1866	28 26	28 26	mA

Conditions	Symbol	Data rate (Mbps)	I_{DD} max		Unit
			X4	X8	
Active Power-Down Current; CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD3P}	2133 1866	30 28	30 28	mA
Active Standby Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD3N}	2133 1866	36 32	36 32	mA
Operating Burst Read Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : High between RD; Command, Address: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD4R}	2133 1866	115 105	115 105	mA
Operating Burst Write Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; : High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2, ... ; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	I_{DD4W}	2133 1866	185 180	185 180	mA
Burst Refresh Current; CKE: High; External clock: On; t_{CK}, CL, nRFC: see timing used table; BL: 8; AL: 0; : High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD5B}	2133 1866	249 242	249 242	mA
Self Refresh Current: Normal Temperature Range; Tcase: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	I_{DD6}	2133 1866	12 12	12 12	mA
Self Refresh Current: Extended Temperature Range; Tcase: 0-95°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	I_{DD6ET}	2133 1866	16 16	16 16	mA

Conditions	Symbol	Data rate (Mbps)	I_{DD} max		Unit
			X4	X8	
Operating Bank Interleave Read Current; CKE: High; External clock: On; t_{CK}, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ... 7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD7}	2133 1866	165 140	165 140	mA
RESET Low Current; RESET: Low; External clock: off; CK and CK: LOW; CKE: FLOATING; CS, Command, Address, Data IO: FLOATING; ODT Signal: FLOATING	I_{DD8}	2133 1866	10 10	10 10	mA

Notes:

1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

3) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit

4) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

5) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range

6) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM

7) Read Burst type: Nibble Sequential, set MR0 A[3]=0B

DDR3-1866 Speed Bins

Speed Bin				- 107 (DDR3-1866)		Unit	Notes
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	Min	Max		
Internal read command to first data			t_{AA}	13.91 (13.125)	20	ns	5,9
Active to read or write delay time			t_{RCD}	13.91 (13.125)	-	ns	5,9
Precharge command period			t_{RP}	13.91 (13.125)	-	ns	5,9
Active to active/auto-refresh command time			t_{RC}	47.91 (47.125)	-	ns	5,9
Active to precharge command period			t_{RAS}	34	9 * t_{REFI}	ns	8
Average Clock Cycle Time	CL = 5	CWL = 5	t_{CK}(avg)	3.0	3.3	ns	1,2,3,6
		CWL = 6,7	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	t_{CK}(avg)	2.5	3.3	ns	1,2,3,6
		CWL = 6,7	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,6
		CWL = 7	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,6
	CL = 8	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,6
		CWL = 7	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,6
	CL = 10	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,6
		CWL = 8	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5,6,7	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 8	t_{CK}(avg)	1.25	1.5	ns	1,2,3,6
		CWL = 9	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 12	CWL = 5,6,7,8	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 9	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 13	CWL = 5,6,7,8	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 9	t_{CK}(avg)	1.07	1.25	ns	1,2,3
Supported CL setting				6, 7, 8, 9, 10, 11, 13		nCK	
Supported CWL setting				5, 6, 7, 8, 9		nCK	

DDR3-2133 Speed Bins

Speed Bin				- 093 (DDR3-2133)		Unit	Notes
CL-nRCD-nRP				14-14-14			
Parameter			Symbol	Min	Max		
Internal read command to first data			t_{AA}	13.09	20	ns	
Active to read or write delay time			t_{RCD}	13.09	-	ns	
Precharge command period			t_{RP}	13.09	-	ns	
Active to active/auto-refresh command time			t_{RC}	46.09	-	ns	
Active to precharge command period			t_{RAS}	33	9 * t_{REFI}	ns	8
Average Clock Cycle Time	CL = 5	CWL = 5,6,7,8,9,10	t_{CK}(avg)	3.0	3.3	ns	1,2,3,4,7
	CL = 6	CWL = 5	t_{CK}(avg)	2.5	3.3	ns	1,2,3,7
		CWL = 6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7,8,9,10	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,7
		CWL = 7	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4,7
		CWL = 8,9,10	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,7
		CWL = 7	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4,7
		CWL = 8,9,10	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,7
		CWL = 8	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4,7
		CWL = 9,10	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 10	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,7
		CWL = 8,9	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4,7
		CWL = 10	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5,6,7	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 8	t_{CK}(avg)	1.25	1.5	ns	1,2,3,7
		CWL = 9	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4,7
		CWL = 10	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4
	CL = 12	CWL = 5,6,7,8	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 9	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 10	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4,7
	CL = 13	CWL = 5,6,7,8	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4
		CWL = 9	t_{CK}(avg)	1.07	1.25	ns	1,2,3,7
		CWL = 10	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,4

	CL = 14	CWL = 5,6,7,8,9	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 10	t_{CK}(avg)	0.938	1.07	ns	1,2,3
Supported CL setting				5, 6, 7, 8, 9, 10, 11, 12, 13, 14		nCK	
Supported CWL setting				5, 6, 7, 8, 9, 10		nCK	

Speed Bin Table Notes

1. The CL setting and CWL setting result in t_{CK}(avg) Min and t_{CK}(avg) Max requirements. When making a selection of t_{CK}(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. t_{CK}(avg) Min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard t_{CK}(avg) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = t_{AA} [ns] / t_{CK}(avg) [ns], rounding up to the next "Supported CL".
3. t_{CK}(avg) Max limits: Calculate t_{CK}(avg) = t_{AA} Max / CL Selected and round the resulting t_{CK}(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is t_{CK}(avg) Max corresponding to CL selected.
4. "Reserved" settings are not allowed. User must program a different value.
5. “Optional” settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier’s data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
7. Any DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
8. t_{REFI} depends on operating case temperature (Tcase).
9. For devices supporting optional down binning to CL=11, CL=9 and CL=7, t_{AA} / t_{RCD} / t_{RPmin} must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1866M devices supporting down binning to DDR3-1600K or DDR3-1333H or 1066F should program 13.125ns in SPD bytes for t_{AA}min (byte 16), tRCDmin(byte18) and t_{RP}min (byte 20). Once t_{RP} (byte 20) is programmed to 13.125ns, t_{RC}min (byte 21, 23) also should be programmed accordingly. For example, 47.125ns (t_{RAS}min + t_{RP}min = 34ns+13.125ns)

AC Characteristics

(V_{DD} = 1.35V; V_{DDQ} =1.35V)

Parameter	Symbol	- 107 (DDR3-1866)		- 093 (DDR3-2133)		Unit	Note
		Min	Max	Min	Max		
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins				ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-	8	-	ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Active Bank A to Active Bank B command period for 1KB page size	t_{RRD}	5	-	5	-	ns	
		4	-	4	-	nCK	
Four activate window for 1KB page size	t_{FAW}	27	-	25	-	ns	
Address and Control input hold time (V_{IH}/V_{IL} (DC) levels)	t_{IH}(base) DC100	100	-	95	-	ps	16
Address and Control input setup time (V_{IH}/V_{IL} (AC) levels)	t_{IS}(base) AC135	65	-	60	-	ps	16,24
DQ and DM input hold time (V_{IH}/V_{IL} (DC) levels)	t_{DH}(base) DC100	70	-	55	-	ps	17
DQ and DM input setup time (V_{IH}/V_{IL} (AC) levels)	t_{DS}(base) AC135	68	-	53	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	535	-	470	-	ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	320	-	280	-	ps	25
DQ high impedance time	t_{HZ}(DQ)	-	195	-	180	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-390	195	-360	180	ps	13,14
DQS, $\overline{DQS}$ high impedance time (RL + BL/2 reference)	t_{HZ}(DQS)	-	195	-	180	ps	13,14
DQS, $\overline{DQS}$ low impedance time (RL - 1 reference)	t_{LZ}(DQS)	-390	195	-360	180	ps	13,14
DQS, $\overline{DQS}$ to DQ Skew, per group, per access	t_{DQSQ}	-	85	-	75	ps	12,13
$\overline{CAS}$ to $\overline{CAS}$ command delay	t_{CCD}	4	-	4	-	nCK	
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	0.38	-	t_{CK}(avg)	12,13
DQS, DQS rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-195	195	-180	180	ps	12,13
DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.27	0.27	-0.27	0.27	t_{CK}(avg)	
DQS falling edge hold time from rising CK	t_{DSH}	0.18	-	0.18	-	t_{CK}(avg)	29
DQS falling edge setup time to rising CK	t_{DSS}	0.18	-	0.18	-	t_{CK}(avg)	29
DQS input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}(avg)	27,28
DQS input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}(avg)	26,28

Parameter	Symbol	- 107 (DDR3-1866)		- 093 (DDR3-2133)		Unit	Note
		Min	Max	Min	Max		
DQS output high time	t_{QSH}	0.40	-	0.40	-	t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.40	-	0.40	-	t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-	4	-	nCK	
Mode register set command update delay	t_{MOD}	15	-	15	-	ns	
		12	-	12	-	nCK	
Read preamble time	t_{RPRE}	0.9	-	0.9	-	t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-	0.3	-	t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-	0.9	-	t_{CK}(avg)	1
Write postamble time	t_{WPST}	0.3	-	0.3	-	t_{CK}(avg)	1
Write recovery time	t_{WR}	15	-	51	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [t_{RP} / t_{CK}(avg)]				nCK	
Multi-purpose register recovery time	t_{MPRR}	1	-	1	-	nCK	22
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	ns	18
		4	-	4	-	nCK	18
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	ns	
		4	-	4	-	nCK	
Minimum CKE low width for Self-refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) +1nCK	-	t_{CKE}(min) +1nCK	-		
Valid clock requirement after Self- refresh entry or Power-down entry	t_{CKSRE}	10	-	10	-	ns	
		5	-	5	-	nCK	
Valid clock requirement before Self- refresh exit or Power-down exit	t_{CKSRX}	10	-	10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands requiring a locked DLL	t_{XSDLL}	tDLLK (min)	-	tDLLK (min)	-	nCK	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	260	-	260	-	ns	
Average Periodic Refresh Interval Commercial: 0°C ≤ Tcase ≤ +85°C Industrial: -40°C ≤ Tcase ≤ +85°C	t_{REFI}	-	7.8	-	7.8	µs	
Average Periodic Refresh Interval Commercial: +85°C < Tcase ≤ +95°C Industrial: +85°C < Tcase ≤ +95°C	t_{REFI}	-	3.9	-	3.9	µs	
CKE minimum high and low pulse width	t_{CKE}	5	-	5	-	ns	
		3	-	3	-	nCK	
Exit reset from CKE high to a valid command	t_{XPR}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
DLL locking time	t_{DLLK}	512	-	512	-	nCK	

Parameter	Symbol	- 107 (DDR3-1866)		- 093 (DDR3-2133)		Unit	Note
		Min	Max	Min	Max		
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	24	-	ns	2
		10	-	10	-	nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-	6	-	ns	
		3	-	3	-	nCK	
Command pass disable delay	t_{CPDED}	2	-	2	-	nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	2	-	nCK	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	2	-	nCK	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [t_{WR}/t_{CK}(avg)]				nCK	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [t_{WR}/t_{CK}(avg)]				nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRAPDEN}$	WL+4 +WR+1	-	WL+4 +WR+1	-	nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	$t_{WRAPDEN}$	WL+2 +WR+1	-	WL+2 +WR+1	-	nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	2	-	nCK	20,21
Timing of MRS command to Power-down entry	$t_{MRSPDEN}$	t_{MOD} (min)	-	t_{MOD} (min)	-		
RTT turn-on	t_{AON}	-195	195	-180	180	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t	0.3	0.7	0.3	0.7	t_{CK}(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}(avg)	
Power-up and reset calibration time	t_{ZQinit}	512	-	512	-	nCK	
Normal operation full calibration time	t_{ZQoper}	256	-	256	-	nCK	

Parameter	Symbol	- 107 (DDR3-1866)		- 093 (DDR3-2133)		Unit	Note
		Min	Max	Min	Max		
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	nCK	23
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	3
DQS, $\overline{DQS}$ delay after write leveling mode is pro-grammed	$t_{WLDQSEN}$	25	-	25	-	nCK	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	140	-	125	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	140	-	125	-	ps	
Write leveling output delay	t_{WLO}	0	7.5	0	7.5	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
Absolute clock period	$t_{CK}(abs)$	$t_{CK}(avg)$ min+ $t_{JIT}(per)$ min	$t_{CK}(avg)$ max+ $t_{JIT}(per)$ max	$t_{CK}(avg)$ min+ $t_{JIT}(per)$ min	$t_{CK}(avg)$ max+ $t_{JIT}(per)$ max	ps	
Absolute clock high pulse width	$t_{CH}(abs)$	0.43	-	0.43	-	$t_{CK}(avg)$	30
Absolute clock low pulse width	$t_{CL}(abs)$	0.43	-	0.43	-	$t_{CK}(avg)$	31
Clock period jitter	$t_{JIT}(per)$	-60	60	-50	50	ps	
Clock period jitter during DLL locking period	$t_{JIT}(per,lck)$	-50	50	-40	40	ps	
Cycle to cycle period jitter	$t_{JIT}(cc)$	-	120	-	100	ps	
Cycle to cycle period jitter during DLL locking period	$t_{JIT}(cc,lck)$	-	100	-	80	ps	
Cumulative error across 2 cycles	$t_{ERR}(2per)$	-88	88	-74	74	ps	
Cumulative error across 3 cycles	$t_{ERR}(3per)$	-105	105	-87	87	ps	
Cumulative error across 4 cycles	$t_{ERR}(4per)$	-117	117	-97	97	ps	
Cumulative error across 5 cycles	$t_{ERR}(5per)$	-126	126	-105	105	ps	
Cumulative error across 6 cycles	$t_{ERR}(6per)$	-133	133	-111	111	ps	
Cumulative error across 7 cycles	$t_{ERR}(7per)$	-139	139	-116	116	ps	
Cumulative error across 8 cycles	$t_{ERR}(8per)$	-145	145	-121	121	ps	
Cumulative error across 9 cycles	$t_{ERR}(9per)$	-150	150	-125	125	ps	
Cumulative error across 10 cycles	$t_{ERR}(10per$	-154	154	-128	128	ps	
Cumulative error across 11 cycles	$t_{ERR}(11per$	-158	158	-132	132	ps	
Cumulative error across 12 cycles	$t_{ERR}(12per$	-161	161	-134	134	ps	
Cumulative error across n = 13,14,...49,50 cycles	$t_{ERR}(nper)$	$t_{ERR}(nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min$ $t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max$				ps	32

Notes for AC Electrical Characteristics

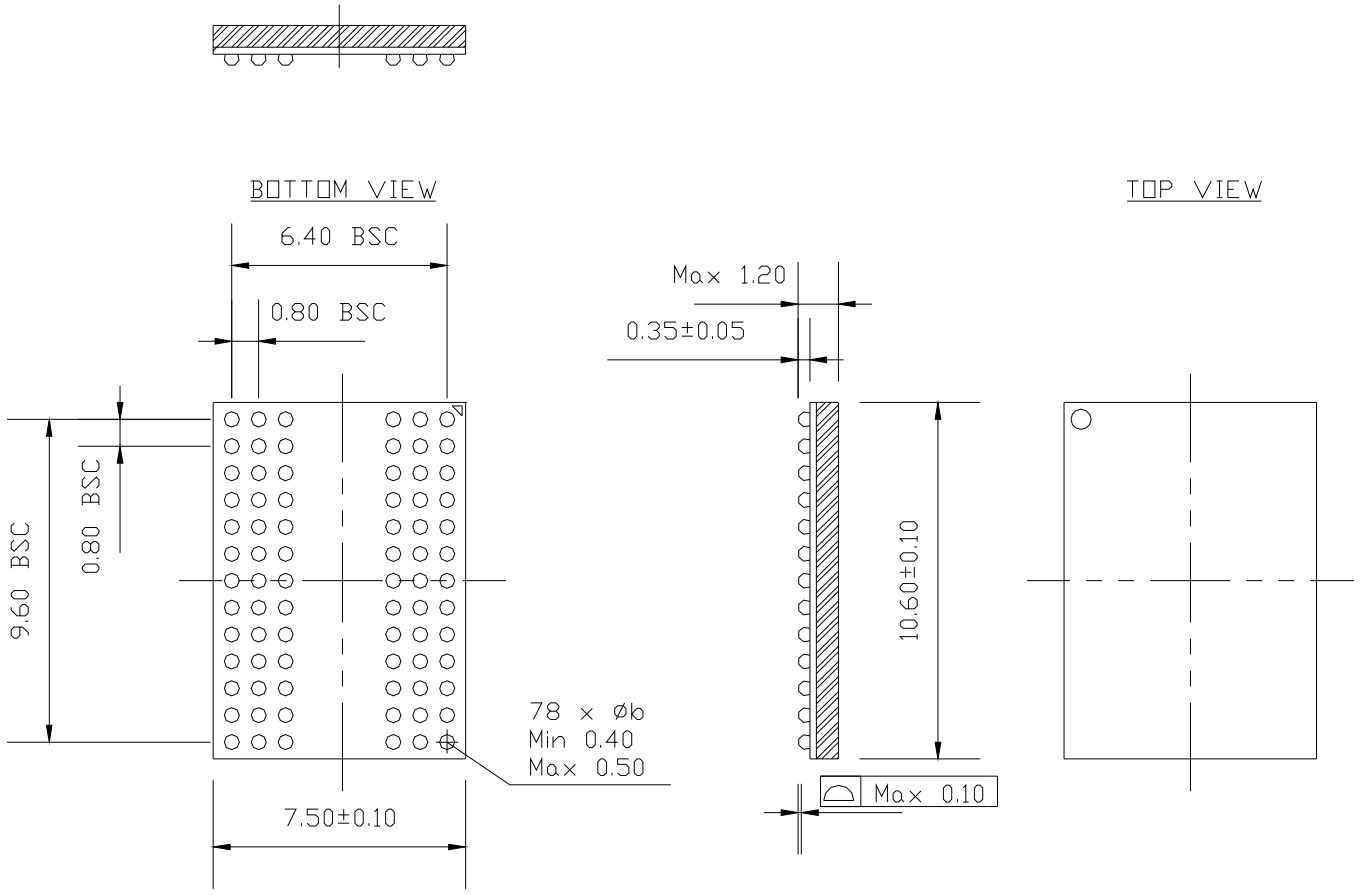
1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI}.
7. ODT turn on time (min) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min) is when the device starts to turn-off ODT resistance. ODT turn-off time (max) is when the bus is in high impedance. Both are measured from ODTLoff.
9. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR} / t_{CK} to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by t_{DQSCK}(min) plus t_{QSH}(min) on the left side and t_{HZ}(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of t_{LZ}(DQS), t_{LZ}(DQ), t_{HZ}(DQS), t_{HZ}(DQ) Notes for definition and measurement method.
15. t_{REFI} depends on operating case temperature (Tc).
16. t_{IS}(base) and t_{IH}(base) values are for 1V/ns command/addresss single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate, Note for DQ and DM signals, V_{REF}(DC) = V_{REFDQ}(DC). For input only pins except $\overline{RESET}$, V_{REF}(DC) = V_{REFCA}(DC). See Address / Command Setup, Hold and Derating section.
17. t_{DS}(base) and t_{DH}(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals,V_{REF}(DC)= V_{REFDQ}(DC). For input only pins except RESET, V_{REF}(DC) = V_{REFCA}(DC). See Data Setup, Hold and and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows ;
    For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by t_{LZDQS}(min) on the left side and t_{DQSCK}(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.
21. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDEN}$(min) is satisfied, there are cases where additional time such as t_{XPDLL}(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

    where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

24. The t_{IS}(base) AC150 specifications are adjusted from the t_{IS}(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
25. Pulse width of a input signal is defined as the width between the first crossing of V_{REF}(DC) and the consecutive crossing of V_{REF}(DC).
26. t_{DQSL} describes the instantaneous differential input low pulse width on DQS - $\overline{DQS}$, as measured from one falling edge to the next consecutive rising edge.
27. t_{DQSH} describes the instantaneous differential input high pulse width on DQS - $\overline{DQS}$, as measured from one rising edge to the next consecutive falling edge.
28. t_{DQSH},act + t_{DQSL},act = 1 t_{CK},act ; with t_{XYZ},act being the actual measured value of the respective timing parameter in the application.
29. t_{DSH},act + t_{DSS},act = 1 t_{CK},act ; with t_{XYZ},act being the actual measured value of the respective timing parameter in the application.
30. t_{CH}(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
31. t_{CL}(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

Package Diagram (x4/x8)
78-Ball Fine Pitch Ball Grid Array Outline



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Revision History

Rev	History	Release Date	Remark
1.0	Formal release	Mar. 2020	
2.0	1. Add x4 configuration 2. Some typo correction	May 2020	
3.0	1. Remove DDR3-1333 and DDR3-1600 timing information 2. Revise the Speed Bin Table of DDR3-1866 and DDR3-2133 3. Revise Part Number Information	Feb. 2021	