APRO Co., Ltd.

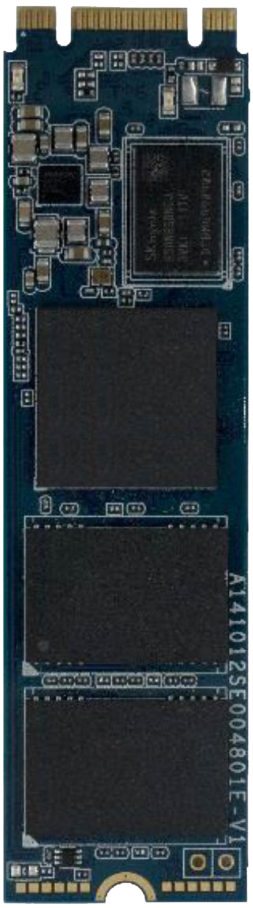
3D NAND TLC Flash

(KIOXIA BiCS5)

M.2 SATA III Module

PHANES-LR Series

M.2 2280 Type



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Product Features

- **Flash IC**
  - KIOXIA **BiCS FLASH™.**[3]
  - KIOXIA BiCS5 3D-NAND Flash.

- **Compatibility**
  - Compliant with SATA Revision 3.1
  - SATA 1.5Gbps/3.0Gbps/6.0Gbps data transfer rate.
  - ATA-8 ACS3 command set

- **Additional Capabilities**
  - S.M.A.R.T.[*1] (Self-Monitoring, Analysis and Reporting Technology) feature set support.
  - Thermal Monitor for SSD's temperature.
  - Native Command Queuing (NCQ) support.
  - TRIM maintenance command support.
  - Both Static & Dynamic wear-leveling algorithm
  - Hardware Low Density Parity Check Code, LDPC support.
  - Support Over-Provisioning.
  - Support expands register for SATA protocol 48 bits addressing mode.
  - Support of **TCG OPAL** (Optional)**[*4]**
  - Power interrupts data protection technology by Tantalum Capacitors.(Optional)

- **Mechanical**
  - Interface compatible with PCI Express™ M.2 2280)
  - M.2 keying notches in B and M positions.
  - Dimension: **2280:** 80 mm x 22 mm.
  - Weight: **2280:** 8.00 g / 0.28 oz.

- **Power Operating Voltage 3.3V(+/-) 5%**
  - Active Read (Max.) < 2000 mW.
  - Active Write (Max.) < 3000 mW.
  - Idle < 1200 mW.

- **Performance (Maximum value)** [*2]
  - **Sequential Read:** up to 550 MB/s
  - **Sequential Write:** up to 530 MB/s
  - **Random 4K Read:** up to 98K IOPS
  - **Random 4K Write:** up to 88K IOPS

- **Capacity**
  - **2280:** 240GB, 480GB, 960GB, 1.9TB.
  -

- **Reliability**
  - **TBW:** Up to 3,259 TBW at 1.9TB Capacity. (Client workload by JESD-219A)
  - **ECC:** Designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding.
  - **MTBF:** <2 million hours.
  - **UBER:** < 1 sector per 1016 bits.
  - **Temperature:** (Operating)
    Standard Grade: 0ºC ~ +70ºC
    Wide Temp. Grade: -40ºC ~ +85ºC
  - **Vibration:** 80 Hz to 2000 Hz, 20G, 3 axes
  - **Shock:** 0.5ms, 1500 G, 3 axes

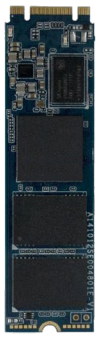
- **Certifications and Declarations**
  - **Certifications**: CE & FCC
  - **Declarations**: RoHS & REACH

Remarks:

1. Support official S.M.A.R.T. Utility.
2. Sequential performance is based on CrystalDiskMark 6.0.0 with file size 1000MB
3. **BiCS** means Bit Cost Scalable Technology.
   BiCS FLASH is a trademark of KIOXIA Corporation.
4. **TCG OPAL: Optional (Different F/W);** requires third-party software management from customer's system.

Order Information

◆ **APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series – 2280 Form-factor**

Product Picture	Grade	Standard grade (0ºC ~ 70ºC)	Wide Temp. Grade (-40ºC ~ +85ºC)
	240GB	SBMDS240G-PLCT58BM(T)	WBMDS240G-PLCT58BMC(T)
	480GB	SBMDS480G-PLCT58BM(T)	WBMDS480G-PLCT58BMC(T)
	960GB	SBMDS960G-PLCT58BM(T)	WBMDS960G-PLCT58BMC(T)
	1,920GB	SBMDS1.9T-PLCT58BM(T)	WBMDS1.9T-PLCT58BMC(T)

Notes:

C : *Special conformal coating treated on whole PCBA* (Optional)

I. Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9—X11 X12 X13 X14 X15 X16 X17 X18 X19 X20

X1 : **Grade**

S: Standard Grade – operating temp. 0º C ~ 70 º C

W: Wide Temp. Grade – operating temp. -40º C ~ +85 º C

X2 : **The material of case**

B : Bare PCBA w/o Casing

X3 X4 X5 : **Product category**

MDS : M.2 SATA III host interface

X6 X7 X8 X9 : **Capacity**

240G:	480GB	**960G:**	960GB
480G:	480GB	**1.9T:**	1,920GB

X11 : **Controller**

P : PHANES Series

X12 : **Controller version**

A, B, C.....

X13 : **Controller Grade**

C : Commercial grade

X14 : **Flash IC**

T : KIOXIA NAND Flash IC

X15 X16: **Flash IC grade / Type**

T : KIOXIA 3D NAND Flash IC.

5 : BiCS-5 Generation.

X17 X18 X19: **Form-Factor**

8: 2280 Type

BM: with two notches in B and M positions use up to two PCI Express lanes and provide broader compatibility at the same time

X20 X21 : **Reserved for specific requirement**

C : Conformal coating (Optional)

T : Power interrupts data protection technology by Tantalum Capacitors.(Optional)

Revision History

Revision	Description	Date
1.0	Initial release.	2022/11/16
2.0	Add. Power interrupts data protection technology by Tantalum Capacitors.(Optional)	2023/05/08

Contents

1. Introduction

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series provides high capacity flash memory Solid State Drive (SSD) that electrically complies with SATA Revision 3.1 standard.

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series, it support SATA 1.5Gbps/3.0Gbps/6.0Gbps data transfer rate with high performance. The available disk capacities are 240GB, 480GB, 960GB and 1.9TB. The operating temperature grade is optional for standard grade 0°C ~ 70°C and Wide Temp. grade -40°C ~ +85°C.

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series provide the ultra-high speed for embedded or server operations with space constraints for host computing systems; the data transfer performance by sequential read is up to 550.0 MB/sec, and sequential write is up to 530.0 MB/sec. which is based on KIOXIA's BiCS 3D NAND flash.

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series PCB design with two notches in B and M positions use up to two PCI Express lanes and provide broader compatibility at the same time for M/B socket mounting, while the M.2 modules with only one notch in the M position use up to four PCI Express lanes; both examples we provide APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series to be a SATA storage devices.

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series provide a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series to read or write blocks of memory. A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC). APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

Figure1 Shows a block diagram of APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series.

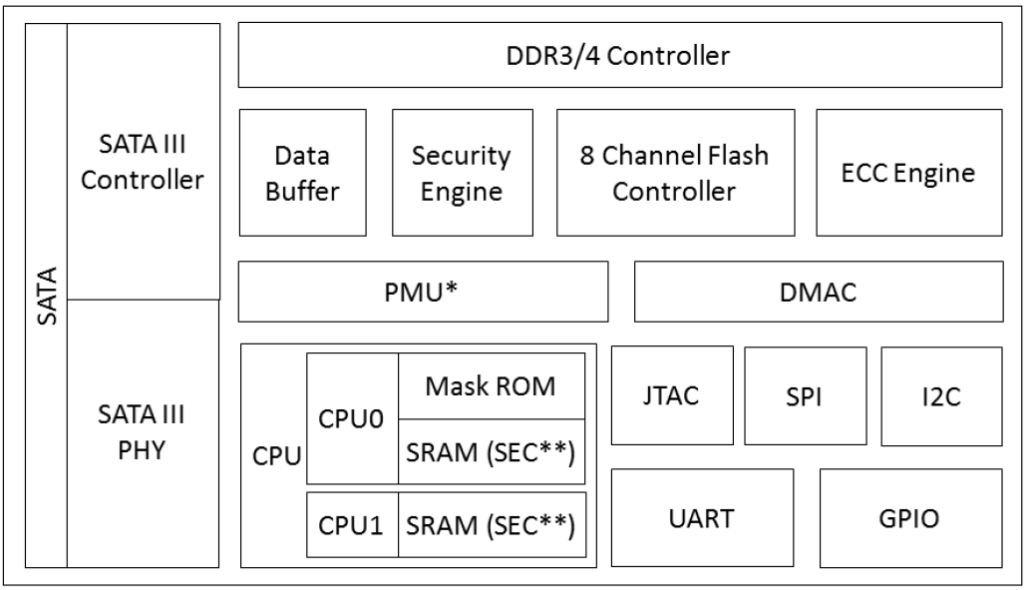


Figure 1: APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series block diagram

1.1. *Scope*

This document describes features, specifications and installation guide of APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *Flash Management Technology - Static & Dynamic Wear Leveling*

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.3. *Bad Block Management*

- **Early Bad Block**

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

- **Later Bad Block**

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Latter Bad Block.

Bad block management is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

1.4. *Error Correcting Coding (ECC)*

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series to read or write blocks of memory.

A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC). APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

1.5. *3D-NAND Flash*

3D NAND is a vertical implementation of the NAND flash cell memory array. The memory cell transistors forming the NAND string are connected in a series vertically and the memory transistors are changed from the floating-gate type to a trapped charge type.

In floating-gate technology, die density is increased by shrinking peripheral circuits and active circuits.

With 3D, holding the X/Y dimension of the die constant, die density is increased through multiple layers of the active circuits on the

Z axis. Higher-density 3D NAND die enables applications needing high-density NAND chip solutions.

1.6. *DRAM Buffer*

SSDs designed with a DRAM buffer which is support high transfer rate as a data buffer for the SSD; SSD with DRAM buffer is able to deliver excellent random data transfer speed.

- 512GB Supports 4GBits DRAM Cache
- 1TB Supports 8GBits DRAM Cache.
- 2TB Supports 16GBits DRAM Cache.

1.7. *Power interrupts data protection Technology*

In the event of an unstable power supply, SSD loses power before it can finish programming process from host to flash, this may cause data being written to the incorrect block and further leads to data corruption.

Power interrupt data protection technology is applied with several tantalum capacitors to provide power buffering after host power interruption. The Data Protection Technology provides enough time for the SSD controller can write all DRAM buffer data to flash, all data will be protected and without data loss.

This ensures all data in the DRAM buffer can be successfully written into flash. Below test is based on a 4TB SSD.

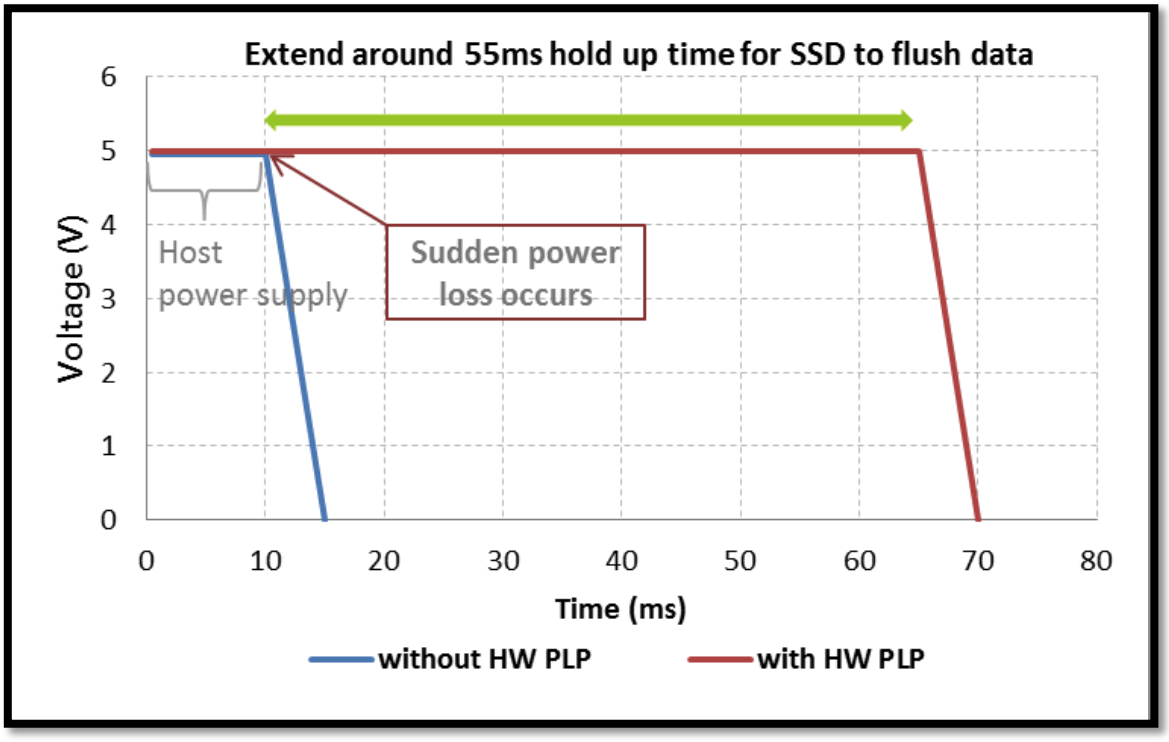


Figure 2: Hold up time for APRO 2.5" Rugged Metal SATA III SSD (3D NAND FLASH) PHANES-LRR Series

1.8. *Over-Provisioning*

Over-Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over-Provisioning, the performance and IOPS (Input / Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.9. *Thermal Monitor*

Thermal monitors are devices for measuring temperature, and can be found in SSDs in order to issue warnings when SSDs go beyond a certain temperature. The higher temperature the thermal monitor detects, the more power the SSD consumes, causing the SSD to get aging quickly. Hence, the processing speed of a SSD should be under control to prevent temperature from exceeding a certain range. Meanwhile, the SSD can achieve power savings.

1.10. *TCG Opal 2.0 (Optional, Not Default Function)*

- Deploy Storage Device & Take Ownership: The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- Activate or Enroll Storage Device: LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device: unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life: erasure of data within one or more.

1.11. *UBER*

Table 1: UBER Calculation.

Capacity	UBER
240GB	< 1 sector per 10^{16} bits read
480GB	
960GB	
1.9TB	

Notes:

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.

2. UBER = FER (fail rate)/ Data Size (user data bit)

3. FER = uncorrectable ECC frame number / total ECC frame number

4. LDPC for Kioxia 3D aSLC ECC capability > 120bit/KB.

1.12. *MTBF*

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

Table 2: MTBF Calculation.

Capacity	MTBF
240GB	> 2 million hours
480GB	
960GB	
1.9TB	

1.13. *SSD Lifetime Management Terabytes Written (TBW)*

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

TBW = [(NAND Endurance) x (SSD Capacity) / WAF

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 219 workload.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 3: Environmental Specification

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series		Standard Grade	Wide Temp. Grade
Temperature	**Operating:**	0ºC ~ +70ºC	-40ºC ~ +85ºC
	Non-operating:	-20ºC ~ +80ºC	-50ºC ~ +95ºC
Humidity	**Operating & Non-operating:**	10% ~ 95% non-condensing	
Vibration	**Frequency/Acceleration:**	80 Hz to 2000 Hz, 20G, 3 axes	
Shock	**Operating & Non-operating:**	0.5ms, 1500 G, 3 axes	
Electrostatic Discharge (ESD)	**Temperature:**	24ºC	
	Relative Humidity:	49% (RH)	
	+/-4KV:	Device functions are affected, but EUT will be back to its normal or operational state automatically.	

2.2. System Power Requirements

Table 4: Power Requirement

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series - 2280		
DC Input Voltage (VCC)		3.3V±5%
Maximum average value	**Reading Mode :**	2,000.0 mW (max.)
	Writing Mode :	3,000.0 mW (max.)
	Idle Mode :	1,200.0 mW (max.)

Notes:

- Use CrystalDiskMark 6.0.0 with the setting of 1GB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5].
- The measured power voltage of M.2 SSD is 3.3V.
- Power consumption may differ according to flash configuration, use condition, environment and platform configuration.
- Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.
- For M.2 SATA SSD PHANES-LR Series, it will not enter to LPM (Low Power Mode) to void complex compatibility issue.
- Idle power consumption is measured at idle state with no write/read operation.

2.3. *System Performance*

Table 5: System Performances

Data Transfer Mode supporting		Serial ATA Gen-III (6.0Gb/s = 768MB/s)			
Maximum Performance	**Capacity**	**240GB**	**480GB**	**960GB**	**1.9TB**
	Sequential Read (MB/s)	550.0	550.0	550.0	550.0
	Sequential Write (MB/s)	150.0	340.0	530.0	530.0
	4KB Random Read IOPS (QD32)	47K	92K	98K	98K
	4KB Random Write IOPS (QD32)	38K	85K	88K	88K

Note:

- Performance may differ according to flash configuration, use condition, environment and platform.
- Use CrystalDiskMark 6.0.0 with Q32T1, 1GB range for sequential read/write test.
- Performance specification is under that Thermal Throttling has not worked yet.
- Operating System: Windows 10 Professional (x64)
- Intel Core i7-8700K CPU @ 3.70GHz
- Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.

2.4. *System Reliability*

Table 6: System Reliability

Wear-leveling Algorithms		Static and Dynamic wear-leveling algorithms	
Bad Block Management		Supportive	
ECC Technology		Hardware design LDPC (Low Density Parity Check)	
Erase counts		KIOXIA **BiCS5 FLASH™** 3D NAND Flash: 3K P/E Cycles	
		TBW	**DWPD**
Capacity	**240GB**	287	1.1
	480GB	705	1.3
	960GB	1,594	1.5
	1.9TB	3,259	1.6

Note:

- TBW is measured by JEDEC Client 219A workload and calculated with PE count = 3,000. It may differ according to flash configuration and platform configuration.
- DWPD (Drive Write Per Day) is calculated based on 3-year lifetime.
- DWPD = TBW / (365 days x 3 years x User Capacity)
- The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Like certain Windows OS, Linux kernel version before 2.6.33, other OS please reference each own user manual)
- The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

2.5. *Device Capacity*

Table 7: User Capacity and Addressable Sectors

	512Bytes/Sector		4KBytes/Sector	
Capacity	**Total LBA**	**Available Bytes**	**Total LBA**	**Available Bytes**
240GB	468,862,128	240,057,409,536	58,607,766	240,057,409,536
480GB	937,703,088	480,103,981,056	117,212,886	480,103,981,056
960GB	1,875,385,008	960,197,124,096	234,423,126	960,197,124,096
1,920GB	3,750,748,848	1,920,383,410,176	468,843,606	1,920,383,410,176

Note:

- 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes or 4K Bytes.
- The calculation is following IDEMA Standard.
- The total actual user usable capacity of the SSD may be less than device capacity due to SSD format, SSD partition, operating system.
- EX: OS shows 223.57GB (NTFS) with 240GB SSD.

2.6. *Physical Specifications*

Refer to Table 5 and see Figure 2 for APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series physical specifications and dimensions.

Table 8: Physical Specifications of APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series

Form-Factor	Length:	Width:	Weight:
2280	80.0 (± 0.15) mm	22.0 (± 0.15)	8.00 g / 0.28 oz.

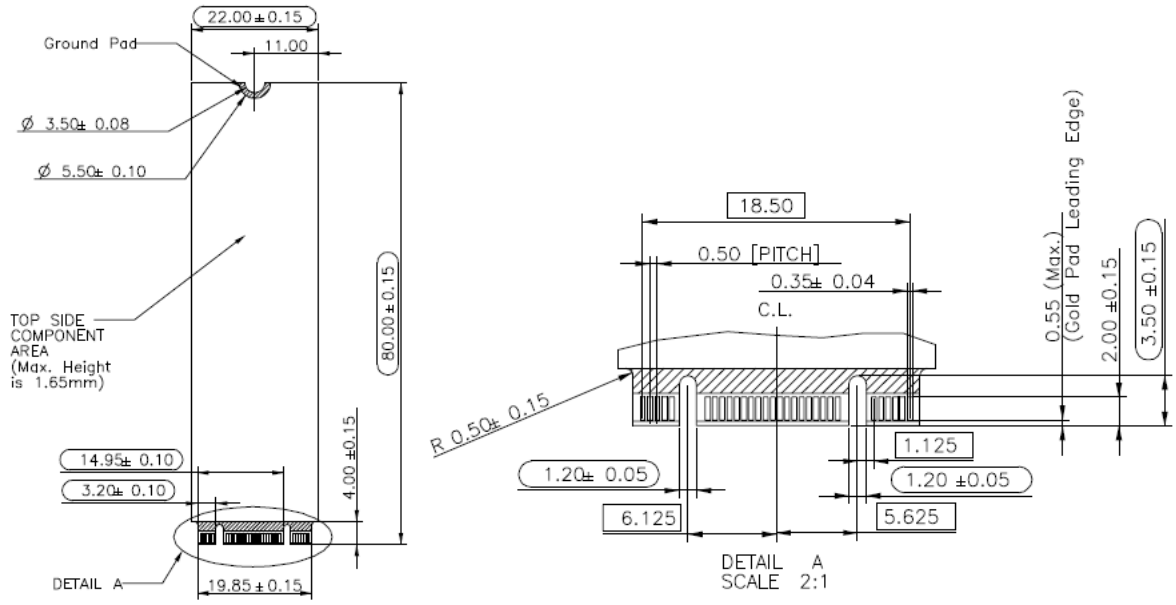


Figure 3: APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series - 2280 Dimension

2.7. *B+M Key M.2 SSD Assembly Precautions*

B+M Key M.2 SSD (Figure1 below) is compatible to both B Key (Figure2) and M Key (Figure3) sockets. However, B-Key notch is not identical to M-Key notch so user should distinguish the mating keys first and then slide M.2 SSD into the sockets accordingly. Misuse may cause severe damages to SSD including burn-out.

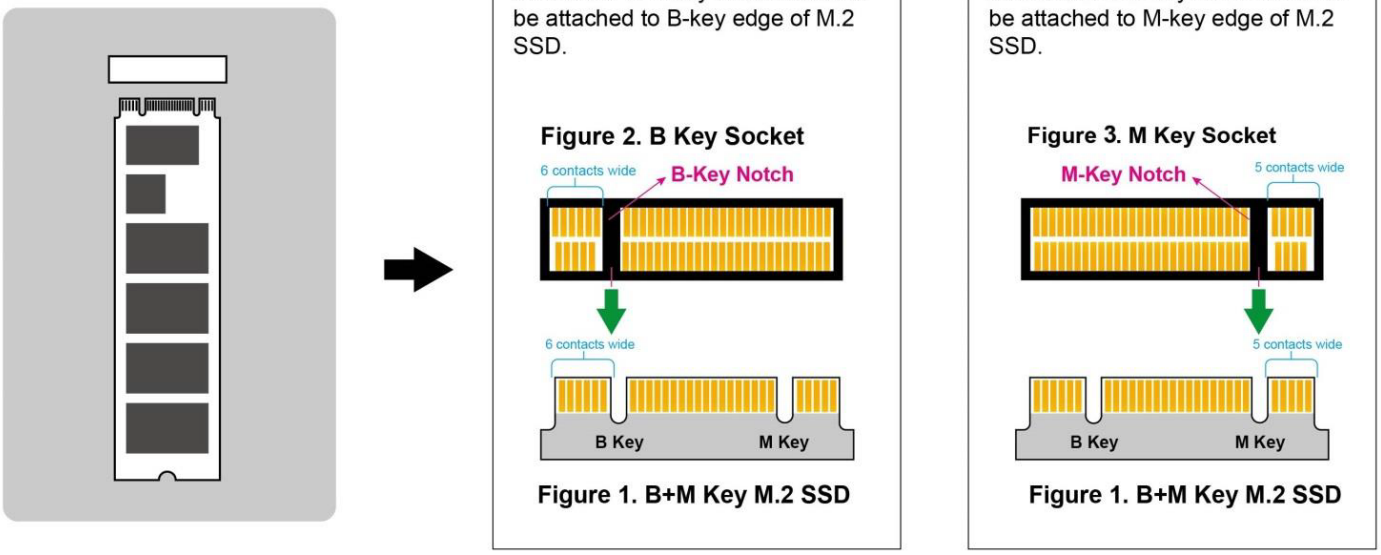


Figure 4: B+M Key M.2 Assembly Precautions

2.8. *Conformal coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. APRO applies only silicone on APRO storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

APRO use MIL-I-46058C silicon conformal coating

3. Interface Description

3.1. M.2 SATA III Module interface

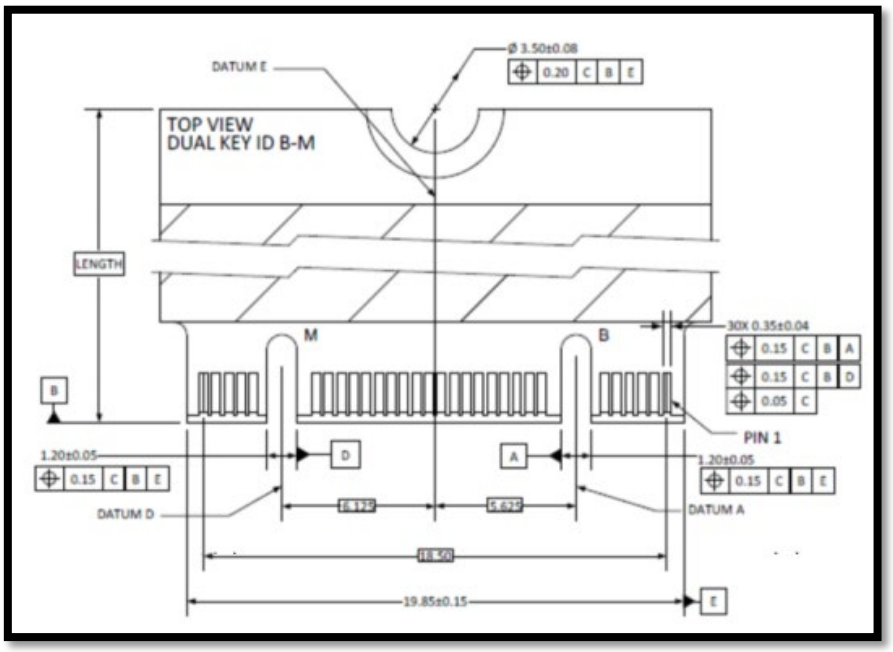


Figure 5: The connectors of Signal Segment and Power Segment

3.2. Pin Assignments

APRO 3D NAND TLC M.2 SATA III SSD PHANES-LR Series operates with standard SATA pin-out. The pin assignments are listed in below table 6.

Table 9 - Pin Assignments

Pin #	SATA Pin	Description
1	CONFIG_3 = GND	Ground
2	3.3V	Supply pin
3	GND	Ground
4	3.3V	Supply pin
5	N/C	No Connect
6	N/C	No Connect
7	N/C	No Connect
8	N/C	No Connect
9	N/C or GND Note	No Connect or Ground
10	DAS/DSS# (O) (OD)	Status indicators via LED devices that will be provided by the system Active Low. A pulled-up LED with series current limiting resistor should allow for 9mA when On.
11	N/C	No Connect
12	Module Key	

13	Module Key	
14	Module Key	
15	Module Key	
16	Module Key	
17	Module Key	
18	Module Key	
19	Module Key	
20	N/C	No Connect
21	CONFIG_0 = GND	Ground
22	N/C	No Connect
23	N/C	No Connect
24	N/C	No Connect
25	N/C	No Connect
26	N/C	No Connect
27	GND	Ground
28	N/C	No Connect
29	N/C	No Connect
30	N/C	No Connect
31	N/C	No Connect
32	N/C	No Connect
33	GND	Ground
34	N/C	No Connect
35	N/C	No Connect
36	N/C	No Connect
37	N/C	No Connect
38	DEVSLP (I) (0/3.3V) (Optional)	Device Sleep, Input. When driven high the host is informing the SSD to enter a low power state
39	GND	Ground
40	N/C	No Connect
41	SATA-B+	SATA differential signals in the SATA specification
42	N/C	No Connect
43	SATA-B-	SATA differential signals in the SATA specification
44	N/C	No Connect
45	GND	Ground
46	N/C	No Connect
47	SATA-A-	SATA differential signals in the SATA specification
48	N/C	No Connect
49	SATA-A+	SATA differential signals in the SATA specification

50	N/C	No Connect
51	GND	Ground
52	N/C	No Connect
53	N/C	No Connect
54	N/C	No Connect
55	N/C	No Connect
56	Reserved for MFG Data	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG Clock	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket
59	Module Key	
60	Module Key	
61	Module Key	
62	Module Key	
63	Module Key	
64	Module Key	
65	Module Key	
66	Module Key	
67	N/C	No Connect
68	SUSCLK (I) (0/3.3V)	No Connect
69	CONFIG_1 = GND	Defines module type
70	3.3V	Supply pin
71	GND	Ground
72	3.3V	Supply pin
73	GND	Ground
74	3.3V	Supply pin
75	CONFIG_2 = GND	Ground

Note:

- N/C for Socket 2, and GND for Socket 3.
- No support low power mode.

Appendix A: Limited Warranty

APRO warrants your 3D NAND TLC M.2 SATA III SSD PHANES-LR Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **3D NAND FLASH (Standard grade / Wide Temp. grade) 2 years / Within 3K Erasing Counts**

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