APRO Co., Ltd.

3D NAND Flash

(KIOXIA BiCS5 3D NAND) / (3D aSLC Mode)

SATA III 1.8" Flash SSD

PHANES-W Series

Document No. : 100-xP8SF-PWCT5

Version No. : 02V0

Date : April, 2023

ISO 9001 : 2015 CERTIFIED

Product Features

- **Flash IC**
  - Kioxia **BiCS-5** 3D-TLC, Toggle 3.0
  - Kioxia **BiCS FLASH™ *3**
  - KIOXIA BiCS5 3D-NAND Flash w/aSLC Technology.

- **Compatibility**
  - Compliant with SATA Revision 3.2
  - SATA 1.5Gbps/3.0Gbps/6.0Gbps data transfer rate.
  - ATA-8 ACS4 command set

- **Additional Capabilities**
  - S.M.A.R.T.*1 (Self-Monitoring, Analysis and Reporting Technology) feature set support.
  - Native Command Queuing (NCQ) support.
  - TRIM maintenance command support.
  - Both Static & Dynamic wear-leveling algorithm
  - Hardware Low Density Parity Check Code, LDPC support.
  - Support bad Block Management
  - Support DIPM/HIPM Mode for power saving
  - Support UART / GPIO function
  - Support of AES 256 & TCG OPAL(Optional)***4**

- **Mechanical**
  - micro SATA 7 pins (data) + 9 pins (power connector) host Interface
  - 1.8” form-factor (shorter than PCMCIA Type II form-factor)
  - Dimension: 54.0 mm x 78.5 mm x 5.0 mm.
  - Weight: 25g /0.88oz.

- **Power Operating Voltage 3.3V(+/-) 5%**
  - Read Mode: 1,450.0 mW (max.)
  - Write Mode: 1,750.0 mW (max.)
  - Idle Mode: 210.0 mW (max.)

- **Performance (Maximum value) *2**
  - Sequential Read: 540.0 MB/sec. (max.) ***2**
  - Sequential Write: 470.0 MB/sec. (max.) ***2**
  - 4KB Random Read: 90,000 IOPS.
  - 4KB Random Write: 80,000 IOPS.

- **Capacity**

  3D NAND : 64GB, 128GB, 256GB, 512GB, 1TB, 2TB

  3D aSLC : 32GB, 64GB, 128GB, 256GB, 512GB

- **Reliability**
  - **TBW:** (Client workload by JESD-219A)
  - **3D NAND :** Up to 3,000 TBW at 2TB Capacity.
  - **3D aSLC :** Up to 25,800 TBW at 512GB Capacity.
  - **ECC:** Designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding.
  - **MTBF :** > 3.0 million hours
  - **Temperature:** (Operating)

    Standard Grade: 0ºC ~ +70ºC

    Wide Temp. Grade: -40ºC ~ +85ºC
  - **Vibration:** 80 Hz to 2000 Hz, 20G, 3 axes.
  - **Shock:** 0.5ms, 1500 G, 3 axes.

- **Certifications and Declarations**
  - **Certifications**: CE & FCC
  - **Declarations**: RoHS & REACH

Remarks:

1. Support official S.M.A.R.T. Utility.
2. Sequential performance is based on CrystalDiskMark 5.1.2 with file size 1000MB
3. **BiCS** means Bit Cost Scalable Technology.

   BiCS FLASH is a trademark of KIOXIA Corporation.
4. **TCG OPAL: Optional (Different F/W);** Requires third-party software management from customer’s system. **AES:** Supported if system BIOS support to Set AES HDD Password.

Order Information

I. Part Number List

◆ **APRO micro SATA III SSD (BiCS-5 3D NAND & 3D aSLC) PHANES-W Series**

Product Picture	Grade	Standard grade (0ºC ~ 70ºC)	Wide Temp. Grade (-40ºC ~ +85ºC)
		Kioxia BiCS-5 3D-TLC	
	64GB	SP8SF064G-PWCT5(TG)	WP8SF064G-PWCT5(TG)C
	128GB	SP8SF128G-PWCT5(TG)	WP8SF128G-PWCT5(TG)C
	256GB	SP8SF256G-PWCT5(TG)	WP8SF256G-PWCT5(TG)C
	512GB	SP8SF512G-PWCT5(TG)	WP8SF512G-PWCT5(TG)C
	1TB	SP8SF001T-PWCT5(TG)	WP8SF001T-PWCT5(TG)C
	2TB	SP8SF002T-PWCT5(TG)	WP8SF002T-PWCT5(TG)C
		Kioxia BiCS-5 3D-TLC aSLC mode	
	32GB	SP8SF032G-PWCT5AS(TG)	WP8SF032G-PWCT5AS(TG)C
	64GB	SP8SF064G-PWCT5AS(TG)	WP8SF064G-PWCT5AS(TG)C
	128GB	SP8SF128G-PWCT5AS(TG)	WP8SF128G-PWCT5AS(TG)C
	256GB	SP8SF256G-PWCT5AS(TG)	WP8SF256G-PWCT5AS(TG)C
	512GB	SP8SF512G-PWCT5AS(TG)	WP8SF512G-PWCT5AS(TG)C

Notes:

C : *Special conformal coating treated on whole PCBA which may support industrial grade operating temperature -40°C ~ +85°C*

II. Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9 - X11 X12 X13 X14 X15 X16 X17 - C

X1 : **Grade**

S: Standard Grade – operating temp. 0º C ~ 70 º C

W: Wide Temp. Grade- operating temp. -40º C ~ +85 º C

X2 : **The material of case**

P : Plastic frame kit

X3 X4 X5 : **Product category**

8SF : 1.8” micro SATA III SSD

X6 X7 X8 X9 : **Capacity**

064G:	64GB	**512G:**	512GB
128G:	128GB	**001T:**	1TB
256G:	256GB	**002T:**	2TB

X11 : **Controller**

P : PHANES Solution

X12 : Controller version

A, B, C…..

X13 : **Controller Grade**

C : Commercial grade

X14 : **Flash IC**

T : Kioxia NAND Flash IC

X15 X16 X17 : **Flash IC grade / Type**

5 : BiCS-5 3D-NAND Flash IC.

AS : KIOXIA 3D NAND Flash IC w/aSLC Technology.

X18 X19 X20: **Reserved for specific requirement**

TG: TCG Opal 2.0 & AES 256-bits **(Optional)**

C : Conformal coating

Revision History

Revision	Description	Date
1.0	Initial release.	2023/4/12
2.0	Add 3D aSLC solution.	2023/08/08

Contents

1. Introduction

APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series provides high capacity flash memory Solid State Drive (SSD) that electrically complies with SATA Revision 3.2 standard; APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series support SATA 1.5Gb/s; SATA 3Gb/s & SATA 6Gb/s data transfer rate with high performance.

The available disk capacities are from 64GB up to 2TB for **Kioxia BiCS5 3D NAND** solution, the capacities from 32GB to 512GB are the **Kioxia BiCS5 aSLC mode solution**. The operating temperature grade is optional for Standard grade 0°C ~ 70°C and Wide Temp. Grade with conformal coating supports -40°C ~ +85°C.

APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series is suitable to handheld device embedded system, inventory recorder and particularly for serious environment monitor recorder system. The sequential read speed is 540 MB/sec and sequential write speed is 470 MB/se which were testing based on **Kioxia BiCS5 3D NAND and 3D aSLC mode solution.**

APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series to read or write blocks of memory. A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC).
APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech micro SATA III SSD controller.

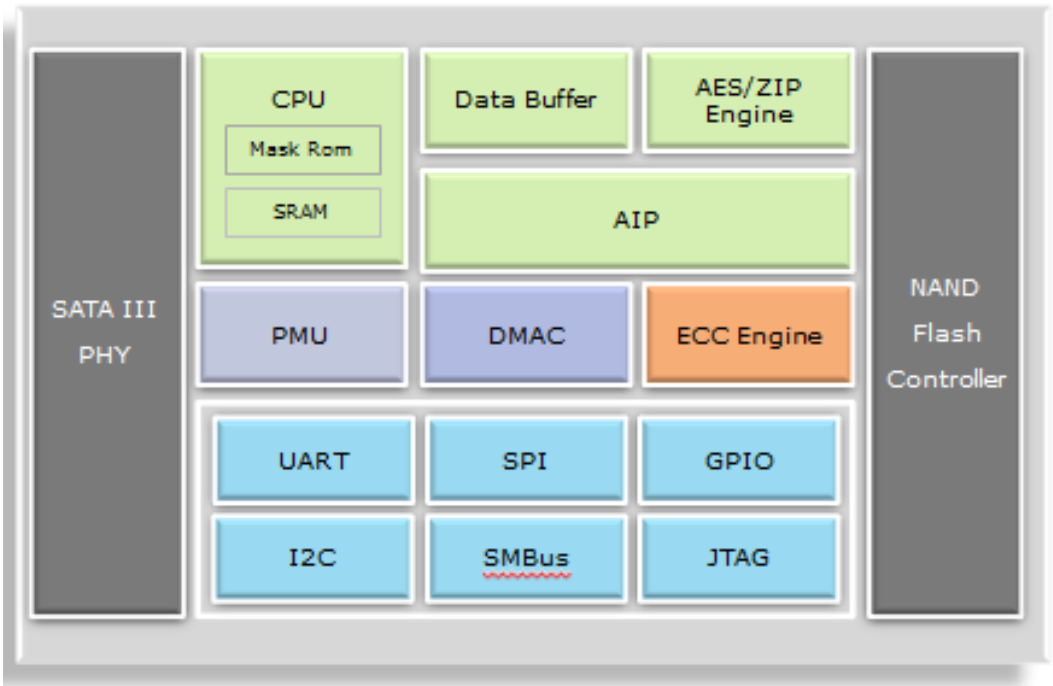

Figure 1: APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series block diagram

1.1. *Scope*

This document describes features, specifications and installation guide of APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *Flash Management Technology – Static & Dynamic Wear Leveling*

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.3. *Bad Block Management*

- **Early Bad Block**

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

- **Later Bad Block**

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Latter Bad Block.

Bad block management is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

1.4. *Error Correcting Coding (ECC)*

APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series to read or write blocks of memory. A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC). APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

1.5. *Over-Provision*

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. However, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.6. *DIPM/HIPM Mode*

SATA interfaces contain two low power management states for power saving: Partial and Slumber modes. For Partial mode, the device has to resume to full operation within 10 microseconds, whereas the device will spend 10 milliseconds to become fully operational in the Slumber mode. SATA interfaces allow low power modes to be initiated by Host (HIPM, Host Initiated Power Management) or Device (DIPM, Device Initiated Power Management). As for HIPM, Partial or Slumber mode can be invoked directly by the software. For DIPM, the device will send requests to enter Partial or Slumber mode.

1.7. *Thermal Throttling*

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations.
APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series is designed with an on-die thermal sensor and with its accuracy; firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

1.8. *3D-NAND Flash*

3D NAND is a vertical implementation of the NAND flash cell memory array. The memory cell transistors forming the NAND string are connected in a series vertically and the memory transistors are changed from the floating-gate type to a trapped charge type.
In floating-gate technology, die density is increased by shrinking peripheral circuits and active circuits.
With 3D, holding the X/Y dimension of the die constant, die density is increased through multiple layers of the active circuits on the Z axis. Higher-density 3D NAND die enables applications needing high-density NAND chip solutions.

1.9. *TCG Opal 2.0*

The Opal specification is a set of specifications for self-encrypting drives published by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes standards and specifications for secure computing. The Opal Security Subsystem Class(SSC) 2.0 defines the details of data management in storage devices and the classes authority for data access, and secures data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system.

1.9.1. TCG Opal 2.0 Main Features:

- **AES 256-bit Hardware Self Encryption**
- **Deploy Storage Device & Take Ownership:** The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- **Activate or Enroll Storage Device:** LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- **Lock & Unlock Storage Device:** Unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- **Repurpose & End-of-Life:** Erasure of data within one or more.
- **Physical Presence SID (PSID):** PSID is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

1.10. *UBER*

Table 1: UBER Calculation.

Capacity	UBER
32GB	< 1 sector per 10^{16} bits read
64GB	
128GB	
256GB	
512GB	
1TB	
2TB	

Notes:

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.

2. UBER = FER (fail rate)/ Data Size (user data bit)

3. FER = uncorrectable ECC frame number / total ECC frame number

1.11. *MTBF*

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

Table 2: MTBF Calculation.

Capacity	MTBF
32GB	> 3.0 million hours
64GB	
128GB	
256GB	
512GB	
1TB	
2TB	

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 3: Environmental Specification

APRO micro SATA III SSD PHANES-W Series		Standard Grade	Wide Temp. Grade
		SP8SFxxxG-PWCT5(TG)	WP8SFxxxG-PWCT5(TG)C
Temperature	Operating:	0ºC ~ +70ºC	-40ºC ~ +85ºC
	Non-operating:	-20ºC ~ +80ºC	-50ºC ~ +95ºC
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
Vibration	Frequency/Acceleration:	80 Hz to 2000 Hz, 20G, 3 axes	
Shock	Operating & Non-operating:	0.5ms, 1500 G, 3 axes	
Electrostatic Discharge (ESD)	Temperature:	24ºC	
	Relative Humidity:	49% (RH)	
	+/-4KV:	Device functions are affected, but EUT will be back to its normal or operational state automatically.	

2.2. System Power Requirements

Table 4: Power Requirement

BiCS-5 3D NAND						Unit: mW
Capacity	Flash Structure	Read	Write	Partial	Slumber	Idle
64GB	64GB x 1, BiCS5 TLC, BGA	970	900	65	25	210
128GB	128GB x 1, BiCS5 TLC, BGA	1,150	1,250	65	25	210
256GB	256GB x 1, BiCS5 TLC, BGA	1,150	1,350	65	25	210
512GB	256GB x 2, BiCS5 TLC, BGA	1,250	1,600	65	27	210
1TB	256GB x 4, BiCS5 TLC, BGA	1,350	1,750	65	27	210
2TB	512GB x 4, BiCS5 TLC, BGA	1,450	1,750	65	27	210
BiCS-5 3D NAND aSLC mode						
32GB	64GB x 2, BiCS5 aSLC, BGA	1,150	1,100	65	25	175
64GB	128GB x 2, BiCS5 aSLC, BGA	1,150	1,150	65	25	175
128GB	256GB x 2, BiCS5 aSLC, BGA	1,200	1,150	65	25	175
256GB	256GB x 4, BiCS5 aSLC, BGA	1,250	1,150	65	25	175
512GB	512GB x 4, BiCS5 aSLC, BGA	1,300	1,250	65	25	175

Notes:

- *It's average value of power consumption is achieved based on 100% conversion efficiency.*
- *Sequential R/W is measured while testing 4000MB sequential R/W 5 times by CrystalDiskMark.*
- *Power Consumption may differ according to flash configuration and platform.*
- *Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.*

2.3. *System Performance*

Table 5: System Performances

Data Transfer Mode supporting		Serial ATA Gen-III (6.0Gb/s = 768MB/s)			
Capacity	Flash Structure	Sequential (MB/s)		4K Random (IOPS)	
		Read	Write	Read	Write
BiCS-5 3D NAND					
64GB	64GB x 1, BiCS5 TLC, BGA	350	250	34,000	55,000
128GB	128GB x 1, BiCS5 TLC, BGA	540	420	42,000	75,000
256GB	256GB x 1, BiCS5 TLC, BGA	540	440	70,000	80,000
512GB	256GB x 2, BiCS5 TLC, BGA	540	470	85,000	80,000
1TB	256GB x 4, BiCS5 TLC, BGA	540	470	90,000	80,000
2TB	512GB x 4, BiCS5 TLC, BGA	540	470	90,000	80,000
BiCS-5 3D NAND aSLC mode					
32GB	64GB x 2, BiCS5 aSLC, BGA	540	420	42,000	75,000
64GB	128GB x 2, BiCS5 aSLC, BGA	540	440	70,000	80,000
128GB	256GB x 2, BiCS5 aSLC, BGA	540	470	85,000	80,000
256GB	256GB x 4, BiCS5 aSLC, BGA	540	470	90,000	80,000
512GB	512GB x 4, BiCS5 aSLC, BGA	540	470	90,000	80,000

Notes:

- *Performance may differ according to flash configuration and platform.*
- *The table above is for reference only.*
- *Performance is measured with the follow conditions*

(a) CrystalDiskMark 6.0, 1GB range, QD32T1 for sequential

(b) IOmeter, QD32T8, 1GB range for 4K Random

(c) Windows 10 professional (x64), Version 1809

- *Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.*

2.4. *System Reliability*

Table 6: System Reliability

Wear-leveling Algorithms		Static & Dynamic Wear-leveling	
ECC Technology		Hardware design LDPC (Low Density Parity Check)	
Erase counts		**KIOXIA BiCS-5 NAND TLC Flash** Cell Level : 3K P/E Cycles	
Capacity	**Flash Type**	**TBW**	**DWPD**
64GB	TLC	65	0.92
128GB	TLC	90	0.64
256GB	TLC	220	0.78
512GB	TLC	540	0.96
1TB	TLC	1,200	1.07
2TB	TLC	3,000	1.29

Erase counts		KIOXIA BiCS-5 aSLC mode : 30K P/E Cycles	
Capacity	**Flash Type**	**TBW**	**DWPD**
32GB	TLC w/aSLC mode	1,000	28.53
64GB	TLC w/aSLC mode	3,000	42.81
128GB	TLC w/aSLC mode	6,400	45.66
256GB	TLC w/aSLC mode	13,000	46.37
512GB	TLC w/aSLC mode	25,800	46.01

Notes:

- TBW is measured by JEDEC 219A Client workload.
- TBW may differ according to flash configuration, platform and data written.
- DWPD (Drive Write Per Day) = TBW / [365 x years x User Capacity(TB)]
- The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

2.5. *Device Capacity*

Table 7: User Capacity and Addressable Sectors

Capacity	512Bytes/Sector Total Sectors (LBA)	4KBytes/Sector Total Sectors (LBA)
32GB	62,533,296	7,816,662
64GB	125,045,424	15,630,678
128GB	250,069,680	31,258,710
256GB	500,118,192	62,514,774
512GB	1,000,215,216	125,026,902
1TB	2,000,409,264	250,051,158
2TB	4,000,797,360	500,099,670

Note:

- User Data Size depended on file management
- 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes or 4K Bytes.
- The calculation is following IDEMA Standard.
- The total actual user usable capacity of the SSD may be less than device capacity due to SSD format, SSD partition, operating system.

2.6. *Physical Specifications*

Refer to Table 5 and see Figure 2 for APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series physical specifications and dimensions.

Table 8: Physical Specifications of APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series

Length:	54.0 mm
Width:	78.5 mm
Thickness:	5.0 mm
Weight:	25g / 0.88 oz.

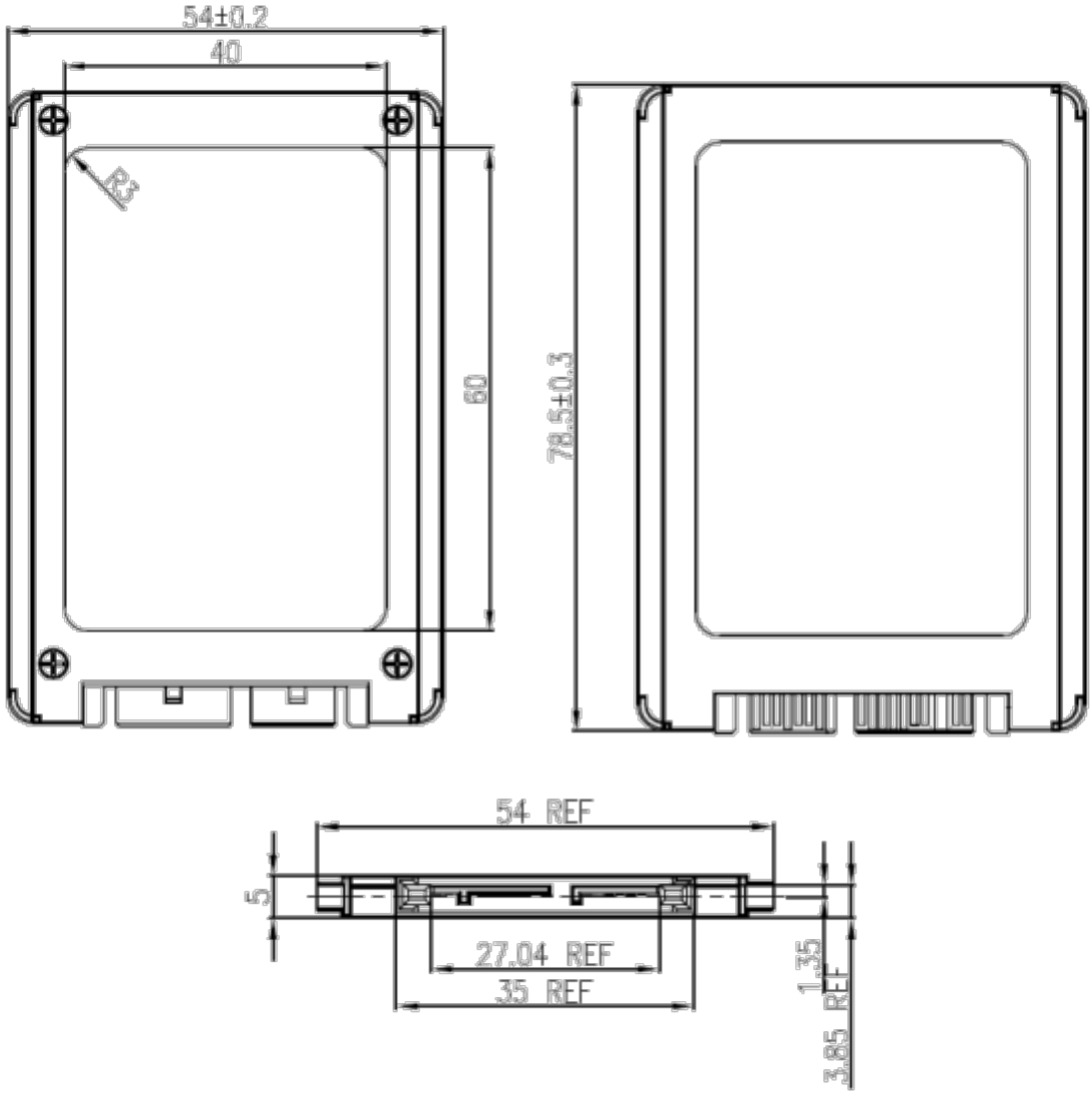

Figure 2: APRO SLC micro SATA III SSD Dimension

2.5.1. *Conformal coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. APRO applies only silicone on APRO storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

APRO use MIL-I-46058C silicon conformal coating

3. Interface Description

3.1. micro SATA III SSD interface

Refer to Table 6 and see Figure 3 for APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series pin assignments.

There are total of 7 pins in the signal segment and 9 pins in the power segment. The pin assignments are listed in below table 6.

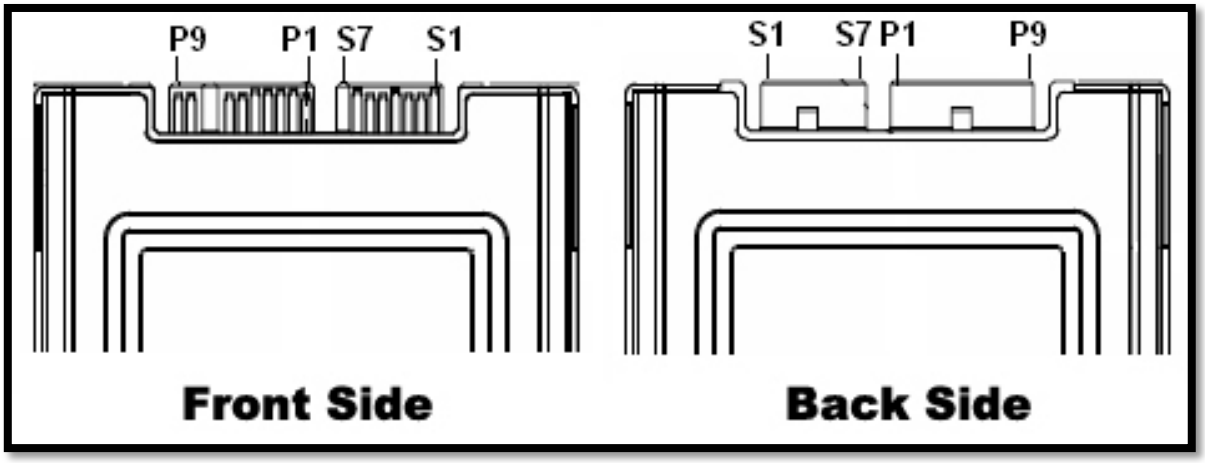

Figure 3: The connectors of SATA 7-pin (data) + 9-pin (power)

3.2. Pin Assignments

APRO micro SATA III SSD (BiCS-5 3D NAND) PHANES-W Series operates with standard SATA pin-out.

The pin assignments are listed in below table 9.

Signal Segment Pin Assignment and Descriptions		
Pin Number	**Function**	
S1	GND	
S2	A+ (Differential Signal Pair A)	
S3	A – (Differential Signal Pair A)	
S4	GND	
S5	B – (Differential Signal Pair B)	
S6	B+ (Differential Signal Pair B)	
S7	GND	
Power Segment Pin Assignment and Description		
Pin Number	**Type**	**Function**
P1	V_{33}	3.3V Power Input
P2	V_{33}	3.3V Power Input
P3	GND	GND
P4	GND	GND
P5	V_5	Reserved for 5V Power Input (Option)
P6	V_5	Reserved for 5V Power Input (Option)
P7	Optional	Reserved for Active LED (Option)
Key	Key	N/C
P8	Optional	Erase function (Option)
P9	Optional	Reserved (Not Connected)

Table 9 - Pin Assignments

4. SMART Command Reference

4.1. I/O Registers

Communication to or from device through Data register and 7 Command Block registers(28bits command format), include Feature register, Error register, Sector Count register, Sector Number register, Cylinder Low register, Cylinder High register, Drive Head register, Status register, Command register.

Table10 - Command Block Registers Addressing

Offset Address	Read	Write	Value Type
0x00	Data	Data	WORD
0x01	Error	Feature	BYTE
0x02	Sector Count	Sector Count	BYTE
0x03	Sector Number (LBA low current)	Sector Number (LBA low current)	BYTE
0x04	Cylinder Low (LBA Mid current)	Cylinder Low (LBA Mid current)	BYTE
0x05	Cylinder High (LBA High current)	Cylinder High (LBA High current)	BYTE
0x06	Drive Head	Drive Head	BYTE
0x07	Status	Command	BYTE

Direction: Input means from Host to Device, Output means from Device to Host

4.2. Command Table

Vender Command	Feature	Sector Count	Sector Number	Cylinder Low	Cylinder High	Drive Head	Command
Smart Read Attribute	0xD0	0x01	XX	0x4F	0xC2	0xA0	0xB0
Smart Read Attribute Thresholds	0xD1	0x01	XX	0x4F	0xC2	0xA0	0xB0
Smart Enable Attribute Auto Save	0xD2	0xF1	XX	0x4F	0xC2	0xA0	0xB0
Smart Disable Attribute Auto Save	0xD2	0x00	XX	0x4F	0xC2	0xA0	0xB0
Smart Enable Operations	0xD8	XX	XX	0x4F	0xC2	0xA0	0xB0
Smart Disable Operation	0xD9	XX	XX	0x4F	0xC2	0xA0	0xB0
Smart Return Status	0xDA	XX	XX	0x4F	0xC2	0xA0	0xB0

4.3. SMART Read Attribute

- **[Protocol] PIO Data In**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD0							
Sector Count	0x01							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command will return 1 sector of SMART Read Attribute information.

■ **Attribute Table**

Attribute ID	Description
01h	Number of Accumulation of Uncorrectable Error.
09h	Power on Hours Count.
0Ch	Drive Power Cycle Count (number of accumulation of power on/off cycles)
A8h	SATA PHY Error Count (Only record from power on, when power off this value will clear to zero. These values include all PHY error count, ex data FIS CRC, code error, disparity error, command FIS CRC…..)
AAh	Bad Block Count (early bad count and later bad count)
ADh	Erase Count (max. erase count and average erase count)
C0h	Number of Unexpected Power Loss
C2h	Temperature (show 33C if no thermal sensor)
DAh	Number of Accumulation CRC Error (read/write data FIS CRC error)
E7h	SSD Life Remaining
F1h	Host Write (GB)

■ **Smart Attribute Actual Data**

0	1	2	3	4	5	6	7	8	9	10	11	12
ID	**flag**	**flag**	**value**	**worst**	**DATA**						**Reserved**	**Threshold**
01h	0Bh	00h	64h	64h	Number of ECC Error						0	32h
09h	12h	00h	64h	64h	Power-on Hours Count						0	00h
0Ch	12h	00h	64h	64h	Power On/Off Cycles Count						0	00h
A8h	12h	00h	64h	64h	SATA PHY Error Count						0	00h
AAh	03h	00h	100-Max Bad Block Percent	100-Max Bad Block Percent	Early Bad Block Count		0		Later Bad Block Count		0	0Ah
ADh	12h	00h	64h	64h	Max. erase count		Avg. erase count		0		0	00h
C0h	12h	00h	64h	64h	Unexpected Power Loss Count						0	00h
C2h	23h	00h	100-Current Temp	100-Highest value	Current Temp		Min Temp		Max Temp		0	00h
DAh	0Bh	00h	64h	64h	CRC Error Count						0	32h
E7h	13h	00h	64h	64h	SSD Life Left						0	00h
F1h	12h	00h	64h	64h	Host Write (GB)						0	00h

4.4. SMART Read Attribute Thresholds

- **[Protocol] PIO Data In**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD1							
Sector Count	0x01							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command will return 1 sector of SMART Read Attribute Thresholds information.

4.5. SMART Enable Attribute Auto Save

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD2							
Sector Count	0XF1							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command enables the optional attribute auto save feature of the device.

4.6. SMART Disable Attribute Auto Save

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD2							
Sector Count	0x00							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command disables the optional attribute auto save feature of the device.

4.7. SMART Enable Operations

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD8							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command enables access to all SMART capabilities within the device.

4.8. SMART Disable Operations

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD9							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature.

4.9. SMART Return Operations

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xDA							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command will return the reliability status of the device to the host.

Appendix A: Limited Warranty

APRO warrants your micro SATA III SSD (3D NAND FLASH) PHANES-W Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **3D NAND FLASH (Wide Temp. Grade) 2 years / Within 3K Erasing Counts**
- **3D aSLC (Wide Temp. Grade) 2 years / Within 30K Erasing Counts**

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