APRO Co., Ltd.

MLC

SATA III 1.8" Flash SSD

PHANES-K Series

Document No. : 100-xP8SF-PKCTM

Version No. : 03V0

Date : April, 2023

ISO 9001 : 2015 CERTIFIED

Product Features

- **Flash IC**
  - KIOXIA 15nm NAND Flash IC.
  - Multi-Level Cell (MLC) management

- **Compatibility**
  - Compliant with SATA Revision 3.2
  - SATA 1.5Gb/s; SATA 3Gb/s & SATA 6Gb/s
  - Interface compatible.
  - ATA-8 ACS2 command set

- **Additional Capabilities**
  - S.M.A.R.T.*1 (Self-Monitoring, Analysis and Reporting Technology) feature set support.
  - Native Command Queuing (NCQ) support.
  - TRIM maintenance command support.
  - Both Static & Dynamic wear-leveling algorithm
  - Hardware Low Density Parity Check Code, LDPC support.
  - Support bad Block Management
  - Support DIPM/HIPM Mode for power saving

- **Mechanical**
  - micro SATA 7 pins (data) + 9 pins (power connector) host Interface
  - 1.8" form-factor (shorter than PCMCIA Type II form-factor)
  - Dimension: 54.0 mm x 78.5 mm x 5.0 mm.
  - Weight: 25g /0.88oz.

- **Power Operating Voltage 3.3V(+/-) 5%**
  - Read Mode: 2,355.0 mW (max.)
  - Write Mode: 2,500.0 mW (max.)
  - Idle Mode: 310.0 mW (max.)

- **Performance (Maximum value) *2**
  - Sequential Read: 550.0 MB/sec. (max.) *2
  - Sequential Write: 470.0 MB/sec. (max.) *2

- **Capacity**
  - 32GB, 64GB, 128GB, 256GB & 512GB

- **Reliability**
  - **TBW:** Up to 540 TBW at 512GB Capacity. (Client workload by JESD-219A)
  - **ECC:** Designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding.
  - **Temperature:** (Operating)
    Standard Grade: 0ºC ~ +70ºC
    Wide Temp. Grade: -40ºC ~ +85ºC
  - **Vibration:** 80 Hz to 2000 Hz, 20G, 3 axes.
  - **Shock:** 0.5ms, 1500 G, 3 axes.

- **Certifications and Declarations**
  - **Certifications**: CE & FCC
  - **Declarations**: RoHS & REACH

Remarks:

1. Support official S.M.A.R.T. Utility.
2. Test by 512GB Capacity; Sequential performance is based on CrystalDiskMark 5.1.2 with file size 1000MB

Order Information

I. Part Number List

◆ **APRO MLC micro SATA III SSD PHANES-K Series**

Product Picture	Grade	Standard grade (0ºC ~ 70ºC)	Wide Temp Grade (-40ºC ~ +85ºC)
	32GB	SP8SF032G-PKCTM	WP8SF032G-PKCTM-C
	64GB	SP8SF064G-PKCTM	WP8SF064G-PKCTM-C
	128GB	SP8SF128G-PKCTM	WP8SF128G-PKCTM-C
	256GB	SP8SF256G-PKCTM	WP8SF256G-PKCTM-C
	512GB	SP8SF512G-PKCTM	WP8SF512G-PKCTM-C

Notes:

C : *Special conformal coating treated on whole PCBA which may support industrial grade operating temperature -40°C ~ +85°C*

II. Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9 X11 X12 X13 X14 X15 X16 X17 -- C

X1 : **Grade**

S: Standard Grade – operating temp. 0º C ~ 70 º C

W: Wide Temp Grade- operating temp. -40º C ~ +85 º C

X2 : **The material of case**

P : Plastic frame kit

X3 X4 X5 : **Product category**

8SF : 1.8" micro SATA III SSD

X6 X7 X8 X9 : **Capacity**

032G:	32GB	**256G:**	256GB
064G:	64GB	**512G:**	512GB
128G:	128GB		

X11 : **Controller**

P : PHANES Solution

X12 : Controller version

A, B, C…..

X13 : **Controller Grade**

C : Commercial grade

X14 : **Flash IC**

T : Kioxia NAND Flash IC

X15 : **Flash IC grade / Type**

M : 15nm MLC **-**NAND Flash IC

C : **Reserved for specific requirement**

C : Conformal-coating

Revision History

Revision	Description	Date
1.0	Initial release.	2019/3/15
2.0	Updated document form	2019/07/19
3.0	Add. SMART Command Reference	2023/04/10

Contents

1. Introduction

APRO MLC 1.8" micro SATA III SSD PHANES-K Series provides high capacity flash memory Solid State Drive (SSD) that electrically complies with SATA Revision 3.2 standard; APRO MLC 1.8" micro SATA III SSD PHANES-K Series support SATA 1.5Gb/s; SATA 3Gb/s & SATA 6Gb/s data transfer rate with high performance.

The available disk capacities are from 32GB up to 512GB. The operating temperature grade is optional for Standard grade 0°C ~ 70°C and wide temp grade with conformal coating supports -40°C ~ +85°C.

APRO MLC 1.8" micro SATA III SSD PHANES-K Series is suitable to handheld device embedded system, inventory recorder and particularly for serious environment monitor recorder system. The sequential read speed is 550 MB/sec and sequential write speed is 470 MB/se which were testing based on 512GB capacity

APRO MLC 1.8" micro SATA III SSD provides a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO MLC 1.8" micro SATA III SSD PHANES-K Series to read or write blocks of memory. A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC).
APRO MLC 1.8" micro SATA III SSD PHANES-K Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech micro SATA III SSD controller.

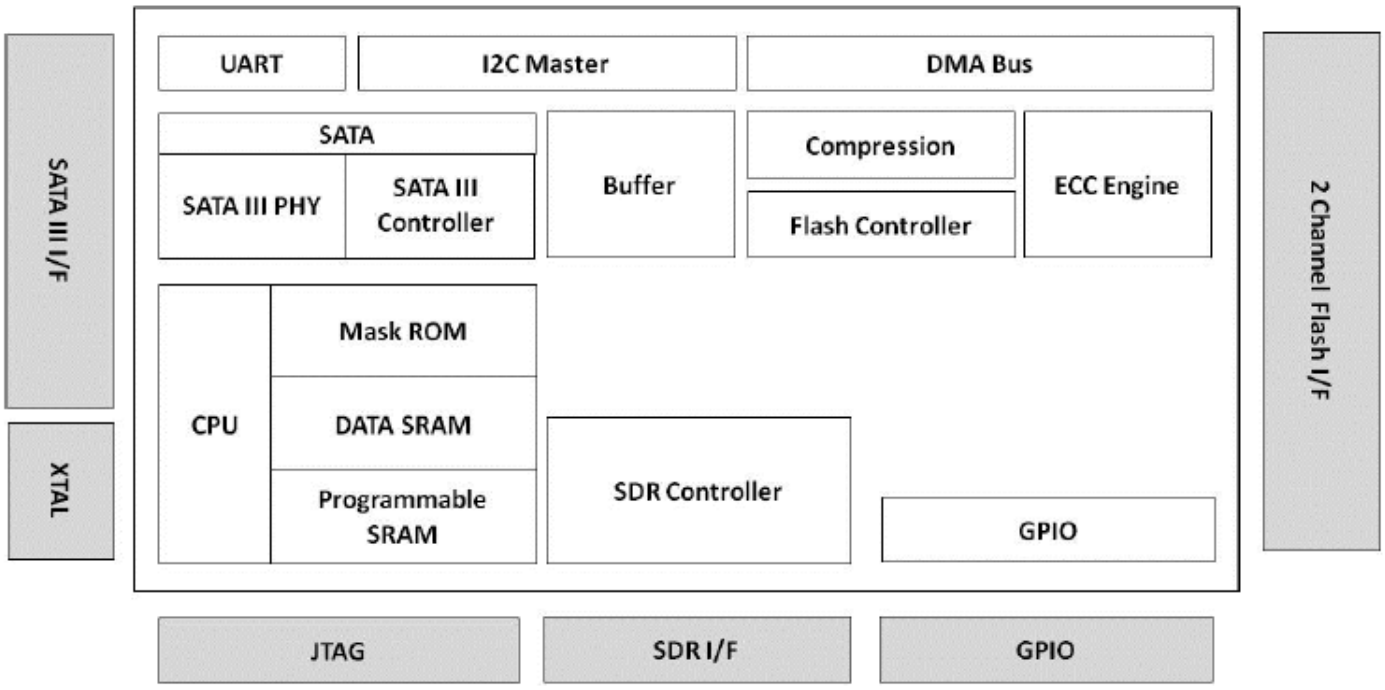

Figure 1: APRO MLC micro SATA III SSD PHANES-K Series block diagram

1.1. *Scope*

This document describes features, specifications and installation guide of APRO MLC 1.8" micro SATA III SSD PHANES-K Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *Flash Management Technology – Static & Dynamic Wear Leveling*

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

APRO MLC 1.8" micro SATA III SSD PHANES-K Series provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.3. *Bad Block Management*

- **Early Bad Block**

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

- **Later Bad Block**

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Latter Bad Block.

Bad block management is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO MLC 1.8" Slim Lite SATA III SSD HERMES-JI Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

APRO MLC 1.8" micro SATA III SSD PHANES-K Series		Standard Grade	Wide Temp Grade
		SP8SFxxxG-PKCTM	WP8SFxxxG-PKCTMC
Temperature	Operating:	0ºC ~ +70ºC	-40ºC ~ +85ºC
	Non-operating:	-20ºC ~ +80ºC	-50ºC ~ +95ºC
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
Vibration	Frequency/Acceleration:	80 Hz to 2000 Hz, 20G, 3 axes	
Shock	Operating & Non-operating:	0.5ms, 1500 G, 3 axes	
Electrostatic Discharge (ESD)	Temperature:	24ºC	
	Relative Humidity:	49% (RH)	
	+/-4KV:	Device functions are affected, but EUT will be back to its normal or operational state automatically.	

2.2. System Power Requirements

Table 2: Power Requirement

APRO MLC 1.8" micro SATA III SSD PHANES-K Series		
DC Input Voltage (VCC)		3.3V±5%
+3.3V Current	Reading Mode :	2,355.0 mW (max.)
	Writing Mode :	2,500.0 mW (max.)
	Idle Mode :	310.0 mW (max.)

2.3. System Performance

Table 3: System Performances

Data Transfer Mode supporting		Serial ATA Gen-III (6.0Gb/s = 768MB/s)				
Maximum Performance	Capacity	32GB	64GB	128GB	256GB	512GB
	Sequential Read (MB/s)	350.0	550.0	550.0	550.0	550.0
	Sequential Write (MB/s)	160.0	320.0	450.0	470.0	470.0

Note: The performance was measured using CrystalDiskMark by file size 1000MB (QD32).

2.4. *System Reliability*

Table 4: System Reliability

Wear-leveling Algorithms		Static & Dynamic Wear-leveling
Bad Block Management		Supportive
ECC Technology		Hardware design LDPC (Low Density Parity Check)
Erase counts		NAND MLC Flash Cell Level : 3K P/E Cycles
TBW (Tera Bytes Written)		
Capacity	**32GB**	13.0
	64GB	30.0
	128GB	87.0
	256GB	198.0
	512GB	540.0

Note:

- Client workload by JESD-219A.
- *The endurance of SSD could be varying based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.*

2.5. *Physical Specifications*

Refer to Table 5 and see Figure 2 for APRO MLC 1.8" micro SATA III SSD PHANES-K Series physical specifications and dimensions.

Table 5: Physical Specifications of APRO MLC micro SATA III SSD PHANES-K Series

Length:	54.0 mm
Width:	78.5 mm
Thickness:	5.0 mm
Weight:	25g / 0.88 oz.

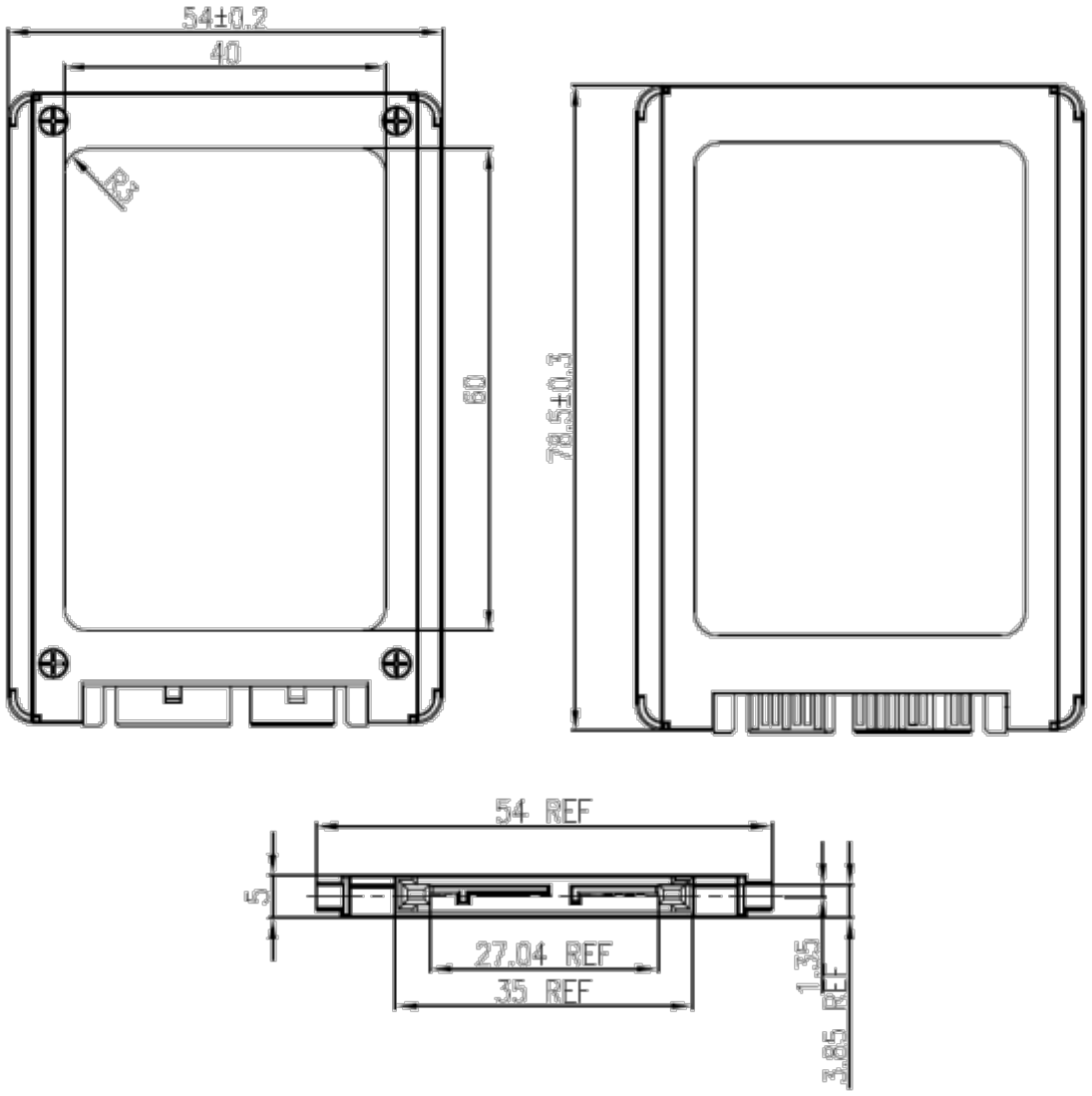

Figure 2: APRO MLC micro SATA III SSD Dimension

2.5.1. *Conformal coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. APRO applies only silicone on APRO storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

APRO use MIL-I-46058C silicon conformal coating

3. Interface Description

3.1. micro SATA III SSD interface

Refer to Table 6 and see Figure 3 for APRO 1.8" MLC micro SATA III SSD PHANES-K Series pin assignments.

There are total of 7 pins in the signal segment and 9 pins in the power segment. The pin assignments are listed in below table 6.

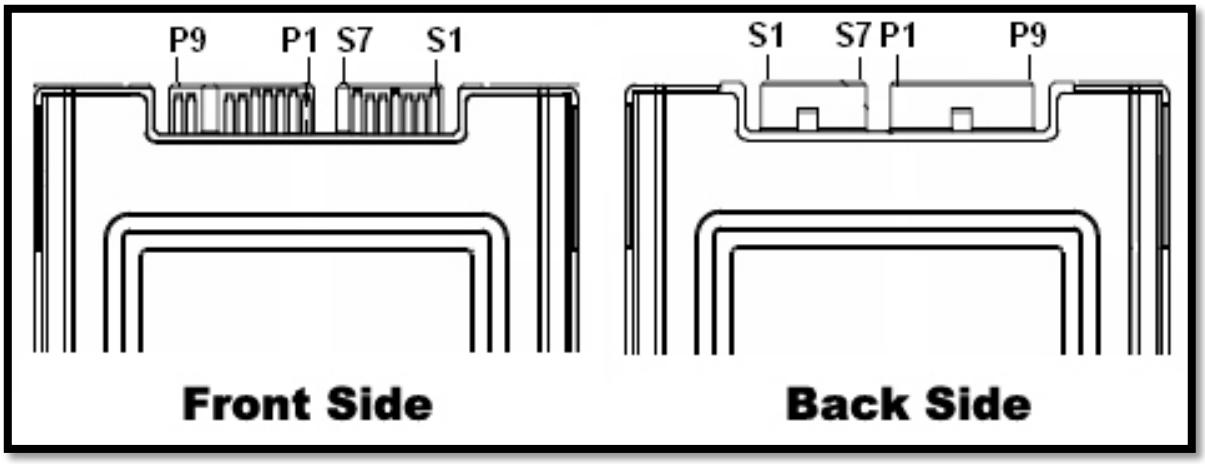

Figure 3: The connectors of SATA 7-pin (data) + 9-pin (power)

3.2. Pin Assignments

APRO MLC 1.8” micro SATA III SSD PHANES-K Series operates with standard SATA pin-out.

The pin assignments are listed in below table 6.

Signal Segment Pin Assignment and Descriptions		
Pin Number	**Function**	
S1	GND	
S2	A+ (Differential Signal Pair A)	
S3	A – (Differential Signal Pair A)	
S4	GND	
S5	B – (Differential Signal Pair B)	
S6	B+ (Differential Signal Pair B)	
S7	GND	
Power Segment Pin Assignment and Description		
Pin Number	**Type**	**Function**
P1	V_{33}	3.3V Power Input
P2	V_{33}	3.3V Power Input
P3	GND	GND
P4	GND	GND
P5	V_5	Reserved for 5V Power Input (Option)
P6	V_5	Reserved for 5V Power Input (Option)
P7	Optional	Reserved for Active LED (Option)
Key	Key	N/C
P8	Optional	Erase function (Option)
P9	Optional	Reserved (Not Connected)

Table 6 - Pin Assignments

4. SMART Command Reference

4.1. I/O Registers

Communication to or from device through Data register and 7 Command Block registers(28bits command format), include Feature register, Error register, Sector Count register, Sector Number register, Cylinder Low register, Cylinder High register, Drive Head register, Status register, Command register.

Table7 - Command Block Registers Addressing

Offset Address	Read	Write	Value Type
0x00	Data	Data	WORD
0x01	Error	Feature	BYTE
0x02	Sector Count	Sector Count	BYTE
0x03	Sector Number (LBA low current)	Sector Number (LBA low current)	BYTE
0x04	Cylinder Low (LBA Mid current)	Cylinder Low (LBA Mid current)	BYTE
0x05	Cylinder High (LBA High current)	Cylinder High (LBA High current)	BYTE
0x06	Drive Head	Drive Head	BYTE
0x07	Status	Command	BYTE

Direction: Input means from Host to Device, Output means from Device to Host

4.2. Command Table

Vender Command	Feature	Sector Count	Sector Number	Cylinder Low	Cylinder High	Drive Head	Command
Smart Read Attribute	0xD0	0x01	XX	0x4F	0xC2	0xA0	0xB0
Smart Read Attribute Thresholds	0xD1	0x01	XX	0x4F	0xC2	0xA0	0xB0
Smart Enable Attribute Auto Save	0xD2	0xF1	XX	0x4F	0xC2	0xA0	0xB0
Smart Disable Attribute Auto Save	0xD2	0x00	XX	0x4F	0xC2	0xA0	0xB0
Smart Enable Operations	0xD8	XX	XX	0x4F	0xC2	0xA0	0xB0
Smart Disable Operation	0xD9	XX	XX	0x4F	0xC2	0xA0	0xB0
Smart Return Status	0xDA	XX	XX	0x4F	0xC2	0xA0	0xB0

4.3. SMART Read Attribute

- **[Protocol] PIO Data In**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD0							
Sector Count	0x01							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command will return 1 sector of SMART Read Attribute information.

■ **Attribute Table**

Attribute ID	Description
01h	Number of Accumulation of Uncorrectable Error.
09h	Power on Hours Count.
0Ch	Drive Power Cycle Count (number of accumulation of power on/off cycles)
A8h	SATA PHY Error Count (Only record from power on, when power off this value will clear to zero. These values include all PHY error count, ex data FIS CRC, code error, disparity error, command FIS CRC…..)
AAh	Bad Block Count (early bad count and later bad count)
ADh	Erase Count (max. erase count and average erase count)
C0h	Number of Unexpected Power Loss
C2h	Temperature (show 33C if no thermal sensor)
DAh	Number of Accumulation CRC Error (read/write data FIS CRC error)
E7h	SSD Life Remaining
F1h	Host Write (GB)

■ **Smart Attribute Actual Data**

0	1	2	3	4	5	6	7	8	9	10	11	12
ID	**flag**	**flag**	**value**	**worst**	**DATA**						**Reserved**	**Threshold**
01h	0Bh	00h	64h	64h	Number of ECC Error						0	32h
09h	12h	00h	64h	64h	Power-on Hours Count						0	00h
0Ch	12h	00h	64h	64h	Power On/Off Cycles Count						0	00h
A8h	12h	00h	64h	64h	SATA PHY Error Count						0	00h
AAh	03h	00h	100-Max Bad Block Percent	100-Max Bad Block Percent	Early Bad Block Count		0		Later Bad Block Count		0	0Ah
ADh	12h	00h	64h	64h	Max. erase count		Avg. erase count		0		0	00h
C0h	12h	00h	64h	64h	Unexpected Power Loss Count						0	00h
C2h	23h	00h	100-Current Temp	100-Highest value	Current Temp		Min Temp		Max Temp		0	00h
DAh	0Bh	00h	64h	64h	CRC Error Count						0	32h
E7h	13h	00h	64h	64h	SSD Life Left						0	00h
F1h	12h	00h	64h	64h	Host Write (GB)						0	00h

4.4. SMART Read Attribute Thresholds

- **[Protocol] PIO Data In**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD1							
Sector Count	0x01							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command will return 1 sector of SMART Read Attribute Thresholds information.

4.5. SMART Enable Attribute Auto Save

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD2							
Sector Count	0XF1							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command enables the optional attribute auto save feature of the device.

4.6. SMART Disable Attribute Auto Save

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD2							
Sector Count	0x00							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command disables the optional attribute auto save feature of the device.

4.7. SMART Enable Operations

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD8							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command enables access to all SMART capabilities within the device.

4.8. SMART Disable Operations

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xD9							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature.

4.9. SMART Return Operations

- **[Protocol] PIO Non-data**
- **[Input]**

Register	7	6	5	4	3	2	1	0
Feature	0xDA							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

- **[Normal Output]**

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number (LBA LOW current)	XX							
Cylinder Low (LBA MID current)	XX							
Cylinder High (LBA HIGH current)	XX							
Drive Head	XX							
Status	0x50							

- **[Description]**

This command will return the reliability status of the device to the host.

Appendix A: Limited Warranty

APRO warrants your MLC SATA III micro SATA III SSD PHANES-K Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **MLC (Standard grade / Wide temp. grade) 2 years / Within 3K Erasing Counts**

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