

# 3D NAND Flash

(KIOXIA BiCS5 3D NAND) / (3D aSLC Mode)

## M.2 PCIe NVMe SSD

### PHANES-X Series

(2280 Form-factor )

( Gen-3 x 4 )

**Document No. :** 100-xBMDP-PXCT5

**Version No. :** 01V0

**Date :** November, 2023



The image only for reference.

ISO 9001 : 2015 CERTIFIED



### Product Features

#### ■ Flash IC

- Kioxia **BiCS-5** 3D-TLC, Toggle 3.0
- Kioxia **BiCS FLASH™** \*3
- KIOXIA **BiCS-5** 3D-NAND Flash w/aSLC Technology.

#### ■ Compatibility

- PCIe Gen 3 x4 compatible to PCIe Gen 2 and Gen 1
- NVMe Express™ 1.3d Standard.
- PCI Express® Base Specification Rev 3.1

#### ■ Additional Capabilities

- S.M.A.R.T.\*1 (Self-Monitoring, Analysis and Reporting Technology) feature set support.
- Thermal Monitor for SSD's temperature.
- End to end data path protection
- Static and Dynamic wear-leveling algorithm.
- Over-Provision
- Hardware Low Density Parity Check Code, LDPC support.
- Support of **TCG OPAL** (Optional)\*3

#### ■ Mechanical

- PCI Gen3 x 4 NVMe interface(2280)
- M.2 keying notches in **M** positions.
- **Dimension: 2280-S2-M**  
**Single Side:** 80.0 mm x 22.0 mm x 2.15mm

#### ■ Power Management

- Operating Voltage 3.3V(+/-) 5%
- Active Read (Typ.) < 4,000mW
- Active Write (Typ.) < 4,000mW
- Idle < 1,500mW

#### ■ Performance (Maximum value) \*2

- Sequential Read: 2,450.0 MB/sec. (max.)
- Sequential Write: 1,900.0 MB/sec. (max.)
- 4KB Random Read: 250K IOPS. (max.)
- 4KB Random Write: 420K IOPS. (max.)

#### ■ Capacity

- **3D NAND** : 128GB, 256GB, 512GB, 1TB, 2TB
- **3D aSLC** : 32GB, 64GB, 128GB, 256GB, 512GB

#### ■ Reliability

- **TBW:** (Client workload by JESD-219A)  
**3D NAND** : Up to 2,400 TBW at 2TB Capacity.  
**3D aSLC** : Up to 8,000 TBW at 512GB Capacity.
- **MTBF:** > 2,000,000 hours.
- **UBER:** < 1 sector per 10<sup>16</sup> bits read.
- **ECC:** Designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding.
- **Temperature:** (Operating)  
Standard Grade: 0°C ~ +70°C  
Wide Temp. Grade: -40°C ~ +85°C
- **Vibration:** 80Hz~2000Hz/20G.
- **Shock:** 0.5ms, 1500 G, 3 axes

#### ■ Certifications and Declarations

- **Certifications:** CE & FCC
- **Declarations:** RoHS & REACH


#### Remarks:

1. Support official S.M.A.R.T. Utility.
2. IOMeter, 1GB range, 4K data size, QD=128;  
CrystalDiskMark 7.0.0, 1GB range, QD=16
3. **TCG OPAL: Optional;** requires third-party software management from customer's system.
4. **BiCS** means Bit Cost Scalable Technology.  
**BiCS FLASH** is a trademark of KIOXIA Corporation.


### Order Information

#### I. Part Number List

##### ◆ APRO (BiCS-5 3D NAND) M.2-2280 Form-factor PCIe NVMe SSD PHANES-X Series

<i>Product Picture</i>	<i>Grade</i>	<i>Standard grade (0°C ~ 70°C)</i>	<i>Wide Temp. grade (-40°C ~ +85°C)</i>
 <p>The image only for reference.</p>	<b>128GB</b>	SBMDP128G-PXCT58M	WBMDP128G-PXCT58M-C
	<b>256GB</b>	SBMDP256G-PXCT58M	WBMDP256G-PXCT58M-C
	<b>512GB</b>	SBMDP512G-PXCT58M	WBMDP512G-PXCT58M-C
	<b>1TB</b>	SBMDP001T-PXCT58M	WBMDP001T-PXCT58M-C
	<b>2TB</b>	SBMDP002T-PXCT58M	WBMDP002T-PXCT58M-C

##### ◆ APRO (BiCS-5 3D aSLC) M.2-2280 Form-factor PCIe NVMe SSD PHANES-X Series

<i>Product Picture</i>	<i>Grade</i>	<i>Standard grade (0°C ~ 70°C)</i>	<i>Wide Temp. grade (-40°C ~ +85°C)</i>
 <p>The image only for reference.</p>	<b>32GB</b>	SBMDP032G-PXCT5AS8M	WBMDP032G-PXCT5AS8MC
	<b>64GB</b>	SBMDP064G-PXCT5AS8M	WBMDP064G-PXCT5AS8MC
	<b>128GB</b>	SBMDP128G-PXCT5AS8M	WBMDP128G-PXCT5AS8MC
	<b>256GB</b>	SBMDP256G-PXCT5AS8M	WBMDP256G-PXCT5AS8MC
	<b>512GB</b>	SBMDP512G-PXCT5AS8M	WBMDP512G-PXCT5AS8MC

### II. Part Number Decoder:

**X1 X2 X3 X4 X5 X6 X7 X8 X9** — **X11 X12 X13 X14 X15 X16 X17 X18 X19 X20**

**X1** : Grade

**S**: Standard Grade – operating temp. 0° C ~ 70 ° C

**W**: Wide Temp. Grade – operating temp. -40° C ~ +85 ° C

**X2** : The material of case

**B** : Bare PCBA w/o Casing

**X3 X4 X5** : Product category

**MDP**: M.2 PCIe NVMe SSD

**X6 X7 X8 X9** : Capacity

<b>032G:</b>	<b>32GB</b>	<b>512G:</b>	<b>512GB</b>
<b>064G:</b>	<b>64GB</b>	<b>001T:</b>	<b>1TB</b>
<b>128G:</b>	<b>128GB</b>	<b>002T:</b>	<b>2TB</b>
<b>256G:</b>	<b>256GB</b>		

**X11** : Controller

**P** : PHANES Series

**X12** : Controller version

**A, B, C.....**

**X13** : Controller Grade

**C** : Commercial grade

**X14 X15**: Flash IC grade / Type

**T** : KIOXIA 3D NAND Flash IC.

**5** : BiCS-5 Generation.

**X16 X17 X18 X19**: Form-Factor

**AS** : KIOXIA 3D NAND Flash IC w/aSLC Technology.

**8**: 2280 Type

**M**: with the notches in M positions

**X20**: Reserved for specific requirement

**C** : Conformal coating (optional)

### **Revision History**

Revision	Description	Date
1.0	Initial release.	2023/11/21

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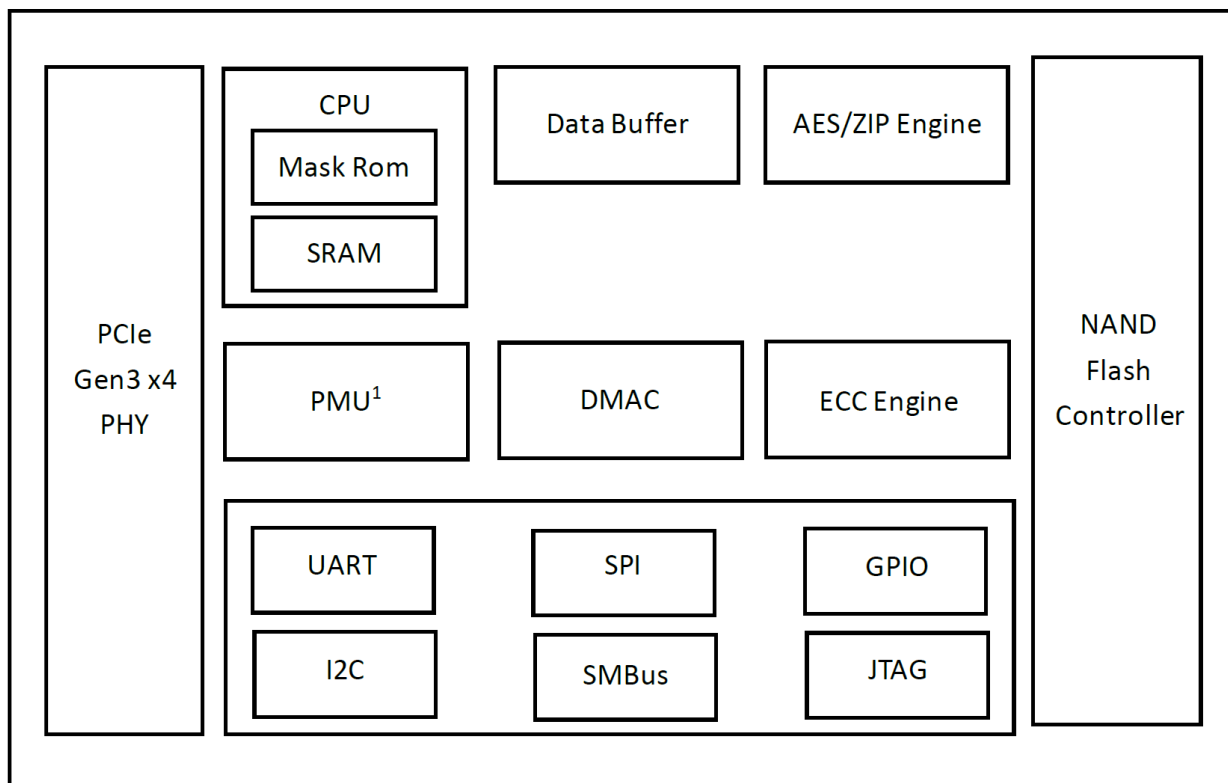
### 1. Introduction

APRO (BiCS-5 3D NAND) PCIe NVMe SSD PHANES-X Series provides high capacity flash memory Solid State Drive (SSD) that electrically complies with NVMe Express™ 1.3d Standard and support PCI Gen3 x 4 NVMe interface with high performance. The available disk capacities are from 128GB up to 2TB for **Kioxia BiCS5 3D NAND** solution, the capacities from 32GB to 512GB are the **Kioxia BiCS5 aSLC mode solution**. The operating temperature grade is optional for Standard grade 0°C ~ 70°C and Wide Temp. Grade with conformal coating supports -40°C ~ +85°C.

APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series comes with M positions and supports up to 3 PCI Express lanes. APRO's PHANES-X Series (BiCS-5 3D NAND) M.2 PCIe NVMe SSD provides the ultra-high random speed but in low power consumption. It is the most favorable solution for heavy-loading embedded systems or server computing with space limitation. The data transfer performance of 4K random read is 250K IOPS and the 4K random write is up to 420K IOPS; the sequential read is up to 2,450 MB/sec, and the sequential write is up to 1,900 MB/sec. test by a 512GB capacity 2280 M.2 SSD.

The powerful controller provides LDPC (Low Density Parity Check) to detect eventual errors while writing and increases the reliability in comparison to a standard ECC mechanism.

APRO's sophisticated S.M.A.R.T. tool is available for customers' request. It is able to monitor the health status of the PHANES-X Series (BiCS-5 3D NAND) PCIe NVMe SSD. The optional product with "Thermal Sensor" function, the user may detect its operating temperature by the S.M.A.R.T. tool whenever the SSD is operating. Currently, the S.M.A.R.T. tool is only for Windows OS based systems.



**NOTES:**

PMU: Power Management Unit

**Figure 1: APRO 3D NAND M.2 PCIe NVMe SSD PHANES-X Series Controller block diagram**

### 1.1. Scope

This document describes features, specifications and installation guide of APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

### 1.2. Flash Management Technology – Static & Dynamic Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both wear-leveling algorithms, the life expectancy of the NAND flash are greatly improved, as dynamic and also static data is shifted, if necessary, in order to guarantee an evenly use of all flash cells.

### 1.3. Bad Block Management

#### ➤ Early Bad Block

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

#### ➤ Later Bad Block

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Later Bad Block.

**Bad block management** is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

### 1.4. 3D-NAND Flash

3D NAND is a vertical implementation of the NAND flash cell memory array. The memory cell transistors forming the NAND string are connected in a series vertically and the memory transistors are changed from the floating-gate type to a trapped charge type.

In floating-gate technology, die density is increased by shrinking peripheral circuits and active circuits.

With 3D, holding the X/Y dimension of the die constant, die density is increased through multiple layers of the active circuits on the Z axis. Higher-density 3D NAND die enables applications needing high-density NAND chip solutions.



### 1.5. **Error Correcting Coding (ECC)**

APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series to read or write blocks of memory. A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC). APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

### 1.6. **Over-Provision**

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

### 1.7. **Thermal Throttling**

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series is designed with an on-die thermal sensor and with its accuracy; firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

### 1.8. **TCG Opal 2.0 (Optional, Not Default Function)**

- **Deploy Storage Device & Take Ownership:** The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- **Activate or Enroll Storage Device:** LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- **Lock & Unlock Storage Device:** unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- **Repurpose & End-of-Life:** erasure of data within one or more.

### 1.9. **SSD Lifetime Management Terabytes Written (TBW)**

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

$$\text{TBW} = [(\text{NAND Endurance}) \times (\text{SSD Capacity})] / \text{WAF}$$

**NAND Endurance:** NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

**SSD Capacity:** The SSD capacity is the specific capacity in total of a SSD.

**WAF:** Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 219 workload.

### 1.10. UBER

**Table 1: UBER Calculation.**

Capacity	UBER
32GB	< 1 sector per 10 <sup>16</sup> bits read
64GB	
128GB	
256GB	
512GB	
1TB	
2TB	

**Notes:**

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.
2.  $UBER = FER \text{ (fail rate)} / \text{Data Size (user data bit)}$
3.  $FER = \text{uncorrectable ECC frame number} / \text{total ECC frame number}$
4. LDPC for Kioxia 3D aSLC ECC capability > 120bit/KB.

### 1.11. MTBF

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

**Table 2: MTBF Calculation.**

Capacity	MTBF
32GB	2million hours
64GB	
128GB	
256GB	
512GB	
1TB	
2TB	

### 1.12. 3D NAND Flash w/ aSLC Technology

3D aSLC can be considered as an extended version of aSLC. While aSLC does Full Sequence Programming into 8 Vth distributions, 3D aSLC only does lower page programming into 2 Vth distributions. Accordingly, because only Lower pages are programmed, 3D aSLC provides better performance and endurance than aSLC. Moreover, 3D aSLC performs similarly with SLC, yet 3D aSLC is more cost-effective

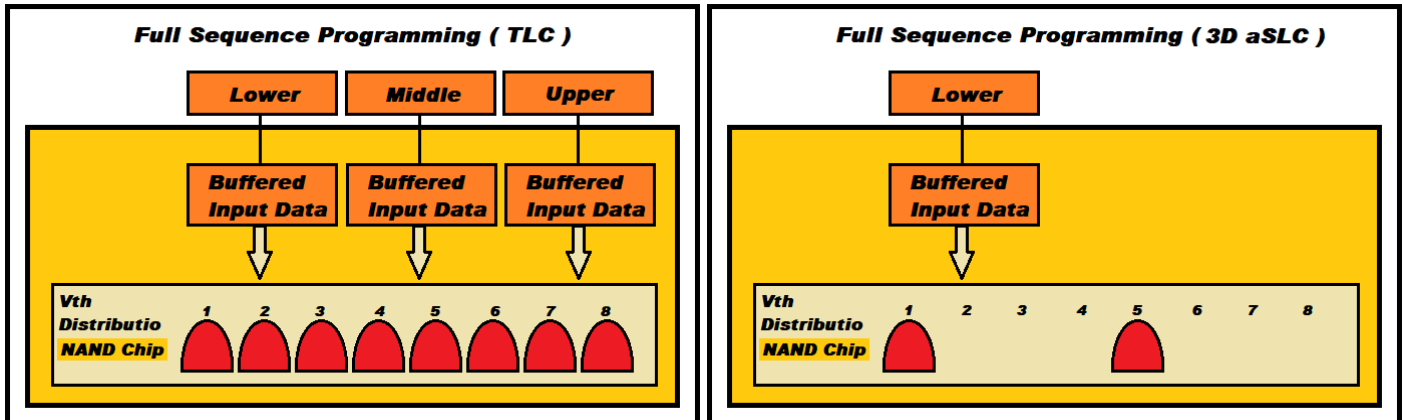


Figure 2: 3D aSLC mode.

## 2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

### 2.1. System Environmental Specifications

Table 3: Environmental Specification

APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series		Standard grade	Wide Temp. grade
Temperature	Operating:	0°C ~ +70°C	-40°C ~ +85°C
	Non-operating:	-40°C ~ +85°C	-50°C ~ +95°C
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
	Frequency/Acceleration:	80Hz~2000Hz/20G.	
Shock	Operating & Non-operating:	0.5ms, 1500 G, 3 axes	
Electrostatic Discharge (ESD)	Temperature:	24°C	
	Relative Humidity:	51%	
	+/-4KV:	Device functions are affected, but EUT will be back to its normal or operational state automatically.	

### 2.2. System Power Requirements

**Table 4: Power Requirement**

APRO (BiCS-5 3D NAND) M.2-2280 Form-factor PCIe NVMe PHANES-X Series			
<b>Operating Voltage</b>		Min = 3.14V / Max = 3.47 V	
<b>Rise Time (Max/Min)</b>		100 ms / 0.1 ms	
<b>Fall Time (Max/Min)</b>		5 s / 1 ms	
<b>Min. Off Time1</b>		1 s	
<b>Power Consumption</b>		Read (W)	Writing (W)
<b>Capacity</b>	<b>128GB</b>	2.0	1.6
	<b>256GB</b>	3.0	2.2
	<b>512GB</b>	3.1	3.0
	<b>1TB</b>	3.3	3.2
	<b>2TB</b>	3.5	3.4
APRO (BiCS-5 3D aSLC) M.2-2280 Form-factor PCIe NVMe PHANES-X Series			
<b>Capacity</b>	<b>32GB</b>	3.3	1.9
	<b>64GB</b>	3.6	2.7
	<b>128GB</b>	3.6	3.3
	<b>256GB</b>	3.8	3.7
	<b>512GB</b>	3.9	3.8

**Note:**

1. Minimum time between power removed from SSD ( $V_{cc} < 100$  mV) and power re-applied to the drive.
2. Ensure the voltage of each power domain in SSD has enough time to discharge less than 0.1V.
3. Rise Time during from 10% to 90% of 3.3V.
4. Fall Time during from 90% to 10% of 3.3V.
5. Use CrystalDiskMark6.0.0 with the setting of 1GB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
6. The measured power voltage of SSD is 3.3V.
7. Power consumption may differ according to flash configuration, use condition, environment and platform configuration.
8. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH.

### 2.3. System Performance

**Table 5: System Performances**

Data Transfer Mode supporting		Serial ATA Gen-III (6.0Gb/s = 768MB/s)			
Capacity	Flash Structure	Sequential (MB/s)		4K Random (IOPS)	
		Read	Write	Read	Write
<b>BiCS-5 3D NAND</b>					
128GB	128GB x 1, Kioxia 112L 3D TLC	1,100	550	95K	125K
256GB	256GB x 2, Kioxia 112L 3D TLC	2,300	1,100	160K	240K
512GB	256GB x 2, Kioxia 112L 3D TLC	2,400	1,700	230K	400K
1TB	256GB x 4, Kioxia 112L 3D TLC	2,450	1,900	270K	420K
2TB	512GB x 4, Kioxia 112L 3D TLC	2,100	1,800	270K	420K
<b>BiCS-5 3D NAND aSLC mode</b>					
32GB	64GB x 2, Kioxia 112L 3D TLC	1,150	550	90K	120K
64GB	128GB x 2, Kioxia 112L 3D TLC	2,300	1,100	160K	230K
128GB	128GB x 4, Kioxia 112L 3D TLC	2,400	1,800	230K	370K
256GB	256GB x 4, Kioxia 112L 3D TLC	2,450	1,900	270K	420K
512GB	512GB x 4, Kioxia 112L 3D TLC	2,450	1,900	250K	420K

**Note:**

1. Performance may differ according to flash configuration, use condition, environment and platform.
2. Tested with CrystalDiskMark 6.0, QD32T1, 1GB range.
3. Performance specification is under Thermal Throttling inactivated.
4. Operating System: Windows 10 Professional (x64), Version 1809
5. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.

### 2.4. System Reliability

**Table 6: System Reliability**

<b>Wear-leveling Algorithms</b>		Static and Dynamic wear-leveling algorithms			
<b>Bad Block Management</b>		Supportive			
<b>ECC Technology</b>		Hardware design LDPC (Low Density Parity Check)			
<b>Erase counts</b>		NAND 3D NAND aSLC Flash Cell Level : 30K P/E Cycles			
<b>TBW (Tera Bytes Written)</b>		<b>3D NAND</b>		<b>3D aSLC</b>	
		<b>TBW</b>	<b>DWPD</b>	<b>TBW</b>	<b>DWPD</b>
<b>Capacity</b>	<b>32GB</b>	N/A	N/A	500	N/A
	<b>64GB</b>	N/A	N/A	1,000	N/A
	<b>128GB</b>	110	0.78	2,000	N/A
	<b>256GB</b>	240	0.85	4,000	N/A
	<b>512GB</b>	520	0.92	8,000	N/A
	<b>1TB</b>	1,120	0.99	N/A	N/A
	<b>2TB</b>	2,400	1.07	N/A	N/A

**Note:**

1. TBW is measured by JEDEC Client 219A workload and calculated with PE count = 30,000.
2. TBW may differ according to flash configuration and platform configuration.
3. The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected.  
(Like certain Windows OS, Linux kernel version before 2.6.33, other OS please reference each own user manual)
4. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

### 2.5. System Capacity

**Table 7: User Capacity and Addressable Sectors**

<b>BiCS-5 3D NAND</b>				
<b>Capacity</b>	<b>512Bytes/Sector</b>		<b>4KBytes/Sector</b>	
	<b>Number of Total LBA</b>	<b>User Available Bytes</b>	<b>Number of Total LBA</b>	<b>User Available Bytes</b>
<b>128GB</b>	250,069,680	128,035,676,160	31,258,710	128,035,676,160
<b>256GB</b>	500,118,192	256,060,514,304	62,514,774	256,060,514,304
<b>512GB</b>	1,000,215,216	512,110,190,592	125,026,902	512,110,190,592
<b>1024GB</b>	2,000,409,264	1,024,209,543,168	250,051,158	1,024,209,543,168
<b>2048GB</b>	4,000,797,360	2,048,408,248,320	500,099,670	2,048,408,248,320
<b>32GB</b>	62,533,296	32,017,047,552	7,816,662	32,017,047,552
<b>64GB</b>	125,045,424	64,023,257,088	15,630,678	64,023,257,088
<b>128GB</b>	250,069,680	128,035,676,160	31,258,710	128,035,676,160
<b>256GB</b>	500,118,192	256,060,514,304	62,514,774	256,060,514,304
<b>512GB</b>	1,000,215,216	512,110,190,592	125,026,902	512,110,190,592

### Notes:

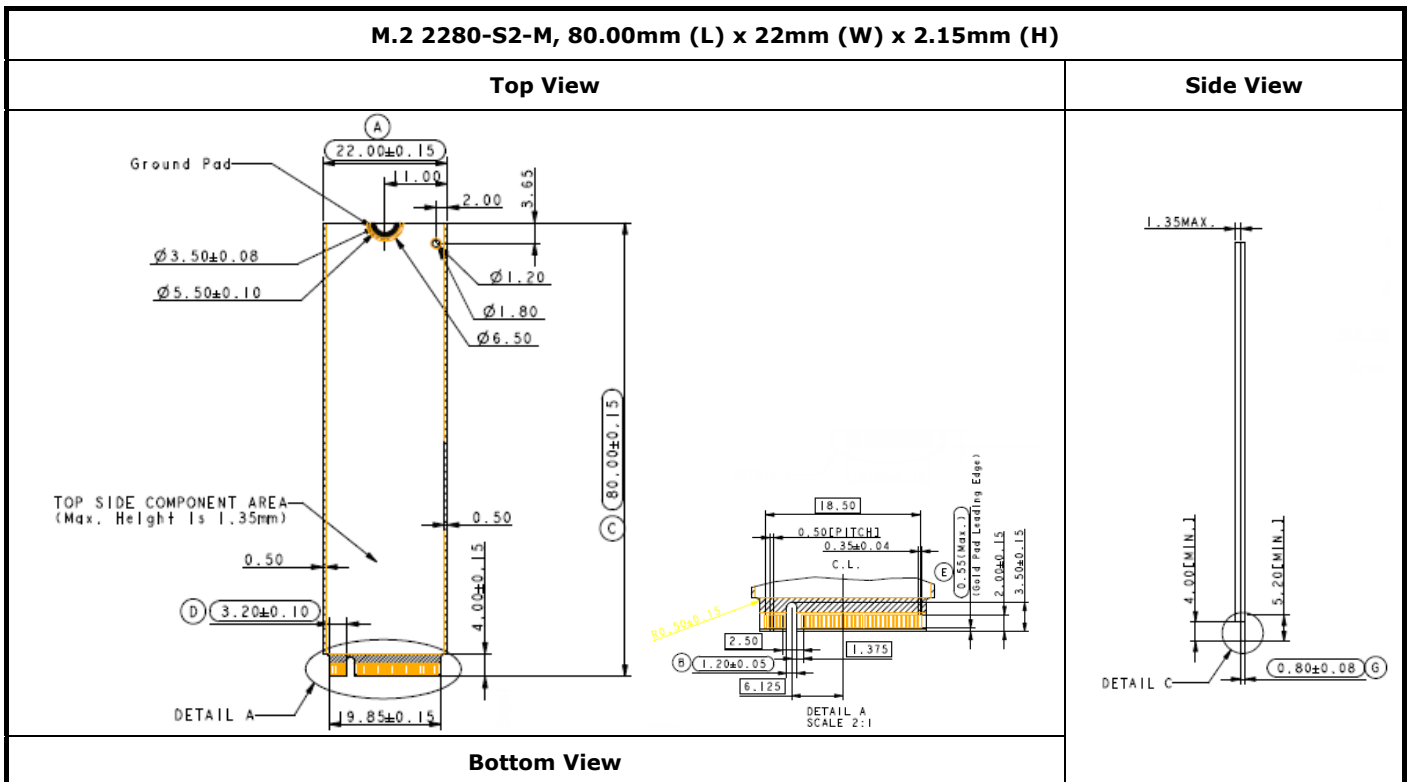
- 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes.
- The calculation is following IDEMA Standard.
- The total actual user usable capacity of the SSD may be less than device capacity due to SSD format, SSD partition, operating system. EX: OS shows 238.47GB (NTFS) with 256GB SSD.

## 2.6. Physical Specifications

Refer to Table 5 and see Figure 2 for 3D NAND/3D aSLC M.2-2280 Form-factor PCIe NVMe SSD PHANES-X Series physical specifications and dimensions.

**Table 8: Physical Specifications**

<b>Form-factor</b>	2280-S2-M
<b>Length:</b>	80.0 mm
<b>Width:</b>	22.0 mm
<b>Thickness</b>	2.15 mm
<b>Weight:</b>	8.0 g



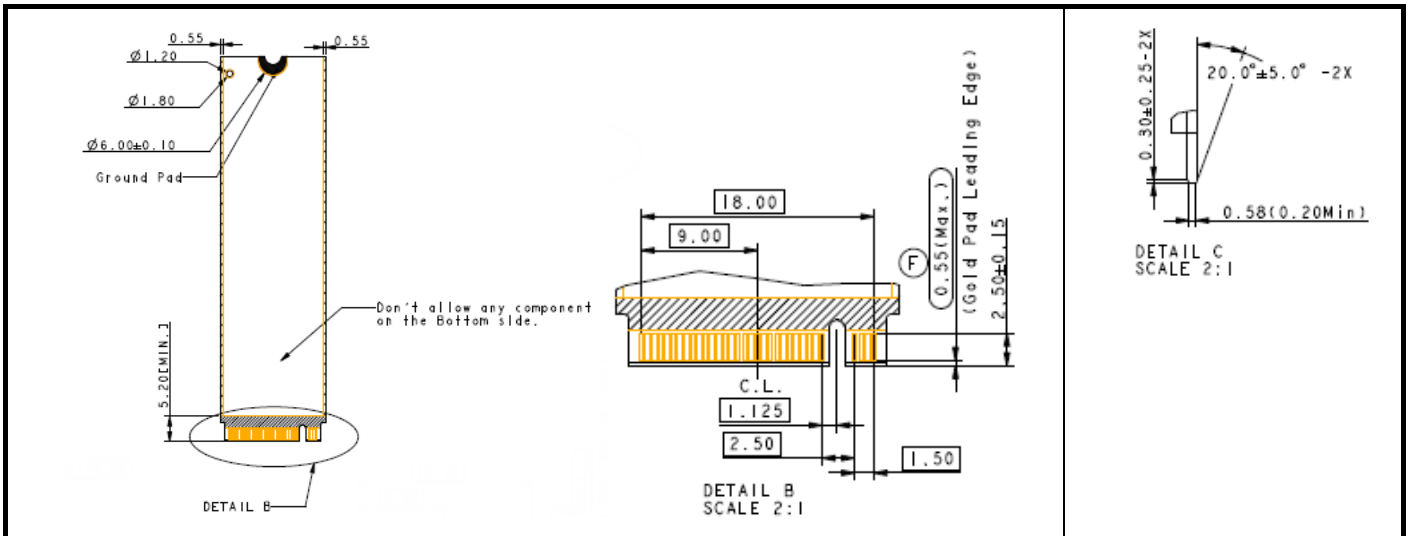


Figure 3: APRO (BiCS-5 3D NAND) M.2-S2-2280 Form-factor

### 3. Interface Description

#### 3.1. M Key M.2 SSD Assembly Precautions

M Key M.2 SSD is only compatible to M Key socket. As shown in Use Case 2, misuse may cause severe damages to SSD including burn-out.

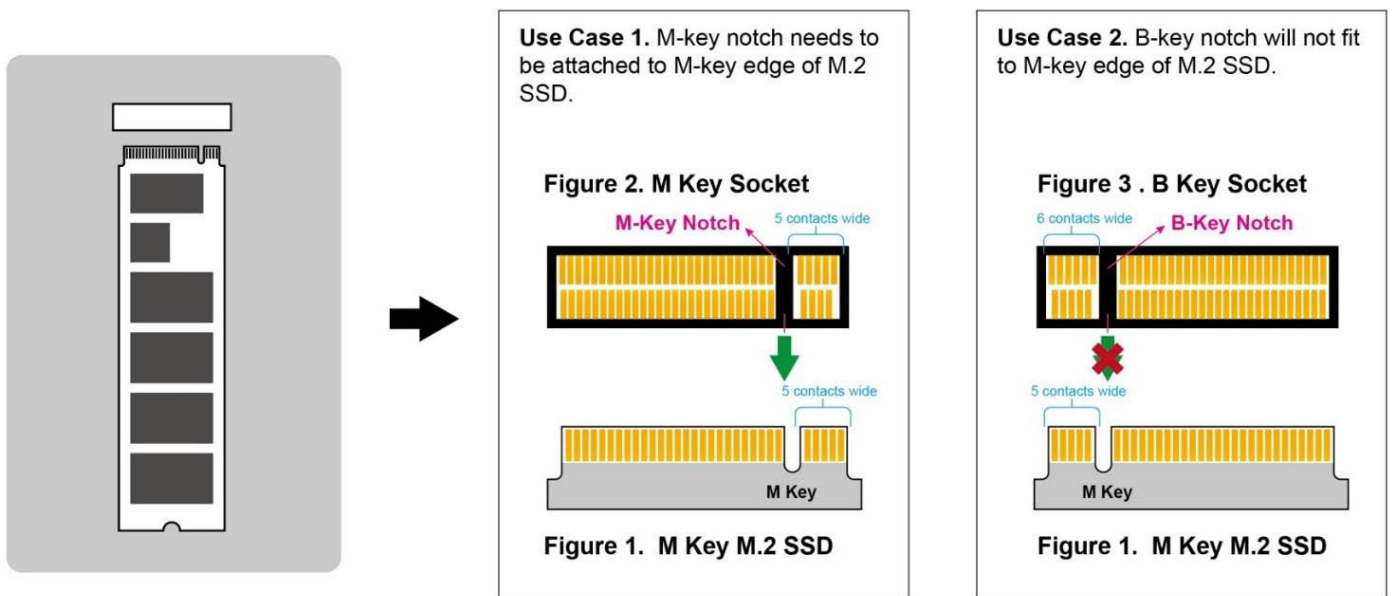


Figure 4: M Key M.2 Assembly Precautions



### 4.1. Pin Assignments

Pin Assignment and Description of APRO (BiCS-5 3D NAND) M.2 PCIe NVMe SSD PHANES-X Series

**Table 9 - Pin Assignments**

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec

32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	

61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No connect
68	N/C	No connect
69	N/C	PEDET (NC-PCIe)
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

### **Appendix A: Limited Warranty**

APRO warrants your 3D NAND/3D aSLC M.2-2280 Form-factor PCIe NVMe SSD PHANES-X Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

**BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.**

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

#### **WARRANTY PERIOD:**

- **3D NAND FLASH (Wide Temp. Grade ) 2 years / Within 3K Erasing Counts**
- **3D aSLC (Wide Temp. Grade ) 2 years / Within 30K Erasing Counts**

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