APRO Co., Ltd.

3D NAND Flash

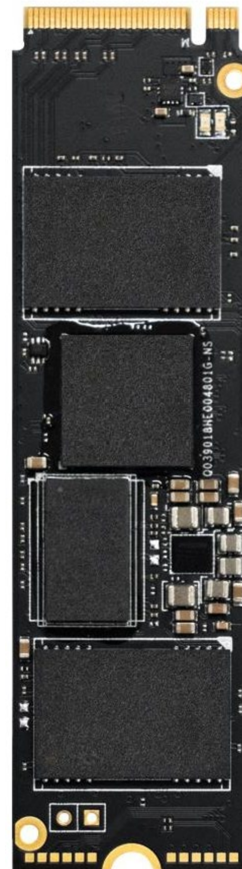
(KIOXIA BiCS5)

M.2 PCIe NVMe SSD

PHANES-V Series

(2280 Form-factor)

(Gen-4 x 4)



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ISO 9001 : 2015 CERTIFIED

Product Features

- **Flash IC**
  - KIOXIA BiCS5 3D-NAND Flash IC.
  - KIOXIA **BiCS FLASH™ *3**

- **Compatibility**
  - PCIe Gen4x4
  - NVMe 1.4
  - PCI Express Base 4.0

- **Additional Capabilities**
  - S.M.A.R.T.***1** (Self-Monitoring, Analysis and Reporting Technology) feature set support.
  - Thermal Monitor for SSD's temperature.
  - End to end data path protection
  - Static and Dynamic wear-leveling algorithm.
  - Over-Provision
  - Hardware Low Density Parity Check Code, LDPC support.
  - Support of **TCG OPAL** (Optional)***4**

- **Mechanical**
  - PCI Gen4 x 4 NVMe interface(2280)
  - M.2 keying notches in **M** positions.
  - **Dimension: M.2 2280-D2-M-H2:** (8.0g)
    480GB,960GB,1920,3840GB
    Double Side: 80.0 mm x 22.0 mm x 1.35mm

- **Power Management: OP. Voltage 3.3V(+/-) 5%**
  - Read Mode: 10.9W (3,840GB.)
  - Write Mode: 11.0W (3,840GB.)
  - Idle Mode: 2,000Mw (3,840GB.)

- **Performance (Maximum value) *2, 3**
  - **2280:**
  - Sequential Read: 7,200.0 MB/sec. (2TB.)
  - Sequential Write: 1,200.0 MB/sec. (2TB.)
  - 4KB Random Read: 580K IOPS.
  - 4KB Random Write: 200K IOPS.

- **Capacity**
  - **2280-D2-M-H2:**
    480GB, 960GB, 1,920GB, 3,840GB

- **Reliability**
  - **TBW:** Up to 6,800 TBW at 3840GB Capacity.
    (Client workload by JESD-219A)
  - **MTBF: >** 1,500,000 hours.
  - **UBER:** < 1 sector per 10^{16} bits read.
  - **ECC:** Designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding.
  - **Temperature:**
    Operating Temp.: 0ºC ~ +70ºC
    Storage Temp.: -40ºC ~ +85ºC
  - **Vibration:** 80Hz~2000Hz/20G.
  - **Shock:** 0.5ms, 1500 G, 3 axes

- **Certifications and Declarations**
  - **Certifications**: CE & FCC
  - **Declarations**: RoHS & REACH
  -

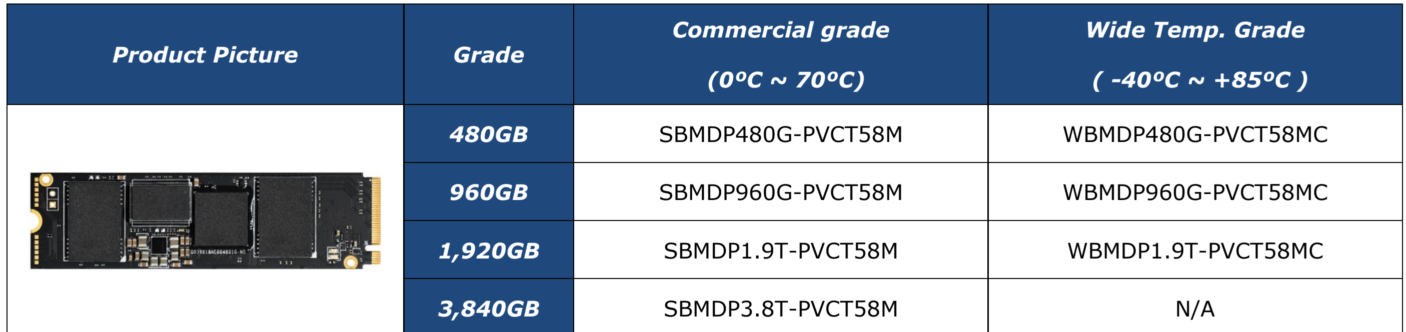
Remarks:

1. Support official S.M.A.R.T. Utility.
2. IOMeter, 1GB range, 4K data size, QD=128, 16 worker, 4k aligned
3. CrystalDiskMark 7.0.0, 1GB range, QD=16, Thread=1
4. **TCG OPAL: Optional (Different F/W);** requires third-party software management from customer's system.

Order Information

I. Part Number List

◆ **APRO 3D NAND TLC M.2-2280 Form-factor PCIe NVMe SSD PHANES-V Series**



Product Picture	Grade	Commercial grade (0ºC ~ 70ºC)	Wide Temp. Grade (-40ºC ~ +85ºC)
	480GB	SBMDP480G-PVCT58M	WBMDP480G-PVCT58MC
	960GB	SBMDP960G-PVCT58M	WBMDP960G-PVCT58MC
	1,920GB	SBMDP1.9T-PVCT58M	WBMDP1.9T-PVCT58MC
	3,840GB	SBMDP3.8T-PVCT58M	N/A

II. Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9 – X11 X12 X13 X14 X15 X16 X17 X18

X1 : Grade

S: Standard Grade – operating temp. 0º C ~ 70 º C

X2 : The material of case

B : Bare PCBA w/o Casing

X3 X4 X5 : Product category

MDP: M.2 PCIe NVMe SSD

X6 X7 X8 X9 : Capacity

480G	480GB	**1.92T**	1,920GB
960G:	960GB	**3.84T**	3,840GB

X11 : Controller

P : PHANES Series

X12 : Controller version

A, B, C.....

X13 : Controller Grade

C : Commercial grade

X14 : Flash IC

T : KIOXIA NAND Flash IC

X15 : Flash IC grade / Type

5 : KIOXIA BiCS5 3D-NAND Flash IC

X16 X17: Form-Factor

8: 2280 Type

M: with the notches in M positions

X18 X19 X20: Reserved for specific requirement

C : Conformal coating

TG: TCG Opal 2.0 **(Optional)**

Revision History

Revision	Description	Date
1.0	Initial release.	2022/11/16

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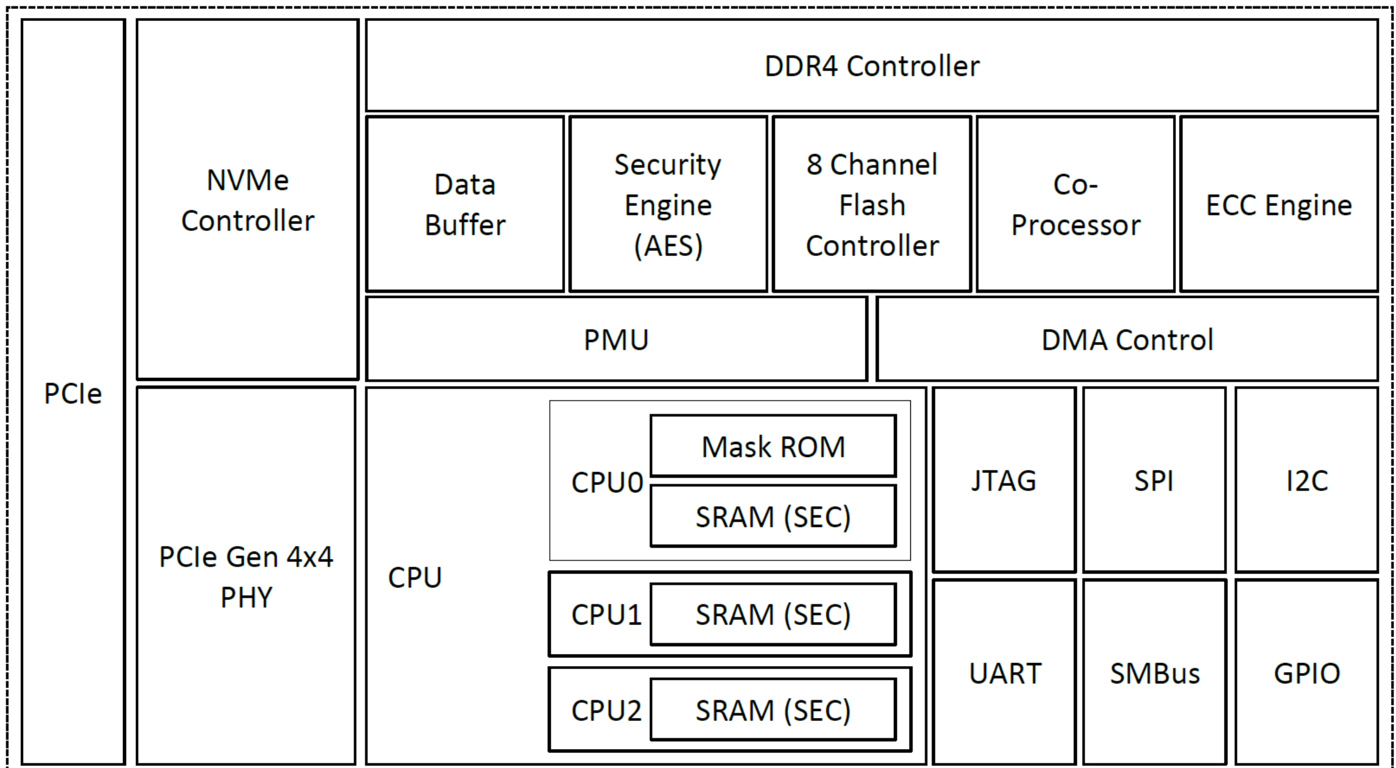
1. Introduction

APRO 3D NAND TLC PCIe NVMe SSD PHANES-V Series provides high capacity flash memory Solid State Drive (SSD) that electrically complies with NVM Express[TM] 1.4 Standard and support PCI Gen4 x 4 NVMe interface with high performance. The PHANES-V Series M.2 2280 SSD available disk capacities are 480GB, 960GB, 1,920GB and 3,840G; the operating temperature range is 0°C ~ +70°C and wide temp. -40°C ~ +85°C.

APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series comes with M positions and supports up to 4 PCI Express lanes. APRO's PHANES-V Series 3D NAND TLC M.2 PCIe NVMe SSD provides the ultra-high random speed but in low power consumption. It is the most favorable solution for heavy-loading embedded systems or server computing with space limitation. The data transfer performance of 4K random read is 580K IOPS and the 4K random write is up to 200K IOPS; the sequential read is up to 72,000 MB/sec, and the sequential write is up to 1,200 MB/sec. test by a 3,840GB capacity 2280 M.2 SSD.

The powerful controller provides LDPC (Low Density Parity Check) to detect eventual errors while writing and increases the reliability in comparison to a standard ECC mechanism.

APRO's sophisticated S.M.A.R.T. tool is available for customers' request. It is able to monitor the health status of the PHANES-V Series 3D NAND TLC PCIe NVMe SSD. The optional product with "Thermal Sensor" function, the user may detect its operating temperature by the S.M.A.R.T. tool whenever the SSD is operating. Currently, the S.M.A.R.T. tool is only for Windows OS based systems.



NOTES:

1.PMU: Power Management Unit

2.SEC: Single Bit Error Correct

Figure 1: APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series Controller block diagram

1.1. *Scope*

This document describes features, specifications and installation guide of APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *Flash Management Technology – Static & Dynamic Wear Leveling*

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both wear-leveling algorithms, the life expectancy of the NAND flash are greatly improved, as dynamic and also static data is shifted, if necessary, in order to guarantee an evenly use of all flash cells.

1.3. *Bad Block Management*

- **Early Bad Block**

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

- **Later Bad Block**

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Later Bad Block.

Bad block management is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

1.4. *3D-NAND Flash*

3D NAND is a vertical implementation of the NAND flash cell memory array. The memory cell transistors forming the NAND string are connected in a series vertically and the memory transistors are changed from the floating-gate type to a trapped charge type.

In floating-gate technology, die density is increased by shrinking peripheral circuits and active circuits.

With 3D, holding the X/Y dimension of the die constant, die density is increased through multiple layers of the active circuits on the Z axis. Higher-density 3D NAND die enables applications needing high-density NAND chip solutions.

1.5. *Error Correcting Coding (ECC)*

APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series to read or write blocks of memory. A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC). APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

1.6. *Over-Provision*

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.7. *Thermal Throttling*

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series is designed with an on-die thermal sensor and with its accuracy; firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

1.8. *TCG Opal 2.0 (Optional)*

- AES 256-bitHardware Self Encryption
- Deploy Storage Device & Take Ownership: The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device’s owner credential.
- Activate or Enroll Storage Device: LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device: unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life: erasure of data within one or more.

1.9. *UBER*

Table 1: UBER Calculation.

Capacity	UBER
480GB	< 1 sector per 10^{16} bits read
960GB	
1,920GB	
3,840GB	

Notes:

- *UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.*
- *UBER = FER (fail rate)/ Data Size (user data bit)*
- *FER = uncorrectable ECC frame number / total ECC frame number*
- *LDPC for Kioxia TLC ECC capability > 120bit/KB*

1.10. *MTBF*

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

Table 2: MTBF Calculation.

Capacity	MTBF
480GB	> 1.5 million hours
960GB	
1,920GB	
3,840GB	

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series		SBMDPxxxG-PVCT58M	WBMDPxxxG-PVCT58MC
Temperature	Operating: Non-operating:	0ºC ~ +70ºC -20ºC ~ +80ºC	-40ºC ~ +85ºC -50ºC ~ +95ºC
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
	Frequency/Acceleration:	80Hz~2000Hz/20G.	
Shock	Operating & Non-operating:	0.5ms, 1500 G, 3 axes	
Electrostatic Discharge (ESD)	Temperature:	24ºC	
	Relative Humidity:	51%	
	+/-4KV:	Device functions are affected, but EUT will be back to its normal or operational state automatically.	

2.2. System Power Requirements

Table 2: Power Requirement

APRO 3D NAND TLC M.2-2280 Form-factor PCIe NVMe PHANES-V Series				
Operating Voltage		Min = 3.14V / Max = 3.47 V		
Rise Time (Max/Min)		100 ms / 0.1 ms		
Fall Time (Max/Min)		5 s / 1 ms		
Min. Off Time1		1 s		
Power Consumption		Read (W)	Writing (W)	Idle (mW)
Capacity	*480GB*	8.8	7.5	2,000
	960GB	10.1	9.5	2,000
	1,920GB	10.6	10.5	2,000
	3,840GB	10.9	11.0	2,000

Note:

- *Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark with the conditions described in 1(B).*
- *Power consumption during read and write operation is measured on Gen4 X570 + 6 Core CPU*

2.3. *System Performance*

Table 3: System Performances

Interface		PCI Gen4 x 4 NVMe			
Form-factor		**2280**			
Utility		**CrystalDiskMark**		**IOMeter**	
Performance		**Read (MB/s)**	**Write (MB/s)**	**Read (IOPS)**	**Write (IOPS)**
Capacity	***480GB***	4,000	350	230K	90K
	960GB	7,000	750	480K	190K
	1,920GB	7,000	1,500	800K	380K
	3,840GB	7,000	1,000	580K	200K

Note:

- *Performance is measured on a fresh slave drive and based on the following conditions:*
  A. CrystalDiskMark 7.0.0, 1GB range, QD=16, Thread=1
  B. IOMeter, 1GB range, 4K data size, QD=128, 16 worker, 4k aligned
- *Performance is based on AMD Gen4 X570 + 8 Core CPU + DDR4 (3200Hz) 16GB.*

2.4. *System Reliability*

Table 4: System Reliability

Wear-leveling Algorithms		Static and Dynamic wear-leveling algorithms	
Bad Block Management		Supportive	
ECC Technology		Hardware design LDPC (Low Density Parity Check)	
Erase counts		NAND 3D NAND TLC Flash Cell Level : 3K P/E Cycles	
TBW (Tera Bytes Written)		**TBW**	**DWPD**
Capacity	***480GB***	700	1.4
	960GB	1,660	1.5
	1,920GB	3,400	1.6
	3,840GB	6,800	1.6

Note:

- *Client workload by JESD-219A. (The capacity lower than 64GB client workload is not specified in JEDEC219A, the values are estimated.)*
- *The endurance of SSD could be varying based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.*

2.5. *Physical Specifications*

Refer to Table 5 and see Figure 2 for 3D NAND TLC M.2-2280 Form-factor PCIe NVMe SSD PHANES-V Series physical specifications and dimensions.

Table 5: Physical Specifications

Form-factor	2280-D2-M / 80.00mm (L) x 22mm (W) x 1.35mm (H)
Length:	80.0 mm
Width:	22.0 mm
Thickness	1.35 mm
Weight:	10.0 g

Figure 2: APRO 3D NAND TLC M.2-S2-2280 Form-factor

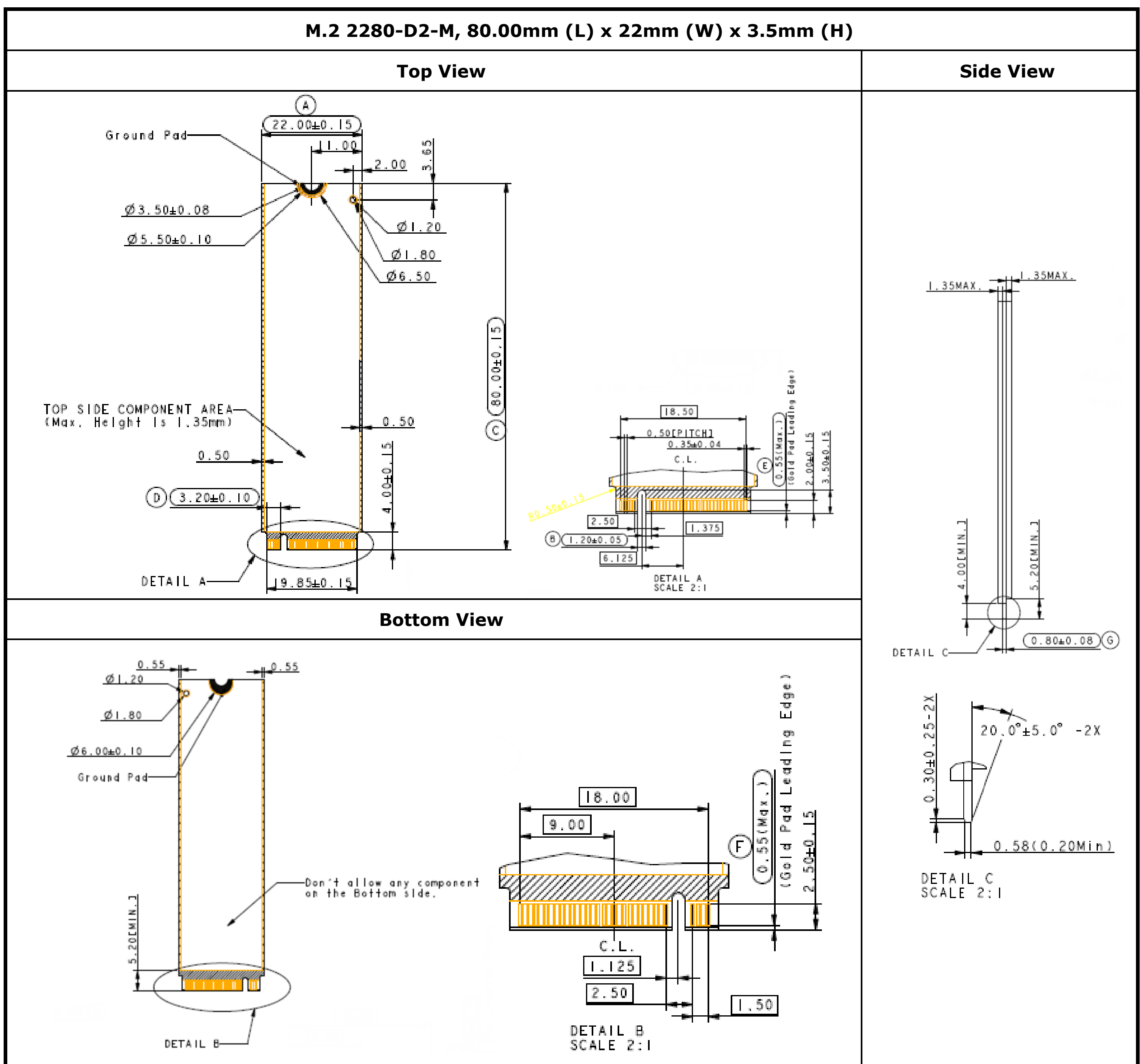


Figure 3: APRO 3D NAND TLC M.2-D2-2280 Form-factor

3. Interface Description

3.1. M Key M.2 SSD Assembly Precautions

M Key M.2 SSD is only compatible to M Key socket. As shown in Use Case 2, misuse may cause severe damages to SSD including burn-out.

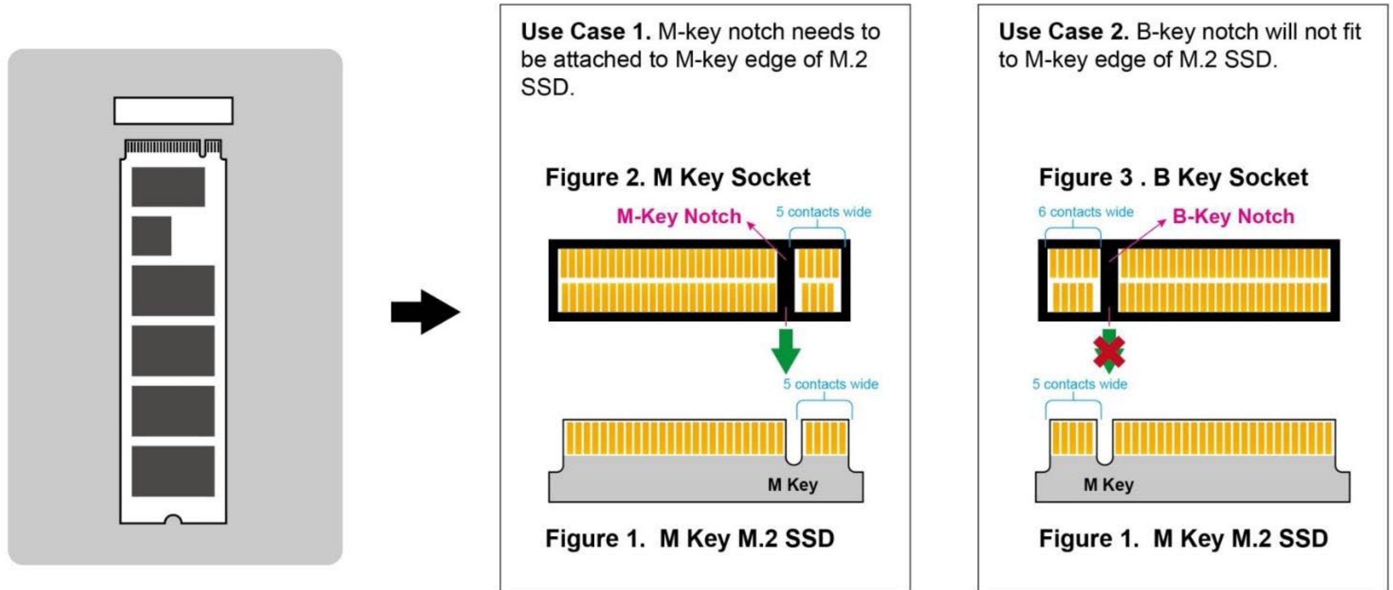


Figure 4: M Key M.2 Assembly Precautions

4.1. Pin Assignments

Pin Assignment and Description of APRO 3D NAND TLC M.2 PCIe NVMe SSD PHANES-V Series

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground

16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground

52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No connect
68	N/C	No connect
69	N/C	PEDET (NC-PCIe)
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

Table 6 - Pin Assignments

Appendix A: Limited Warranty

APRO warrants your 3D NAND TLC M.2-2280 Form-factor PCIe NVMe SSD PHANES-V Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **3D NAND TLC (Standard grade / Wide temp. grade) 2 years / Within 3K Erasing Counts**

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