VP460

6U VPX Direct RF Processing System with Xilinx Zynq Ultrascale+ RFSoC

The VP460 is a 6U VPX RF processing system featuring the transformational Xilinx® Zynq® Ultrascale+™ RF system-on-chip technology (RFSoC) and the latest Xilinx Virtex™ Ultrascale+ High Bandwidth Memory (HBM) FPGA device. The RFSoC ZU29DR device used on the VP460 includes 16 integrated analog-to-digital converters at 2GSPS, 16 digital-to-analog converters at 6.4 GSPS, a user-programmable FPGA fabric, and multi-core Zynq ARM® processing subsystem. The HBM VU37P device features the speed and capabilities of an UltraScale+ FPGA plus integrated DRAM in the FPGA package capable of up to 460GB/s data transfer rates on -chip.

Reduce RF Signal Chain Complexity

RF systems with multiple channels suffer from a cost- and complexity challenge. More channels means more expensive and large RF signal up/down conversion and signal conditioning. As a solution, the VP460 enables direct RF sampling which can be implemented in the digital domain, bringing greater flexibility to the signal processing chain. Additionally, simplified integration with RF sampling devices removes the complexity of JESD204B high speed serial interfaces.

Maximize Input/Output Channel Density

The VP460 is one of the densest 6U VPX analog FPGA carrier boards available with the ability to synchronize all 16 channels as well as multiple boards for even larger system applications. In previous generations of technology, this combination would have taken four times as many boards.

Revolutionary processing capability

The VP460 is a revolution in COTS RF and FPGA processing, perfectly balancing the need for high performance FPGA processing, the ease of a hardened embedded processor and the ultra-low latency of integrated analog interfaces. The revolutionary RF and DSP technology enables a user to create the most advanced multi-channel electronic warfare systems, radar, and SDR applications today.

Offload Data More Efficiently

The VP460 has a traditonal VPX data plane interface, allowing a x8 PCIe™ Gen3 connection to a host computer. With 16 ADCs sampling at rates up to 2GSPS with two bytes per sample, even the modern PCIe Gen 3 high speed data connection is too slow for a direct transfer. To overcome this challenge, the VP460 includes – in addition to the PCIe Gen3 data plane - up to 48 high speed serial lanes to the Xilinx Virtex Ultrascale+ HBM device supporting protocols such as PCIe Gen3, 10G Ethernet, Aurora, etc.

The VP460 is designed to be air-cooled. When paired with Abaco's extensive portfolio of multi-architecture processing boards including SBCs and GPGPUs, the state-of-the-art VP460 enables systems to be built from leading edge, interoperable components.

FEATURES:

- Dual FPGA Architecture:
  - Zynq UltraScale+ RFSoC
  - Virtex UltraScale+ HBM
- ADC 16 channels 2 GSPS 12-bit
- DAC 16 channel 6.4 GSPS 14-bit
- Independent clock generation circuit for the ADC and DAC front ends
- Application Processing Unit
  - Quad-core ARM Cortex-A53
- Real-Time Processing Unit
  - Dual-core ARM Cortex-R5
- Up to 8 GB DDR4 memory available to the RFSoC
- Up to 12 GB DDR4 memory available to the Virtex UltraScale+
  - 8 GB integrated on the device
  - Up to 460 GB/s transfer rates with integrated DRAM
- VITA 57.4 FMC+ site available to the Virtex UltraScale+ HBM
- PCIe Gen3 x 16 from HBM to the backplane and x8 from the RFSoC
- Low latency, high bandwidth parallel data bus between the Zynq UltraScale+ RFSoC and Virtex UltraScale+ HBM devices
- User I/O to backplane RTM
  - DisplayPort™ 1.2a
  - SATA 3.1
  - USB 3.0
  - Gigabit Ethernet
- Linux® and Windows® BSP available
- SOSA Backplane Option

abaco SYSTEMS

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Specifications

Processing/FPGA
- Xilinx ZU29DUR Zynq UltraScale+ RFSoC
- Xilinx VU37P Virtex UltraScale+ w/HBM

Memory
- Two 64-bit 4GBytes DDR4 (8GB total) memory blocks to RFSoC. Up to 2400 Mb/s.
- Single 64-bit 4GBytes DDR4 memory block to Virtex Ultrascale+. Up to 2400 Mb/s.
- 8GB on-chip HBM blocks inside Virtex Ultrascale+
- Block RAM and UltraRAM available inside the FPGA devices

ADC and DAC
- ADC: 16-channels, 12-bit, 2GSPS with DDC
- DAC: 16-channels, 14-bit, 6.4GSPS with DUC

Programmable FPGA Logic

RFSoC
- 930k System Logic Cells
- 425k CLB LUTs
- 4,272 DSP Slices

Virtex Ultrascale+
- 2,852k System Logic Cells
- 1,304k CLB LUTs
- 9,024 DSP Slices

Application Processing Unit
- Quad-core ARM Cortex-A53 MPCore
- Up to 1.5GHz

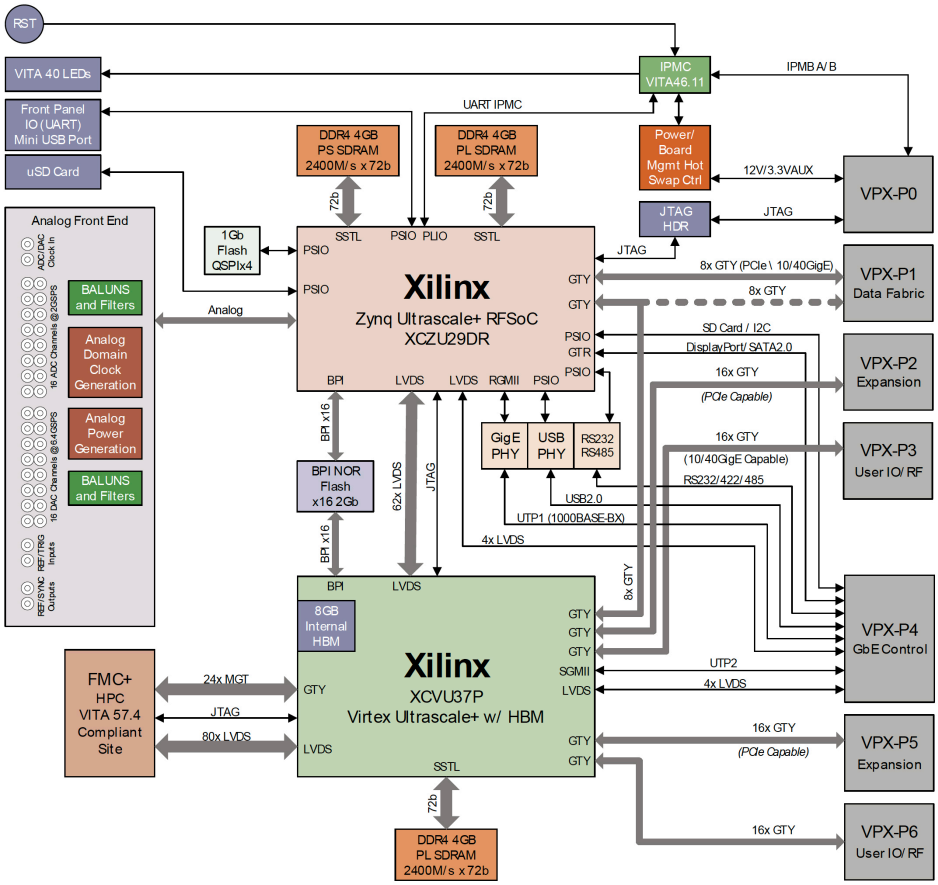
Real-time Processing Unit
- Dual-core ARM Cortex-R5 MPCore
- Up to 533MHz

Backplane Connectivity
- X16 PCIe to Virtex Ultrascale+
- X8 PCIe to RFSoC
- X16 GTY to P5
- X16 GTY to P6 and P3 each (Depopulated for SOSA aligned backplane)

Software Support
- Linux
- Windows
- VxWorks® (contact factory)

Environment
- Convection Cooled
- Operating Temperature: 0 oC to + 70oC

Block diagram



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