A5G08RC6BVQKSBV

8GB DDR5-4800 Unbuffered NON-ECC SODIMM

Datasheet

Version 1.2

CONTENT

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Revision History

Date	Version	Changes compared to previous issue
Dec. 15th, 2022	1.0	First release.
Jan. 09th, 2023	1.1	Updated Recommended DC operating conditions
Mar. 16th, 2023	1.2	Updated operating temperature section

1. Product Description

The ATP A5G08QC6BVQKSBV is a high performance 8GB DDR5-4800 Unbuffered NON-ECC SDRAM memory module. It is organized as 1024M x 64 in a 262-pin Small Outline Dual-In-Line Memory Module (SODIMM) package. The module utilizes four 1024Mx16 DDR5 SDRAMs in FBGA package. The module consists of a 1024-byte serial EEPROM, which contains the module configuration information.

2. Key Feature

- High Density: 8GB (1024M x 64)
- DIMM Rank: 1 Rank
- Cycle Time: 0.416ns (4800MHz), 0.454ns (4400MHz)
- CAS Latency: 40(DDR5-4800), 36(DDR5-4400)
- Power supply: V_{DD}= 1.1V (1.067V(- 3%) ~ 1.166V(+6%))
  V_{DDQ}= 1.1V (1.067V(- 3%) ~ 1.166V(+6%))
  V_{PP}=1.8V (1.746 (-3%) ~ 1.908 (+6%))
- PCB Height: 30.00mm (1.18 inches)
- Weight: 15 grams Max.
- JEDEC standard compliant
- On module Power Management IC (JEDEC Standard: 1.1V)
- 32 internal banks with x4/x8; 8 Bank groups ,16 internal banks with x16; 4 Bank groups
- Internal ZQ calibration via Multi-Purpose Command (MPC)
- 16bit prefetch
- Burst Length: 16 by default. 8 with tCCD=8
- 3.9 µs refresh interval at lower than T_{CASE} 85°C, 1.95µs refresh interval at 85°C < T_{CASE} < 95 °C
- Bi-directional Differential Data-Strobe
- On Die ECC
- On Die Termination via Mode Register setting
- Connectivity Test Mode (TEN) is supported
- Asynchronous Reset
- Fly-by topology
- RoHS compliant and Halogen-Free

Part No.	Max Freq.
A5G08RC6BVQKSBV	2400MHz (0.416ns@CL=40) x2

3. PIN Description

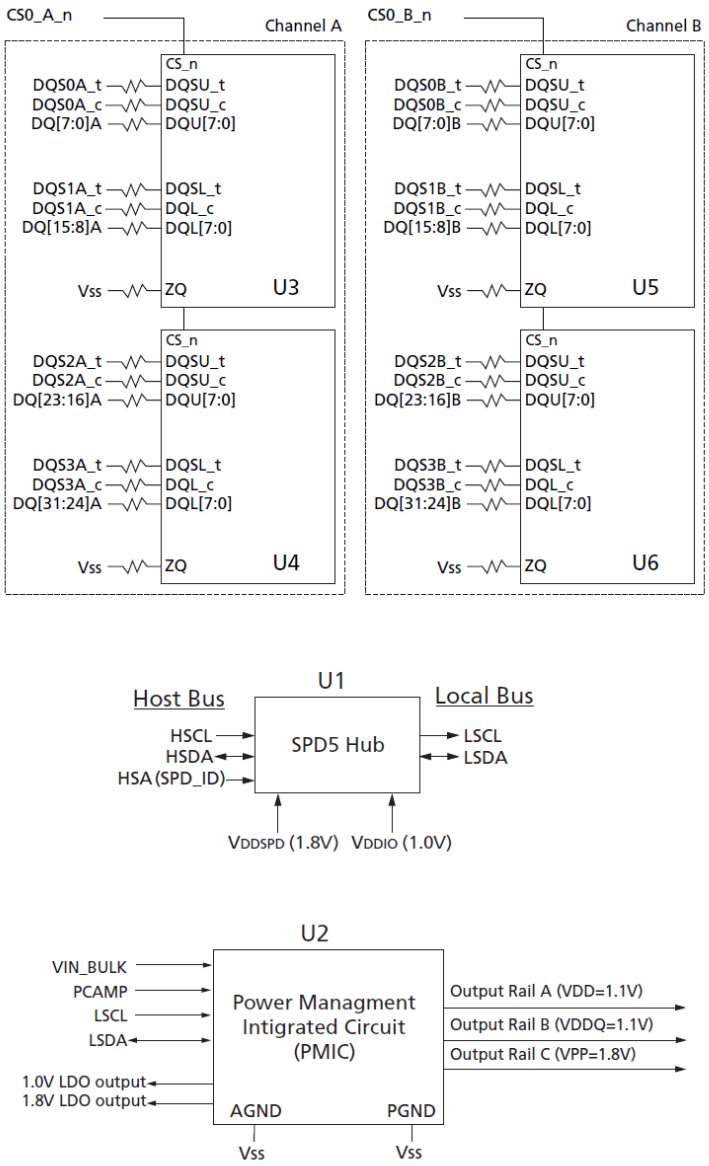
Pin Symbol	Description
CA[12:0]_A CA[12:0]_B,	SDRAM Command/Address bus
CS[1:0]_A CS[1:0]_B, CS[1:0]_A_n, CS[1:0]_B_n	SDRAM Chip Select
PAR_A PAR_B	SDRAM Parity input
CK_t CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM Clocks (true/positive)
CK_c CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM Clocks (complement/negative)
ALERT_n	SDRAM alert for CRC error
RESET_n	Set DRAM to known state
PCAMP	Control and Monitor Port
HSCL	I2C/I3C-Basic Host Sideband Bus Clock
HSDA	I2C/I3C-Basic Host Sideband Bus Data
HSA	I2C/I3C-Basic Host Sideband Bus Address
LBDQ	Loopback data output:
DQ[31:0]_A DQ[31:0]_B	DIMM memory data bus channel A and B
CB[7:0]_A CB[7:0]_B	DIMM ECC check bits(CB) channel A and B
DQS[9:0]_A_t DQS[9:0]_B_t	SDRAM data strobes (positive line of differential pair)
DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM data strobes (negative line of differential pair)
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
VIN_BULK	DIMM Power Supply from system to PMIC
VIN_MGMT	DIMM Power Supply from system to PMIC
VSS	Power supply return (ground)
RFU	Reserved for future use
LBDQS	Loopback data strobe output
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable

4. PIN Assignment

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VIN_BULK	2	HSA	131	CK0_A_t	132	CK1_A_t
3	VIN_BULK	4	HSCL	133	CK0_A_c	134	CK1_A_c
5	RFU	6	HSDA	135	VSS	136	VSS
7	PWR_GOOD	8	PWR_EN	137	CK0_B_t	138	CK1_B_t
9	VSS	10	VSS	139	CK0_B_c	140	CK1_B_c
11	DQ0_A	12	DQ1_A	141	VSS	142	VSS
13	VSS	14	VSS	143	RFU	144	CA12_B
15	DQ2_A	16	DQ3_A	145	CA11_B	146	CA10_B
17	VSS	18	VSS	147	VSS	148	VSS
19	DM0_A_n	20	DQS0_A_c	149	CA9_B	150	CA8_B
21	VSS	22	DQS0_A_t	151	CA7_B	152	CA6_B
23	DQ4_A	24	VSS	153	VSS	154	VSS
25	VSS	26	DQ5_A	155	CA5_B	156	CA4_B
27	DQ6_A	28	VSS	157	CA3_B	158	CA2_B
29	VSS	30	DQ7_A	159	VSS	160	VSS
31	DQ8_A	32	VSS	161	CS0_B_n	162	CA1_B
33	VSS	34	DQ09_A	163	RESET_n	164	CA0_B
35	DQ10_A	36	VSS	165	CS1_B_n	166	VSS
37	VSS	38	DQ11_A	167	VSS	168	CB0_B
39	DQS1_A_c	40	VSS	169	DQS4_B_c	170	VSS
41	DQS1_A_t	42	DM1_A_n	171	DQS4_B_t	172	CB1_B
43	VSS	44	VSS	173	VSS	174	VSS
45	DQ12_A	46	DQ13_A	175	CB3_B	176	CB2_B
47	VSS	48	VSS	177	VSS	178	VSS
49	DQ14_A	50	DQ15_A	179	DQ0_B	180	DQ1_B
51	VSS	52	VSS	181	VSS	182	VSS
53	DQ16_A	54	DQ17_A	183	DQ2_B	184	DQ3_B
55	VSS	56	VSS	185	VSS	186	VSS
57	DQ18_A	58	DQ19_A	187	DM0_B_n	188	DQS0_B_c
59	VSS	60	VSS	189	VSS	190	DQS0_B_t
61	DM2_A_n	62	DQS2_A_c	191	DQ4_B	192	VSS
63	VSS	64	DQS2_A_t	193	VSS	194	DQ5_B
65	DQ20_A	66	VSS	195	DQ6_B	196	VSS
67	VSS	68	DQ21_A	197	VSS	198	DQ7_B
69	DQ22_A	70	VSS	199	DQ8_B	200	VSS
71	VSS	72	DQ23_A	201	VSS	202	DQ9_B
73	DQ24_A	74	VSS	203	DQ10_B	204	VSS
75	VSS	76	DQ25_A	205	VSS	206	DQ11_B
77	DQ26_A	78	VSS	207	DQS1_B_c	208	VSS
79	VSS	80	DQ27_A	209	DQS1_B_t	210	DM1_B_n
81	DQS3_A_c	82	VSS	211	VSS	212	VSS
83	DQS3_A_t	84	DM3_A_n	213	DQ12_B	214	DQ13_B
85	VSS	86	VSS	215	VSS	216	VSS
87	DQ28_A	88	DQ29_A	217	DQ14_B	218	DQ15_B
89	VSS	90	VSS	219	VSS	220	VSS
91	DQ30_A	92	DQ31_A	221	DQ16_B	222	DQ17_B
93	VSS	94	VSS	223	VSS	224	VSS
95	CB0_A	96	CB1_A	225	DQ18_B	226	DQ19_B
97	VSS	98	VSS	227	VSS	228	VSS
99	CB2_A	100	DQS4_A_c	229	DM2_B_n	230	DQS2_B_c
101	VSS	102	DQS4_A_t	231	VSS	232	DQS2_B_t
103	CB3_A	104	VSS	233	DQ20_B	234	VSS
105	VSS	106	CS0_A_n	235	VSS	236	DQ21_B
107	CA0_A	108	ALERT_n	237	DQ22_B	238	VSS
109	CA1_A	110	CS1_A_n	239	VSS	240	DQ23_B
111	VSS	112	VSS	241	DQ24_B	242	VSS
113	CA2_A	114	CA3_A	243	VSS	244	DQ25_B
115	CA4_A	116	CA5_A	245	DQ26_B	246	VSS

117	VSS	**118**	VSS	**247**	VSS	**248**	DQ27_B
119	CA6_A	**120**	CA7_A	**249**	DQS3_B_c	**250**	VSS
121	CA8_A	**122**	CA9_A	**251**	DQS3_B_t	**252**	DM3_B_n
123	VSS	**124**	VSS	**253**	VSS	**254**	VSS
125	CA10_A	**126**	CA11_A	**255**	DQ28_B	**256**	DQ29_B
Key				**257**	VSS	**258**	VSS
127	CA12_A	**128**	RFU	**259**	DQ30_B	**260**	DQ31_B
129	VSS	**130**	VSS	**261**	VSS	**262**	VSS

5. Function Block Diagram



Note:
1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

6. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.3V ~ 1.4V	V	1,3
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.4V	V	1,3
Voltage on V_{PP} pin relative to V_{SS}	V_{PP}	-0.4V ~ 2.1V	V	4
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.4V	V	1,3,5
Storage Temperature	T_{STG}	-55 to +100	˚C	1,2

Note
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5 V is specified in JEDEC Standard No.79-5 Section 8.3.4, Section 8.3.5, and Section 8.3.6.

7. Recommended DC Operating Conditions

Item	Symbol	Low Freq Voltage Spec Freq: DC to 2MHz			Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 10 to 20Mhz		Notes
		Min.	Typical	Max.	Zmax	Unit	Zmax	Unit	
Device Supply Voltage	V_{DD}	1.067	1.1	1.166	30	mOhm	50	mOhm	1,2,3
Supply Voltage	V_{DDQ}	1.067	1.1	1.166	40	mOhm	80	mOhm	1,2,3
Core Power Voltage	V_{PP}	1.746	1.8	1.908	100	mOhm	170	mOhm	3

Note:
1. VDDQ must be less than or equal to VDD. VDD must be within 66 mV of VDDQ.
2 .AC parameters are measured separately on VDD and VDDQ.
3. DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations.
4. Z(f) is per voltage domain per DRAM device. Per DRAM BGA pin is not required.
5. Z(f) does not include the DRAM package and silicon die.

8. DIMM Voltage Requirements

Symbol		Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Min.	Typical	Max.		
VIN_BULK	Host Supply Voltage	4.25	5.0	5.5	2.5/2.0	Operational
SWA, SWB	PMIC Output Supply Voltage	-	1.1	-	6	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	12	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	2	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020	Operational

Note:
1. During first power on, the input voltage supply must reach minimum 4.25 V for PMIC to detect valid input supply.
2. The ramp up rate between 300 mV and 4.0 V.
3. The ramp down rate between 4.0 V and 300 mV.
4. The area under the curve above VIN_Bulk = TBD V. VIN_Bulk_AC spec must also be satisfied.
5. The minimum input current requirement is to deliver the maximum output current on VOUT_1.8V and VOUT_1.0V LDO plus the current.
6. VIN_Bulk = 5.0 V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR_EN signal is static.
7. VIN_Bulk = 5.0 V. Measured at room temperature. All output regulators and LDOs are on with 0 A output load. VR_EN signal is static.
8. 20 MHz bandwidth limited measurement for all voltages in the table.
9. Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedance.
10.The SDRAM specification must be met and take precedence over this document.
11. Voltages are measured at the DIMM gold fingers and at PMIC output pins.
12. Typical voltage is platform dependent. This is a suggested value only.

9. Operating Temperature Range

Symbol	Parameter	Ratings	Unit	Notes
T_{STG}	Storage Temperature	-55 to +100	°C	1
T_{CASE}	Normal Operating Temperature Range	0 to +85	°C	1,2,4,5
	Extended Operating Temperature Range	85 to +95	°C	1,3,4,5
T_A	Operating Temperature Range	0 to +85	°C	1,3,4,5,6

Note:
1.The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer to JESD51-2.
2.The Normal Temperature Range specifies the temperatures maximum limit when device is operating in the Normal Temperature Mode. During operation, the DRAM case temperature must be maintained between 0 to 85°C under all operating conditions.
3.The Extended Temperature Range specifies the temperatures maximum limit when device is operating in the Extended Temperature Mode, during operation, the DRAM case temperature must be maintained between 85 to 95°C under all operating conditions.
4.Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [TOPER – (2.5°C × log2N)], where N is the number of the stacked dies.
5. Both operating temperature specifications must be satisfied.
6. Operating ambient temperature surrounding the package

10. Electrostatic Discharge Sensitivity

Item	Min.	Max	Units	Notes
HBM (Human-Body Model)	1000V	-	V	2
CDM (Charge-Device Model)	250V	-	V	3

Note:
1. State-of-the-art basic ESD control measures have to be in place when handling devices
2. Refer to ESDA / JEDEC Joint Standard JS-001 for measurement procedures.
3. Refer to ESDA / JEDEC Joint Standard JS-002 f for measurement procedures

11. Reliability

MTBF @25 °C (Hours) [1]	FIT @ 25 °C [2]	MTBF @40 °C (Hours) [1]	FIT @ 40 °C [2]
18,162,005	55	8,924,587	112

Note:
1.The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Bellcore Prediction, which based on reliability data of the individual components in the module. It assumes nominal voltage, with all other parameters within specified range.
2. Failures per Billion Device-Hours.

12. IDD Specification Parameter

Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

Symbol	Proposed Conditions	Value	Units
IDD0	Operating One Bank Active-Precharge Current	150	mA
IDD0F	Operating Four Bank Active-Precharge Current	190	mA
IDD2N	Precharge Standby Current	80	mA
IDD2NT	Precharge Standby Non-Target Command Current	90	mA
IDD2P	Precharge Power-Down Current	50	mA
IDD3N	Active Standby Current	100	mA
IDD3P	Active Power-Down Current	50	mA
IDD4R	Operating burst read Current	480	mA
IDD4W	Operating Burst Write Current	720	mA
IDD4WC	Operating burst write with write CRC current	720	mA
IDD5B	Burst Refresh Current (Normal Refresh Mode):	231	mA
IDD5F	Burst Refresh Current (Fine Granularity Refresh Mode)	230	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	140	mA
IDD6N	Self Refresh Current	30	mA
IDD7	Operating Bank Interleave Read Current	630	mA
IDD8	Maximum Power Saving Deep Power Down Mode Current	20	mA

13. Timing Parameter

Parameter(JEDEC)	Symbol	DDR5-4800		Units	Notes
		Min.	Max.		
Clock Timing					
Average Clock Period	tCK(avg)	0.416	<0.682	ns	1
Command and Address Timing					
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(8nCK,5ns)	-	nCK	
WRITE CAS_n to WRITE CAS_n command delay for same bank group	tCCD_L_WR	Max(32nCK,20ns)	-	ns	
WRITE CAS_n to WRITE CAS_n command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)	-	nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK,5ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK,5ns)	-	tCK	
Four activate window for 2KB page size	tFAW_2K	Max(40nCK,16.640ns)	-	ns[1]	1
Four activate window for 1KB page size	tFAW_1K	Max(32nCK,13.312ns)	-	ns[1]	1
Delay from start of internal write transaction to internal read command for different bankgroup	tWTR_S	Max(4nCK,2.5ns)	-	ns	
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max(16nCK,10ns)	-	ns	
Delay from start of internal write transaction to internal read with auto precharge command for same bank	tWTRA	=tWR-tRTP	-	ns	
Internal READ Command to PRECHARGE Command delay	tRTP	Max(12nCK,7.5ns)	-	ns	
PRECHARGE (PRE) to PRECHARGE (PRE) delay	tPPD	2	-	nCK (avg)	
WRITE recovery time	tWR	29.952	-	ns[1]	1
Command and Address Timing for 3DS					
Minimum Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(8nCK,5ns)	-	nCK	4
Minimum Write to Write command delay for same bank group in same logical rank	tCCD_L_WR_slr	Max(32nCK,20ns)	-	nCK	4
Minimum Read to Write command delay for same bank group in same logical rank	tCCD_L_RTW_slr	CL - CWL+RBL/2 + 2tCK(Read DQS offset)+ (tRPST-0.5tCK)+tWPRE			4,5,7,8
Minimum Write to Read command delay for same bank group in same logical rank	tCCD_L_WTR_slr	CWL+WBL/2 + tWTR_S		nCK	4,6,8
Minimum Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	8	-	nCK	4
Minimum Write to Write command delay for different bank group in same logical rank	tCCD_S_WR_slr	8	-	nCK	4
Minimum Read to Write command delay for different bank group in same logical rank	tCCD_S_RTW_slr	CL - CWL+RBL/2+2tCK (Read DQS offset)+(tRPST-0.5tCK)+tWPRE			4,5,7,8
Minimum Write to Read command delay for different bank group in same logical rank	tCCD_S_WTR_slr	CWL + WBL/2 + tWTR_S		nCK	4,6,8
Minimum Read to Read command delay in different logical ranks	tCCD_dlr	8	-	nCK	4
Minimum Write to Write command delay in different logical ranks	tCCD_WR_dlr	8	-	nCK	4,12
Minimum Write to Write command delay in different physical ranks	tCCD_WR_dpr	8	-	nCK	4,12,13
Minimum Read to Write command delay in different physical ranks	tCCD_RTW_dlr	CL - CWL+RBL/2+2tCK (Read DQS offset)+(tRPST-0.5tCK)+tWPRE			4,5,7,8
Minimum Write to Read command delay in different logical ranks	tCCD_WTR_dlr	CWL + WBL/2 + tWTR_S		nCK	4,6,8
ACTIVATE to ACTIVATE Command delay to different bank group in the same logical rank	tRRD_S_slr	8	-	nCK	4
ACTIVATE to ACTIVATE Command delay to same bank group in the same logical rank	tRRD_L_slr	Max(12nCK, 5ns)	-	nCK	4
ACTIVATE to ACTIVATE Command delay to different logical ranks	tRRD_dlr	4	-	nCK	4
Four activate window to the same logical rank	tFAW_slr	Max(32nCK,13.312ns)	-	nCK	1,4,9
Four activate window to different logical ranks	tFAW_dlr	16	-	nCK	4
Activate window by DIMM channel	tDCAW	128	-	nCK	4,10,11,13
DIMM Channel Activate Command Count in tDCAW	nDCAC	-	32	ACT	4,10,11,13
Exit Self Refresh to commands not requiring a locked DLL	tXS_3DS	Max(5nCK,tRFC_slr1(min)	-		2,3,4

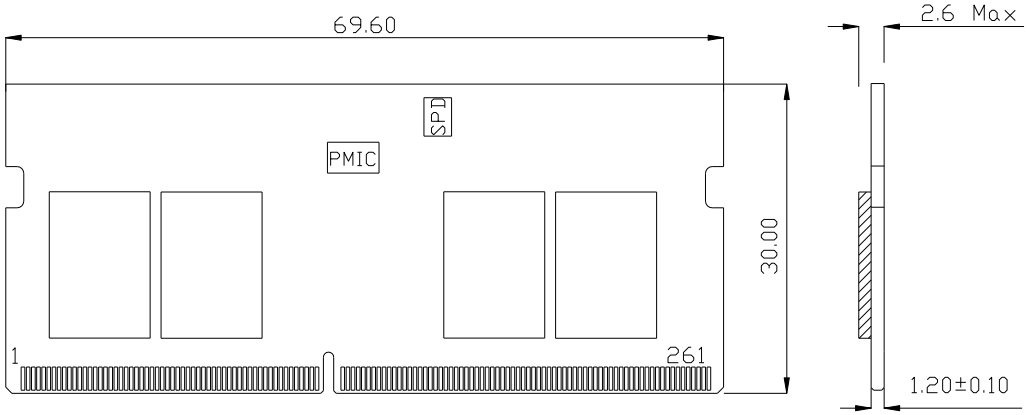
Note:

1. Timing Parameters that scale are rounded down to 1ps of accuracy..
2. Upon exit from Self-Refresh, the 3D Stacked DDR5 SDRAM requires a minimum of one extra refresh command to all logical ranks before it is put back into Self-Refresh Mode.
3. This parameter utilizes a component that varies based on density. Refer to Section 4.13.5 for more information 3DS Refresh.
4. These timings are for x4 2H and 4H 3Ds devices
5. RBL: Read burst length associated with Read command
   RBL = 32 for fixed BL32 and BL32 in BL32 OTF mode
   RBL = 16 for fixed BL16 and BL16 in BL32 OTF mode
   RBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
6. WBL: Write burst length associated with Write command
   WBL = 32 for fixed BL32 and BL32 in BL32 OTF mode
   WBL = 16 for fixed BL16 and BL16 in BL32 OTF mode
   WBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
7. The following is considered for tRTW equation
   1tCK needs to be added due to tDQS2CK
   Read DQS offset timing can pull in the tRTW timing
   1tCK needs to be added when 1.5tCK postamble
8. CWL=CL-2
9. Timing Parameters that scale are rounded down to 1ps of accuracy.
10. Activate commands to different channels on the same DIMM may be issued on the same cycle, not requiring any stagger.
11. Activate commands to the same channel on a DIMM are subject to tDCAW. No more than nDCAC activate commands may be issued to the same channel on a DIMM within tDCAW.
12. tCCD_ WR_dlr and tCCD_ WR_dpr also apply to the WRITE PATTERN command.
13. Parameter applies to dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JEDEC PMICXXXX, but may not applyto DIMMs built with higher current capacity PMICs

14. Physical Dimensions (Units in Millimeters)

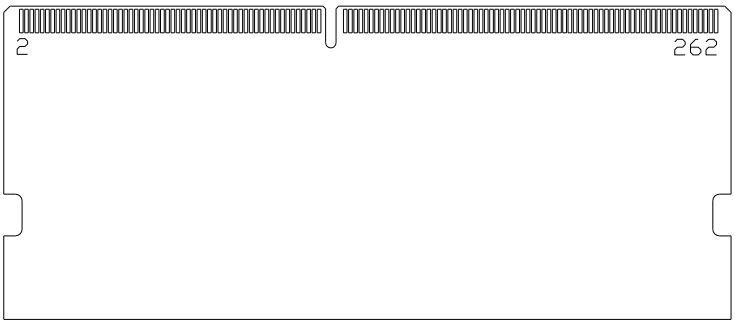
(Drawing not to scale)

Front



Side

Back



Note: Tolerance on all dimensions ±0.006 inch (0.15mm) unless otherwise noted

15. Serial Presence Detects

Byte No.	Function Described	Hex Value
0	Number of Bytes in SPD Device and Beta Level	30
1	SPD Revision for Base Configuration Parameters	10
2	Key Byte / Host Bus Command Protocol Type	12
3	Key Byte / Module Type	03
4	First SDRAM Density and Package	04
5	First SDRAM Addressing	00
6	First SDRAM I/O Width	40
7	First SDRAM Bank Groups & Banks Per Bank Group	42
8	Second SDRAM Density and Package	00
9	Second SDRAM Addressing	00
10	Second SDRAM I/O Width	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	00
12	SDRAM BL32 & Post Package Repair	90
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	02
14	SDRAM Fault Handling 1	00
15	Reserved	00
16	SDRAM Nominal Voltage, VDD	00
17	SDRAM Nominal Voltage, VDDQ	00
18	SDRAM Nominal Voltage, VPP	00
19	SDRAM Timing	00
20	SDRAM Minimum Cycle Time (tCKAVGmin), LSB	A0
21	SDRAM Minimum Cycle Time (tCKAVGmin), MSB	01
22	SDRAM Maximum Cycle Time (tCKAVGmax), LSB	F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), MSB	03
24	CAS Latencies Supported, First Byte	7A
25	CAS Latencies Supported, Second Byte	0D
26	CAS Latencies Supported, Third Byte	00
27	CAS Latencies Supported, Fourth Byte	00
28	CAS Latencies Supported, Fifth Byte	00
29	Reserved	00
30	SDRAM Minimum CAS Latency Time (tAAmin), LSB	80
31	SDRAM Minimum CAS Latency Time (tAAmin), MSB	3E
32	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), LSB	80
33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), MSB	3E
34	SDRAM Minimum Row Precharge Delay Time (tRPmin), LSB	80
35	SDRAM Minimum Row Precharge Delay Time (tRPmin), MSB	3E
36	SDRAM Minimum Active to Precharge Delay Time (tRASmin), LSB	00
37	SDRAM Minimum Active to Precharge Delay Time (tRASmin), MSB	7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), LSB	80
39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), MSB	BB
40	SDRAM Minimum Write Recovery Time (tWRmin), LSB	30

Byte No.	Function Described	Hex Value
41	SDRAM Minimum Write Recovery Time (tWRmin), MSB	75
42	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min), LSB	27
43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min), MSB	01
44	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min), LSB	A0
45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min), MSB	00
46	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min), LSB	82
47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsb_dlr min), MSB	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (tRFC1_dlr min), LSB	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (tRFC1_dlr min), MSB	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (tRFC2_dlr min), LSB	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (tRFC2_dlr min), MSB	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (tRFCsb_dlr min), LSB	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (tRFCsb_dlr min), MSB	00
54	SDRAM Refresh Management, First Byte, First SDRAM	00
55	SDRAM Refresh Management, Second Byte, First SDRAM	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (tRRD_Lmin), LSB	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (tRRD_Lmin), MSB	13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (tRRD_Lmin), Lower Clock Limit	08
73	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group (tCCD_Lmin), LSB	88
74	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group (tCCD_Lmin), MSB	13
75	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group (tCCD_Lmin), Lower Clock Limit	08
76	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group (tCCD_L_WRmin), LSB	20
77	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group (tCCD_L_WRmin), MSB	4E

Byte No.	Function Described	Hex Value
78	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group (tCCD_L_WRmin), Lower Clock Limit	20
79	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group (tCCD_L_WR2min), LSB	10
80	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group (tCCD_L_WR2min), MSB	27
81	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group (tCCD_L_WR2min), Lower Clock Limit	10
82	SDRAM Minimum Four Activate Window (tFAWmin), LSB	1A
83	SDRAM Minimum Four Activate Window (tFAWmin), MSB	41
84	SDRAM Minimum Four Activate Window (tFAWmin), Lower Clock Limit	28
85	SDRAM Minimum Write to Read Command Delay Time, Same Bank Group, (tCCD_L_WTRmin), LSB	10
86	SDRAM Minimum Write to Read Command Delay Time, Same Bank Group, (tCCD_L_WTRmin), MSB	27
87	SDRAM Minimum Write to Read Command Delay Time, Same Bank Group, (tCCD_L_WTRmin), Lower Clock Limit	10
88	SDRAM Minimum Write to Read Command Delay Time, Different Bank Group, (tCCD_S_WTRmin), LSB	C4
89	SDRAM Minimum Write to Read Command Delay Time, Different Bank Group, (tCCD_S_WTRmin), MSB	09
90	SDRAM Minimum Write to Read Command Delay Time, Different Bank Group, (tCCD_S_WTRmin), Lower Clock Limit	04
91	SDRAM Minimum Read to Precharge Command Delay Time, (tRTPmin), LSB	4C
92	SDRAM Minimum Read to Precharge Command Delay Time, (tRTPmin), MSB	1D
93	SDRAM Minimum Read to Precharge Command Delay Time, (tRTPmin), Lower Clock Limit	0C
94~127	Reserved -- must be coded as 0x00	00
128~191	Reserved for future use	00
192	SPD Revision for SPD bytes 192~447	10
193	Hashing Sequence	00
194	SPD Manufacturer ID Code, First Byte	80
195	SPD Manufacturer ID Code, Second Byte	B3
196	SPD Device Type	80
197	SPD Device Revision Number	21
198	PMIC 0 Manufacturer ID Code, First Byte	80
199	PMIC 0 Manufacturer ID Code, Second Byte	B3
200	PMIC 0 Device Type	82
201	PMIC 0 Revision Number	20
202	PMIC 1 Manufacturer ID Code, First Byte	00
203	PMIC 1 Manufacturer ID Code, Second Byte	00
204	PMIC 1 Device Type	00
205	PMIC 1 Revision Number	00
206	PMIC 2 Manufacturer ID Code, First Byte	00
207	PMIC 2 Manufacturer ID Code, Second Byte	00
208	PMIC 2 Device Type	00
209	PMIC 2 Revision Number	00
210	Thermal Sensor Manufacturer ID Code, First Byte	00
211	Thermal Sensor Manufacturer ID Code, Second Byte	00

Byte No.	Function Described	Hex Value
212	Thermal Sensor Device Type	00
213	Thermal Sensor Revision Number	00
214~229	Reserved -- must be coded as 0x00	00
230	Module Nominal Height	0F
231	Module Maximum Thickness	11
232	Reference Raw Card Used	02
233	DIMM Attributes	81
234	Module Organization	00
235	Memory Channel Bus Width	22
236~239	Reserved -- must be coded as 0x00	00
240	Reserved(UDIMM/SODIMM), Registering Clock Driver Manufacturer ID Code, First Byte	00
241	Reserved(UDIMM/SODIMM), Registering Clock Driver Manufacturer ID Code, Second Byte (RDIMM/LRDIMM).	00
242	Reserved(UDIMM/SODIMM), Register Device Type (RDIMM/LRDIMM).	00
243	Reserved(UDIMM/SODIMM), Register Revision Number (RDIMM/LRDIMM).	00
244	Reserved(UDIMM/SODIMM), Data Buffer Manufacturer ID Code, First Byte (RDIMM/LRDIMM).	00
245	Reserved(UDIMM/SODIMM), Data Buffer Manufacturer ID Code, Second Byte (RDIMM/LRDIMM).	00
246	Reserved(UDIMM/SODIMM), Data Buffer Device Type (RDIMM/LRDIMM).	00
247	Reserved(UDIMM/SODIMM), Data Buffer Revision Number (RDIMM/LRDIMM).	00
248	Reserved(UDIMM/SODIMM), RCD-RW08 Clock Driver Enable (RDIMM/LRDIMM).	00
249	Reserved(UDIMM/SODIMM), RCD-RW09 Output Address and Control Enable (RDIMM/LRDIMM).	00
250	Reserved(UDIMM/SODIMM), RCD-RW0A QCK Driver Characteristics (RDIMM/LRDIMM).	00
251	Reserved(UDIMM/SODIMM), RCD-RW0B (RDIMM/LRDIMM).	00
252	Reserved(UDIMM/SODIMM), RCD-RW0C QxCA and QxCS_n Driver Characteristics (RDIMM/LRDIMM).	00
253	Reserved(UDIMM/SODIMM), RCD-RW0D Data Buffer Interface Driver Characteristics (RDIMM/LRDIMM).	00
254	Reserved(UDIMM/SODIMM), RCD-RW0E QCK, QCA and QCS Output Slew Rate (RDIMM/LRDIMM).	00
255	Reserved(UDIMM/SODIMM), RCD-RW0F BCK, BCOM, and BCS Output Slew Rate (RDIMM/LRDIMM).	00
256	Reserved(UDIMM/SODIMM), DB-RW86 DQS RTT Park Termination (RDIMM/LRDIMM).	00
257~319	Reserved -- must be coded as 0x00	00
320~383	Reserved -- must be coded as 0x00	00
384~447	Reserved -- must be coded as 0x00	00
448~509	Reserved for future use	00
510~511	CRC for SPD bytes 0~509	2D 8C
512~513	Module Manufacturer's ID Code	86 E3
514	Module Manufacturing Location	05
515~516	Module Manufacturing Date	YY WW
517~520	Module Serial Number	00000000

Byte No.	Function Described	Hex Value
521~550	Module Part Number	A5G08RC06VQKSBV
551	Module Revision Code	31
552~553	DRAM Manufacturer's ID Code	80 CE
554	DRAM Stepping	42
555~575	Module Manufacturer's Specific Data	00
579~637	Module Manufacturer's Specific Data	00
638~639	Module Manufacturer's Specific Data	00
640~703	End User Programmable	00
704~767	End User Programmable	00
768~831	End User Programmable	00
832~895	End User Programmable	00
896~959	End User Programmable	00
960~1023	End User Programmable	00

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