

IMM4G72D3RDQ4AG (Die Revision D) 32GByte (4G x 72 Bit)

32GB DDR3 Registered DIMM
RoHS Compliant Product

Remark:

Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures.

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Features

- 240-Pin Registered Dual-In-Line Memory Module
- Capacity: 32GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
 - PC3-8500: 5, 6, 7, 8
- Programmable CAS Write Latency (CWL):
 - PC3-8500: 5, 6
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) with EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.18inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM4G72D3xRDQ4AG-Dzzzy	32GB	4Gx72	4	32GB DDR3 Registered DIMM

Notes:

- x: Operating Voltage
- y: Operating Temperature
- zzz: Speed Grade

Table 2 - Operating Voltage

Part Number	Operating Voltage
Blank	$V_{DD}, V_{DDQ} = 1.5V (1.425V-1.575V)$

Table 3 – Temperature Grade

Part Number	Temperature Grade	Tcase
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when $85^{\circ}C < T_{case} \leq 95^{\circ}C$.

Table 4 – Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
187E	PC3-8500 (DDR3-1066)	533MHz (1.875ns@CL=7)

Table 5 – Memory Chip Information

Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM4G72D3RDQ4AG-Dzzzy	I'M	IM8G04D3FDDG	1.35V/1.5V	1Gx4x2 DDP	Lead Free

Part Number Decoder

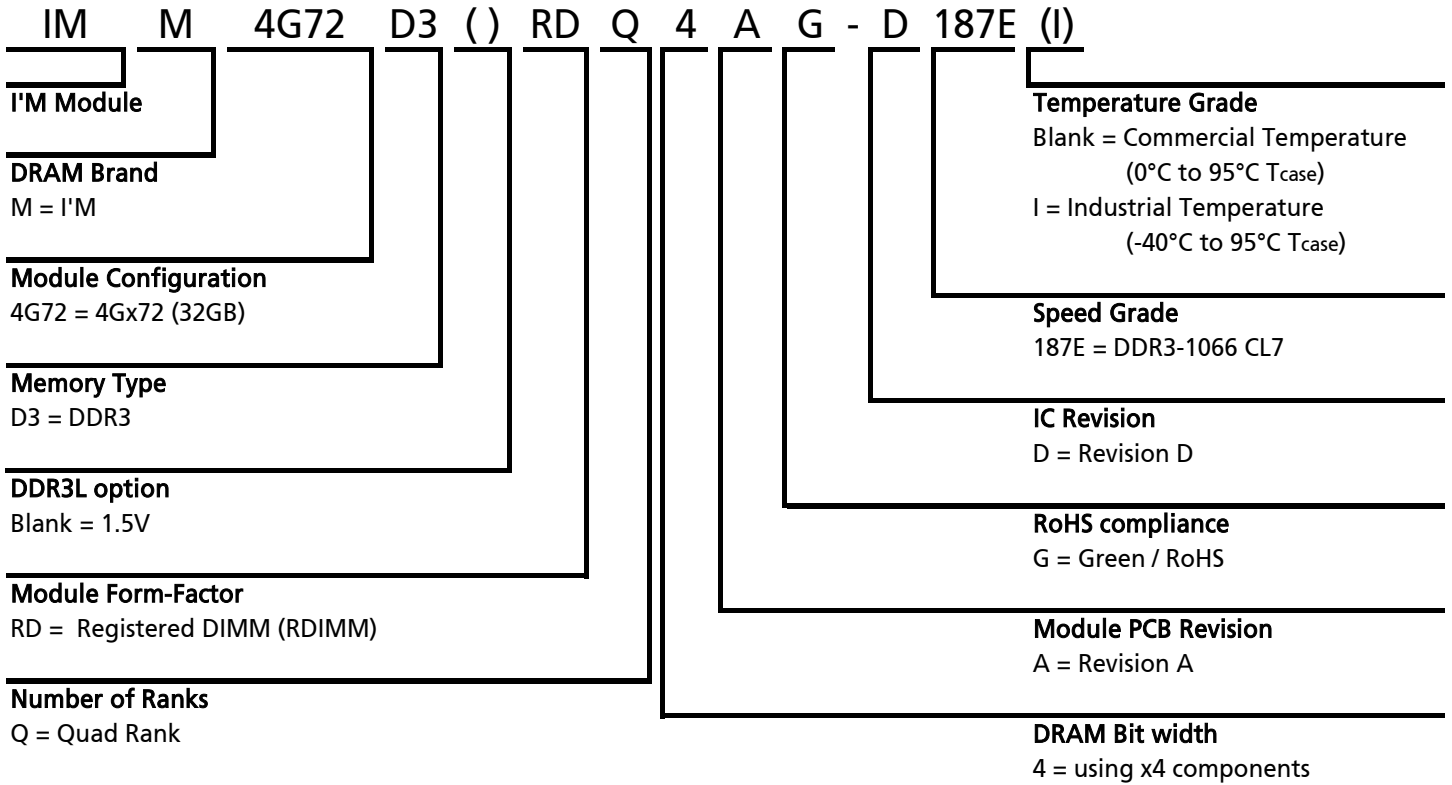


Table 6 - Addressing

Parameter	32GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1Gx4x2 DDP)
Column address	2K A[9:0], A11
Module rank address	4 /S[3:0]
Number of devices	36

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V _{REFDQ}	121	V _{SS}	61	A2	181	A1
2	V _{SS}	122	D4	62	V _{DD}	182	V _{DD}
3	D0	123	D5	63	CK1	183	V _{DD}
4	D1	124	V _{SS}	64	/CK1	184	CK0
5	V _{SS}	125	DQS9	65	V _{DD}	185	/CK0
6	/DQS0	126	/DQS9	66	V _{DD}	186	V _{DD}
7	DQS0	127	V _{SS}	67	V _{REFCA}	187	/EVENT
8	V _{SS}	128	D6	68	PAR_IN	188	A0
9	D2	129	D7	69	V _{DD}	189	V _{DD}
10	D3	130	V _{SS}	70	A10, AP	190	BA1
11	V _{SS}	131	D12	71	BA0	191	V _{DD}
12	D8	132	D13	72	V _{DD}	192	/RAS
13	D9	133	V _{SS}	73	/WE	193	/S0
14	V _{SS}	134	DQS10	74	/CAS	194	V _{DD}
15	/DQS1	135	/DQS10	75	V _{DD}	195	ODT0
16	DQS1	136	V _{SS}	76	/S1	196	A13
17	V _{SS}	137	D14	77	ODT1	197	V _{DD}
18	D10	138	D15	78	V _{DD}	198	/S3
19	D11	139	V _{SS}	79	/S2	199	V _{SS}
20	V _{SS}	140	D20	80	V _{SS}	200	D36
21	D16	141	D21	81	D32	201	D37
22	D17	142	V _{SS}	82	D33	202	V _{SS}
23	V _{SS}	143	DQS11	83	V _{SS}	203	DQS13
24	/DQS2	144	/DQS11	84	/DQS4	204	/DQS13
25	DQS2	145	V _{SS}	85	DQS4	205	V _{SS}
26	V _{SS}	146	D22	86	V _{SS}	206	D38
27	D18	147	D23	87	D34	207	D39
28	D19	148	V _{SS}	88	D35	208	V _{SS}
29	V _{SS}	149	D28	89	V _{SS}	209	D44
30	D24	150	D29	90	D40	210	D45
31	D25	151	V _{SS}	91	D41	211	V _{SS}
32	V _{SS}	152	DQS12	92	V _{SS}	212	DQS14
33	/DQS3	153	/DQS12	93	/DQS5	213	/DQS14
34	DQS3	154	V _{SS}	94	DQS5	214	V _{SS}
35	V _{SS}	155	D30	95	V _{SS}	215	D46
36	D26	156	D31	96	D42	216	D47
37	D27	157	V _{SS}	97	D43	217	V _{SS}
38	V _{SS}	158	CB4	98	V _{SS}	218	D52
39	CB0	159	CB5	99	D48	219	D53
40	CB1	160	V _{SS}	100	D49	220	V _{SS}
41	V _{SS}	161	DQS17	101	V _{SS}	221	DQS15
42	/DQS8	162	/DQS17	102	/DQS6	222	/DQS15
43	DQS8	163	V _{SS}	103	DQS6	223	V _{SS}
44	V _{SS}	164	CB6	104	V _{SS}	224	D54
45	CB2	165	CB7	105	D50	225	D55
46	CB3	166	V _{SS}	106	D51	226	V _{SS}
47	V _{SS}	167	NC	107	V _{SS}	227	D60
48	V _{TT}	168	/RESET	108	D56	228	D61
49	V _{TT}	169	CKE1	109	D57	229	V _{SS}
50	CKE0	170	V _{DD}	110	V _{SS}	230	DQS16
51	V _{DD}	171	A15	111	/DQS7	231	/DQS16
52	BA2	172	A14	112	DQS7	232	V _{SS}
53	/ERR_OUT	173	V _{DD}	113	V _{SS}	233	D62
54	V _{DD}	174	A12, /BC	114	D58	234	D63
55	A11	175	A9	115	D59	235	V _{SS}
56	A7	176	V _{DD}	116	V _{SS}	236	V _{DDSPD}
57	V _{DD}	177	A8	117	SA0	237	SA1
58	A5	178	A6	118	SCL	238	SDA
59	A4	179	V _{DD}	119	SA2	239	V _{SS}
60	V _{DD}	180	A3	120	V _{TT}	240	V _{TT}

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
V _{DD}	SDRAM core power supply	V _{REFDQ}	SDRAM I/O reference supply
V _{REFCA}	SDRAM command/address reference supply	V _{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0, CK1	SDRAM clocks (positive line of differential pair)	/CK0, /CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S3	DIMM rank select lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS17	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS17	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	CB0-CB7	Data check bits input/output
SCL	EEPROM clock	SDA	EEPROM data line
SA0-SA2	EEPROM address input	V _{DDSPD}	EEPROM positive power supply
PAR_IN	Parity input	/EVENT	Temperature event
/ERR_OUT	Parity error output	/RESET	Register and SDRAM control pin
V _{TT}	Termination voltage	NC	Spare pins (no connect)

Module Dimension

Figure 1 – 240 Pin DDR3 SDRAM Registered DIMM

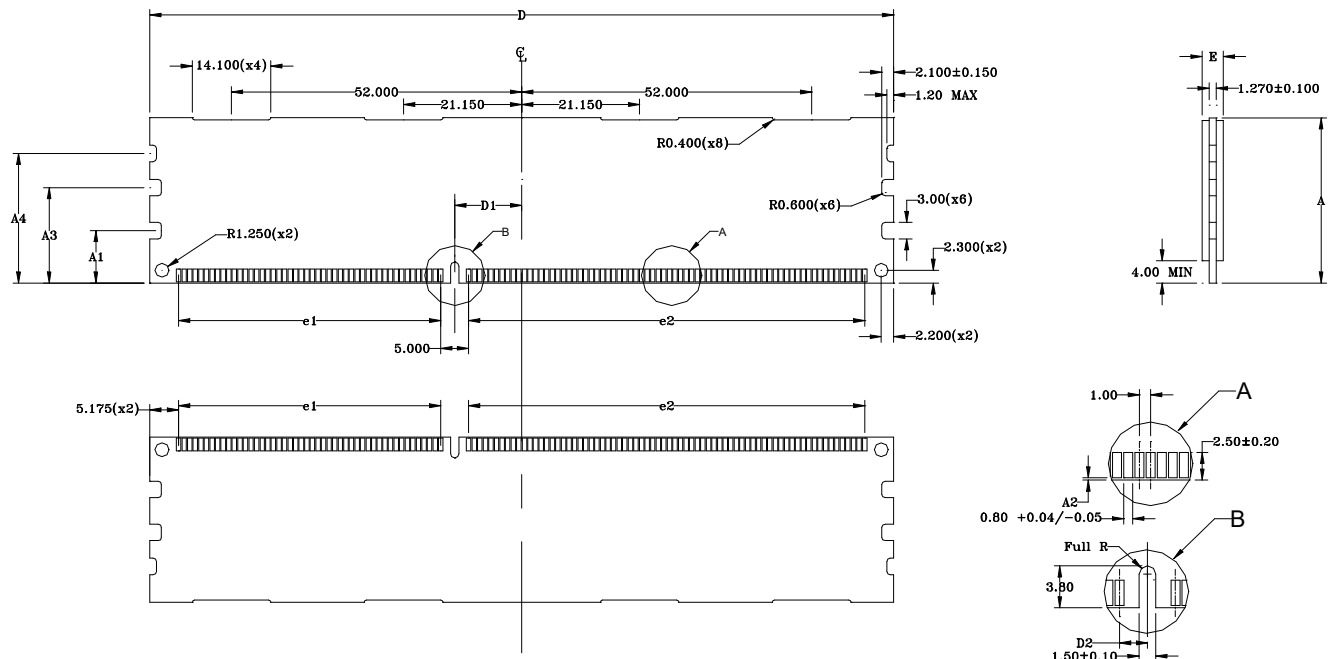


Table 9 - PCB Dimension

Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1	9.35	9.50	9.65
A2	0.05	0.20	0.35
A3	17.15	17.30	17.45
A4	23.15	23.30	23.45
D	133.20	133.35	133.50
D1		12.00 Basic	
D2		2.50 Basic	
e1		47.00 Basic	
e2		71.00 Basic	
E1			4.00

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ± 0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 7)

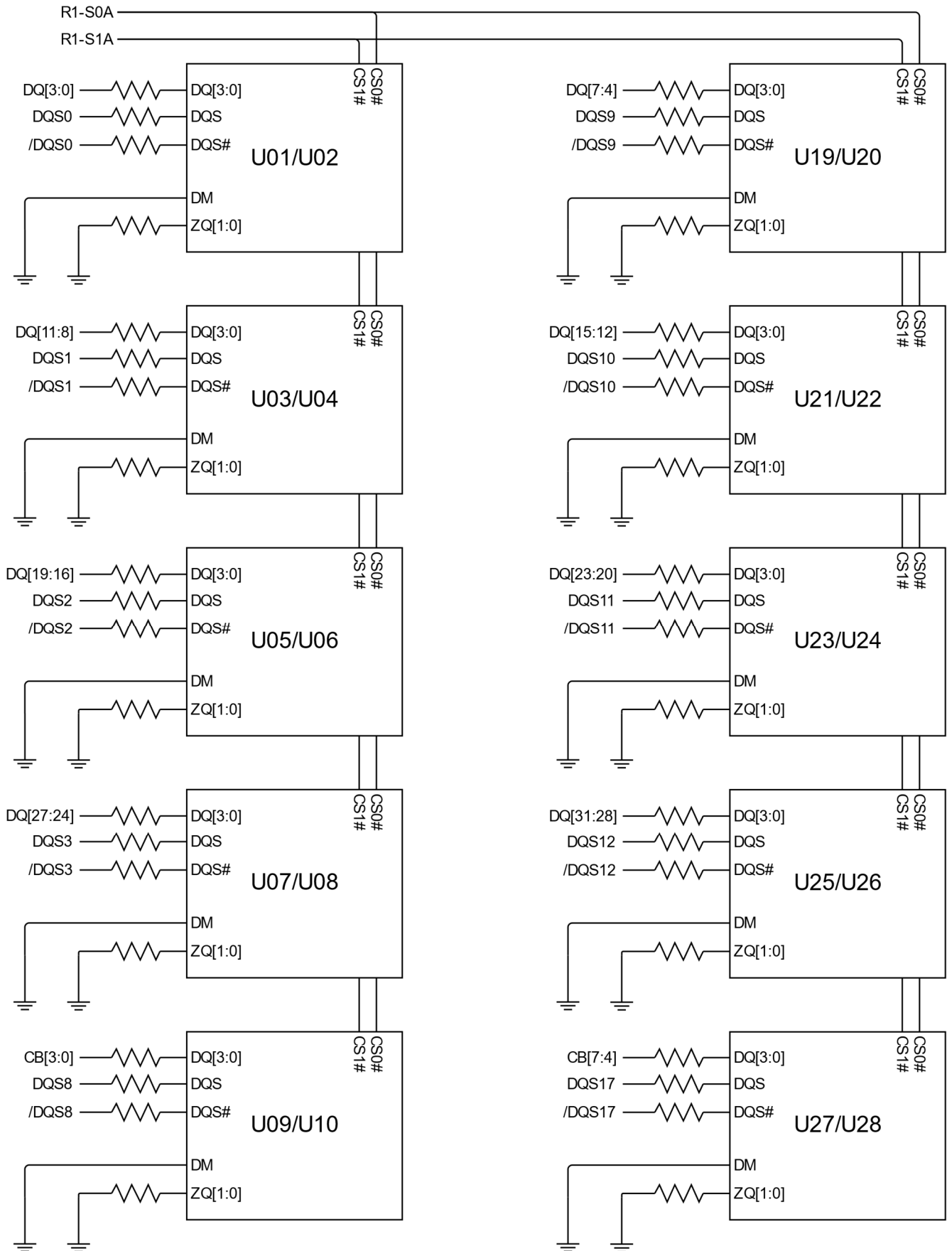


Figure 3 – Functional Block Diagram (Page 2 of 7)

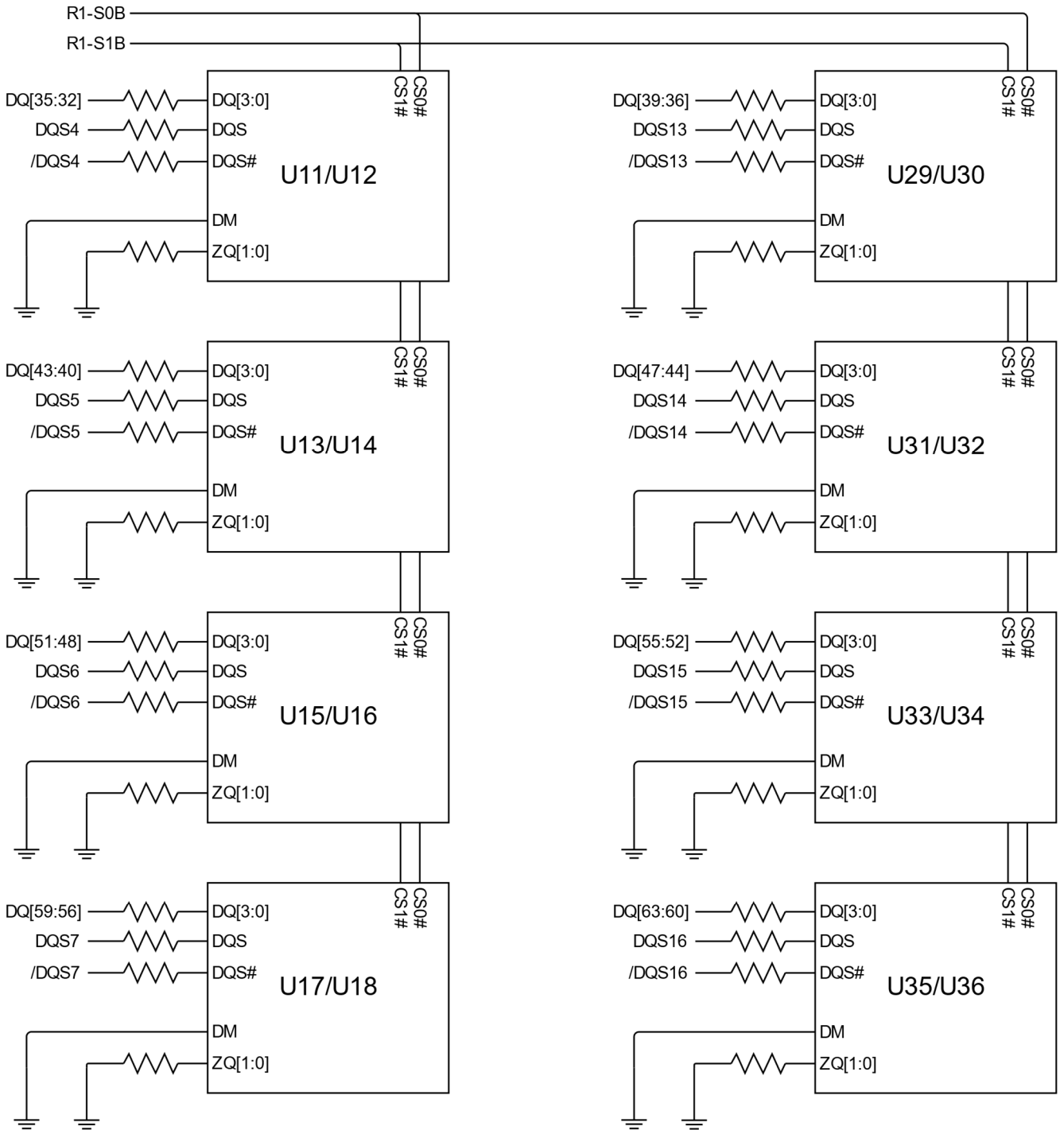


Figure 4 – Functional Block Diagram (Page 3 of 7)

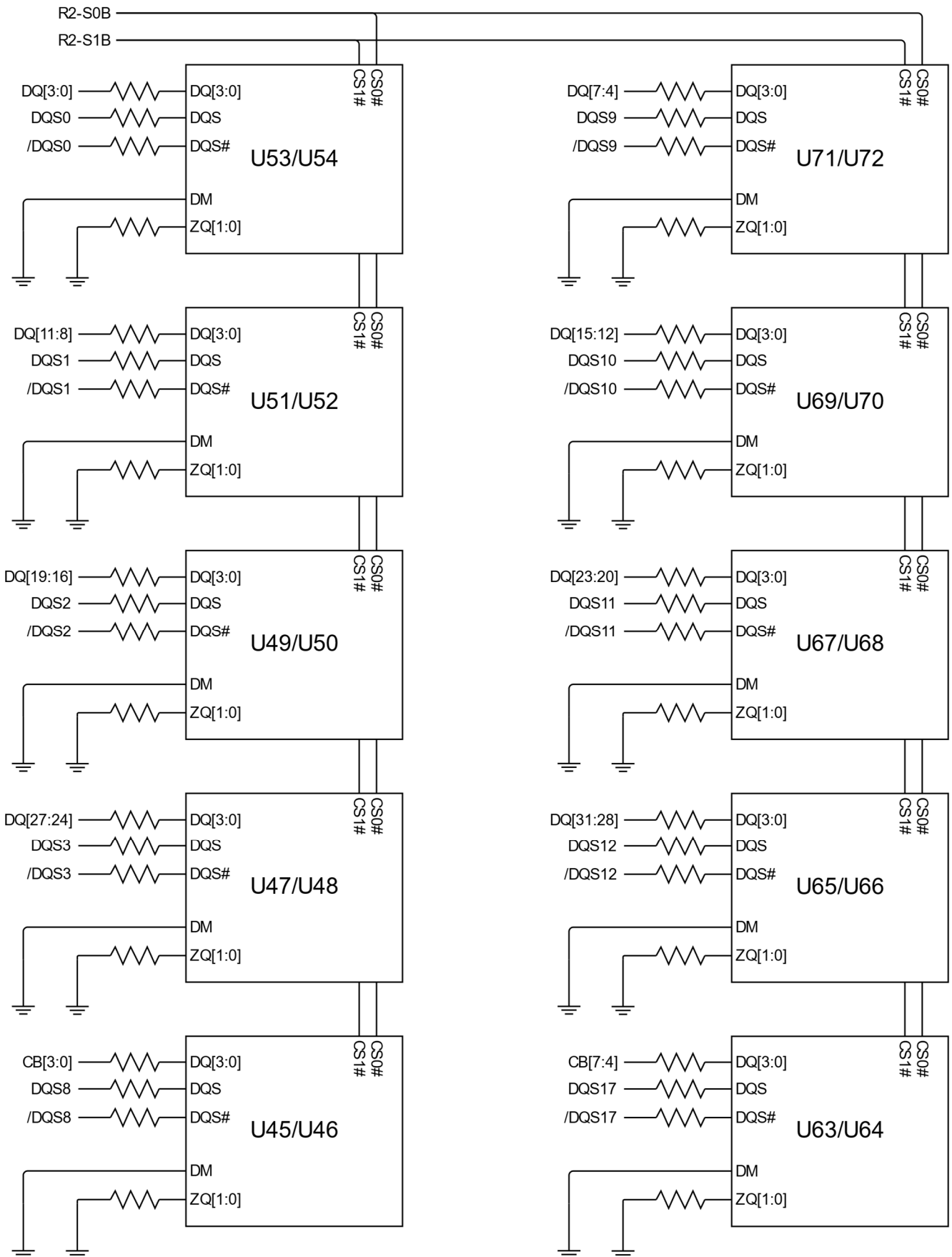


Figure 5 – Functional Block Diagram (Page 4 of 7)

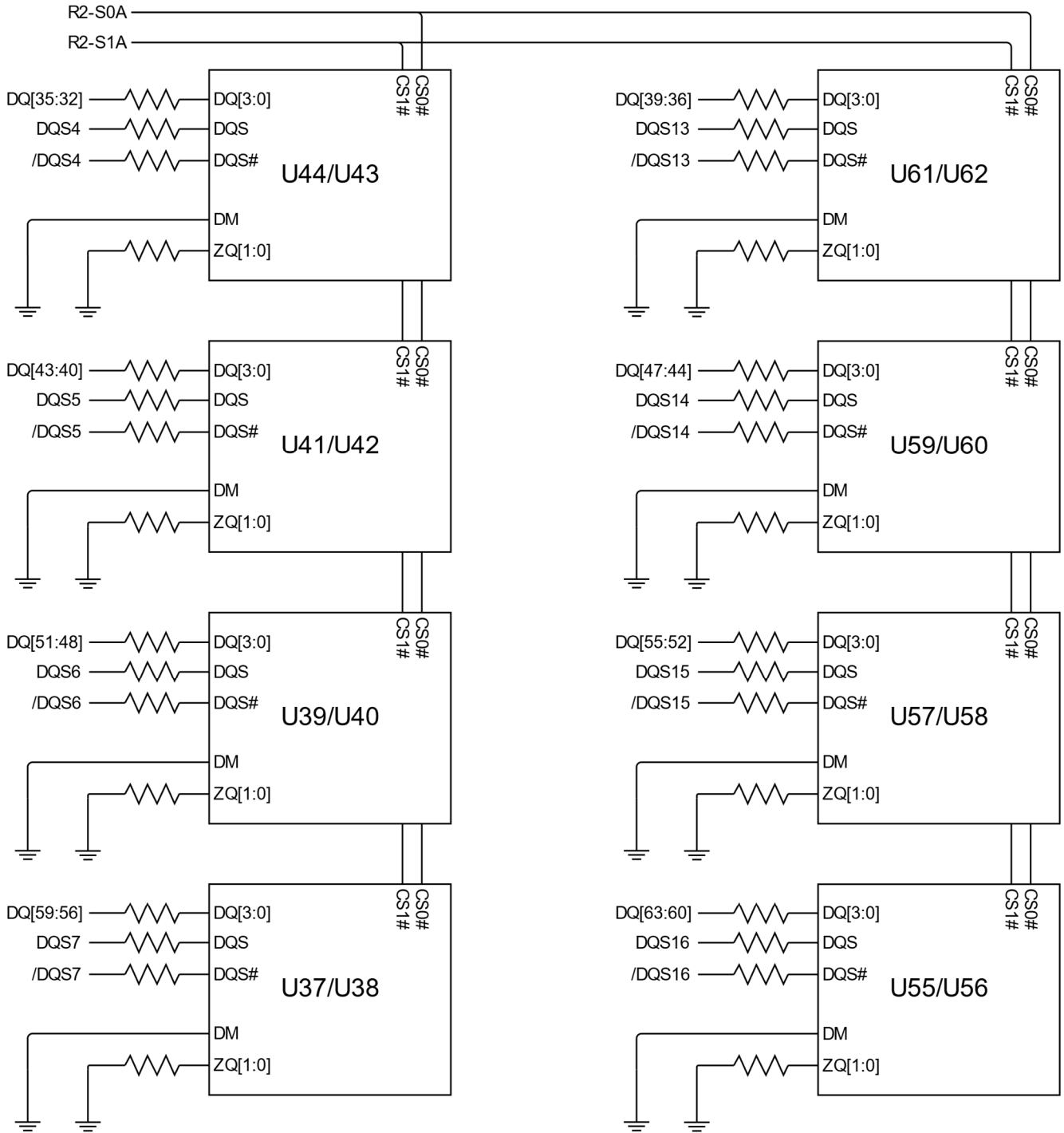
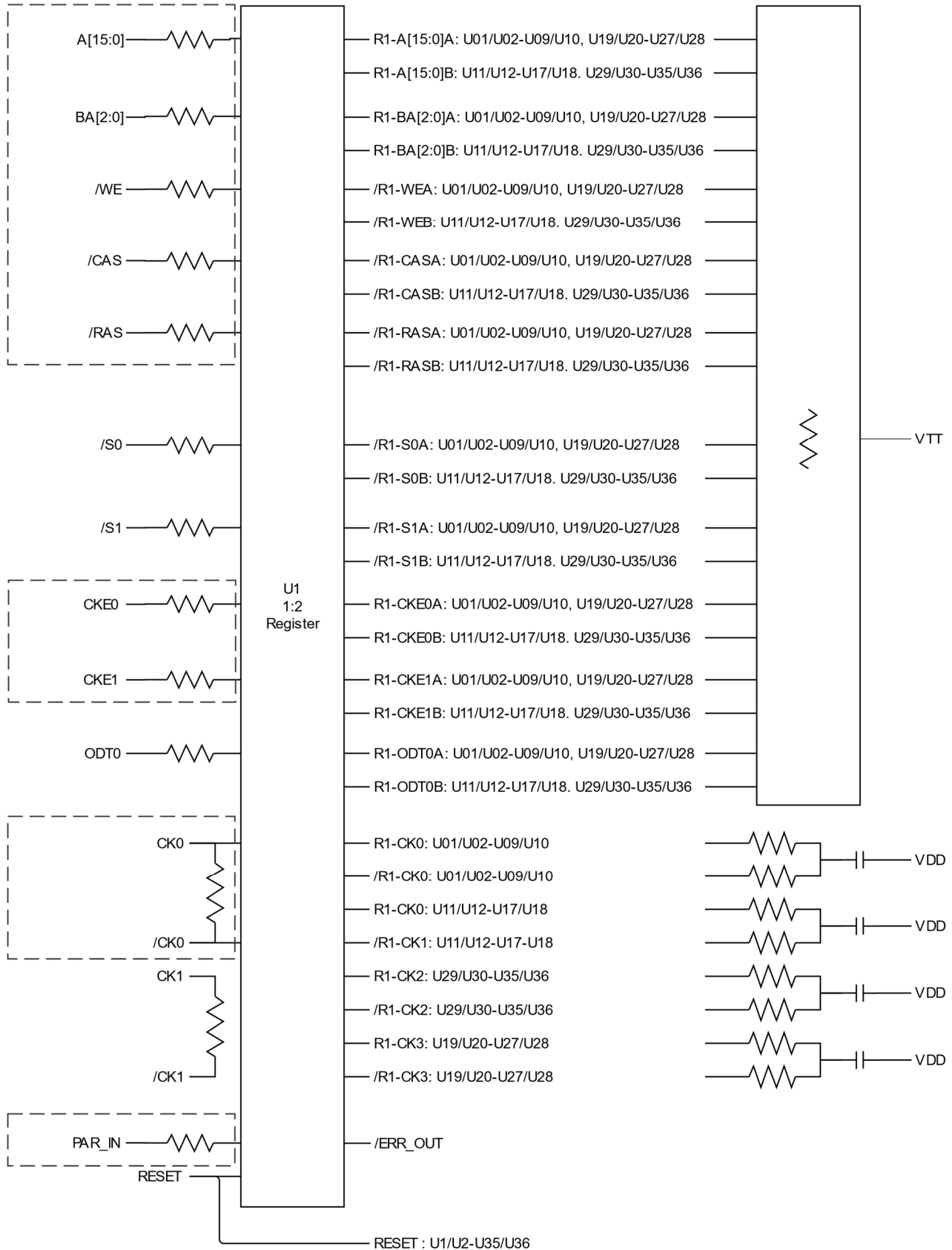
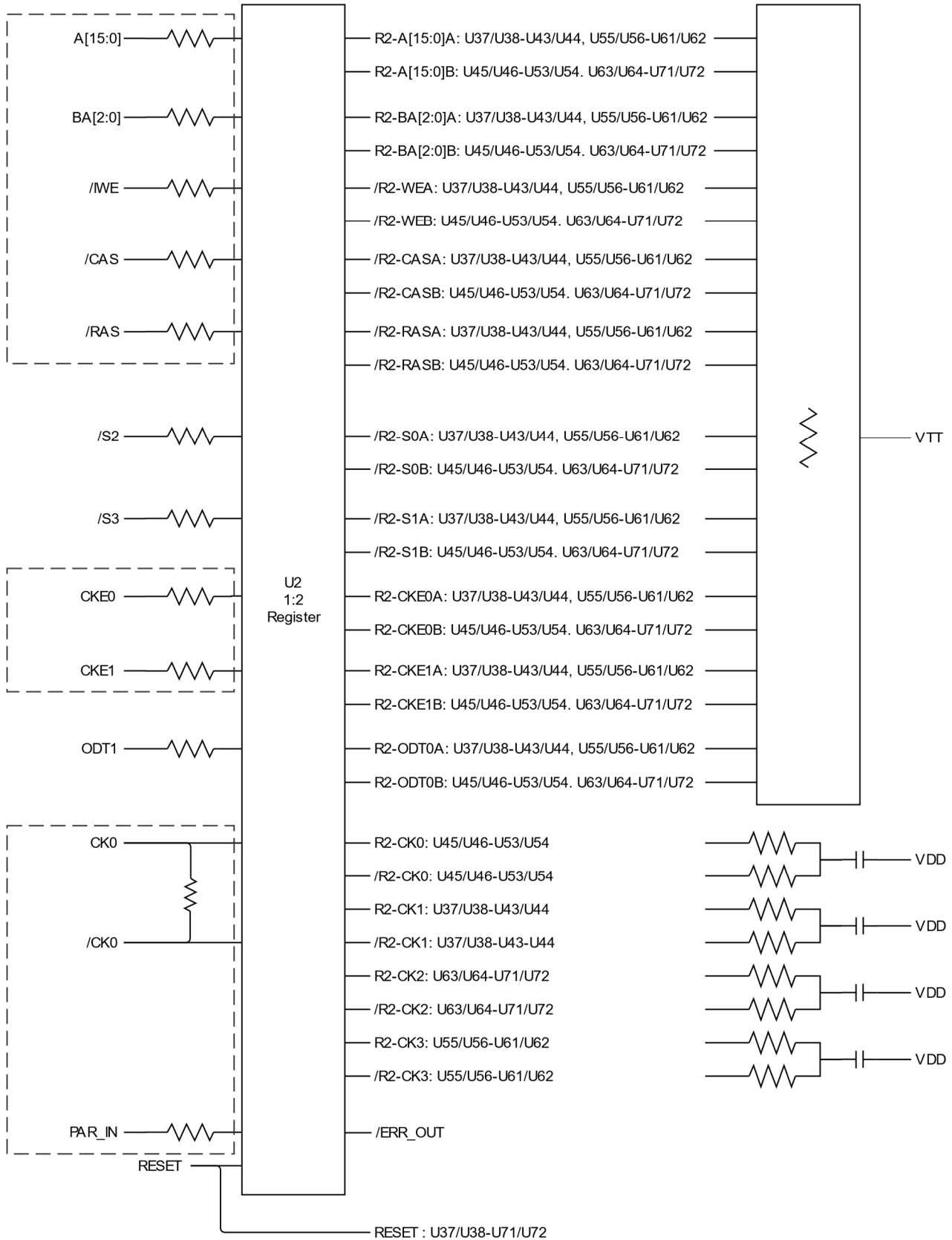


Figure 6 – Functional Block Diagram (Page 5 of 7)



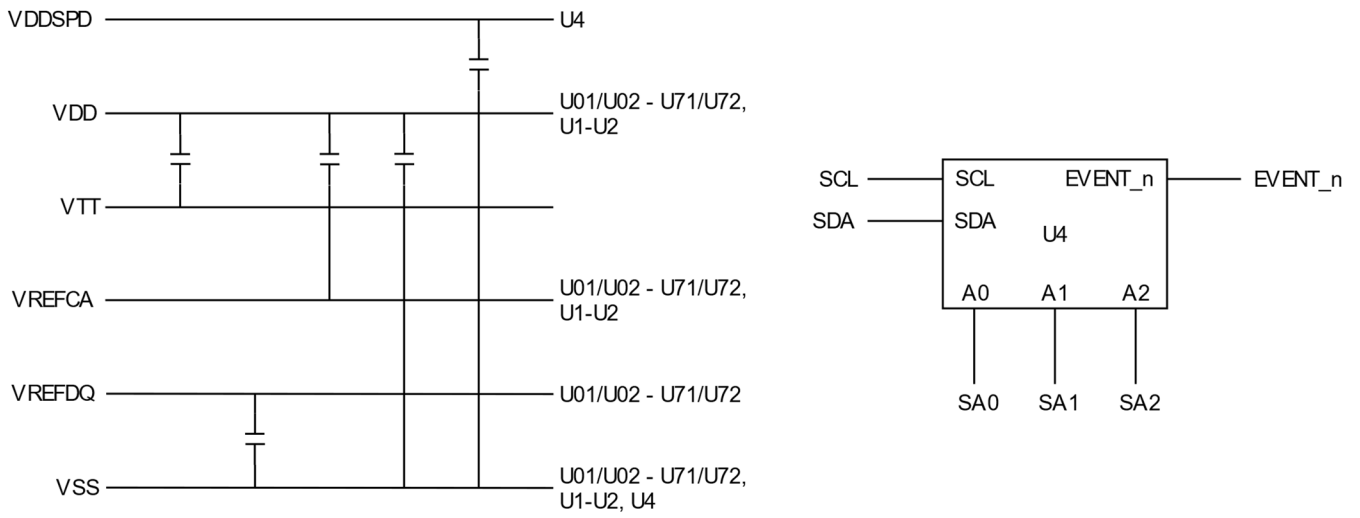
* Register input signals with the same name inside the dotted areas are the same signal, and shares series resistor for the single ended and differential termination resistor for the clock

Figure 7 – Functional Block Diagram (Page 6 of 7)



* Register input signals with the same name inside the dotted areas are the same signal, and shares series resistor for the single ended and differential termination resistor for the clock

Figure 8 – Functional Block Diagram (Page 7 of 7)



Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on V_{DD} , pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V_{DDQ} , pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 150	°C	1,2
DRAM Operation temperature for Commercial temperature product	T_{case}	0 ~ 95	°C	2,4,6
DRAM Operation temperature for Industrial temperature product	T_{case}	-40 ~ 95	°C	2,5,6

Notes:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JE51-2 standard.
- V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must not be greater than $0.6 \times V_{DDQ}$, when V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.
- The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.
- The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.
- Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval t_{REFI} to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1,2
I/O supply voltage	V_{DDQ}				V	1,2

Notes:

- V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD} . $V_{SS} = V_{SSQ}$.
- V_{DD} and V_{DDQ} may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
V_{IN} low; DC/commands/address buses	V_{IL}	V_{SS}	-	-0.100	V	
V_{IN} high; DC/commands/address buses	V_{IH}	0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	$0.49 * V_{DD}$	$0.50 * V_{DD}$	$0.51 * V_{DD}$	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	$0.49 * V_{DD}$	$0.50 * V_{DD}$	$0.51 * V_{DD}$	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	$0.50 * V_{DDQ}$	-	V	4

Notes:

- $V_{REFCA(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed $\pm 2\%$ of $V_{REFCA(DC)}$.
- DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
- $V_{REFDQ(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed $\pm 2\%$ of $V_{REFDQ(DC)}$.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition	Symbol	Value	Units
Command and Address			
Input high AC voltage: Logic 1 @ 175mV	DDR3-1066	$V_{IH(AC175)min}$	175 mV
Input high AC voltage: Logic 1 @ 150mV	DDR3-1066	$V_{IH(AC150)min}$	150 mV
Input high DC voltage: Logic 1 @ 100mV	DDR3-1066	$V_{IH(DC100)min}$	100 mV
Input low DC voltage: Logic 0 @ -100mV	DDR3-1066	$V_{IL(DC100)max}$	-100 mV
Input low AC voltage: Logic 0 @ -150mV	DDR3-1066	$V_{IL(AC150)max}$	-150 mV
Input low AC voltage: Logic 0 @ -175mV	DDR3-1066	$V_{IL(AC175)max}$	-175 mV

Parameter / Condition	Symbol	Value	Units
DQ and DM			
Input high AC voltage: Logic 1	DDR3-1066	$V_{IH(AC175)min}$	175 mV
Input high AC voltage: Logic 1	DDR3-1066	$V_{IH(AC150)min}$	150 mV
Input high AC voltage: Logic 1	DDR3-1066	$V_{IH(AC135)min}$	135 mV
Input high DC voltage: Logic 1	DDR3-1066	$V_{IH(DC100)min}$	100 mV
Input low DC voltage: Logic 0	DDR3-1066	$V_{IL(DC100)max}$	-100 mV
Input low AC voltage: Logic 0	DDR3-1066	$V_{IL(AC135)max}$	-135 mV
Input low AC voltage: Logic 0	DDR3-1066	$V_{IL(AC150)max}$	-150 mV
Input low AC voltage: Logic 0	DDR3-1066	$V_{IL(AC175)max}$	-175 mV

Notes:

1. All voltages are referenced to V_{REF} . V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
2. Input setup timing parameters (t_{IS} and t_{DS}) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (t_{IH} and t_{DH}) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high AC	$V_{IH,diff(AC)}$	$2 * (V_{IH(AC)} - V_{REF})$	-	mV	2
Differential input voltage logic low AC	$V_{IL,diff(AC)}$	-	$2 * (V_{IL(AC)} - V_{REF})$	mV	3
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2 + 175$	-	mV	
Single-ended high level for CK, /CK		$V_{DD}/2 + 175$	-	mV	
Single-ended low level for strobes	V_{SEL}	-	$V_{DDQ}/2 - 175$	mV	
Single-ended low level for CK, /CK		-	$V_{DD}/2 - 175$	mV	

Notes:

1. Defines slew rate reference points, relative to input crossing voltages.
2. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
3. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{TT} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{TT} + 0.1 * V_{DDQ}$	SRQ_{se}	2.5	5	V/ns	1,2,3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 * V_{DDQ}$		V	1,2
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	$0.5 * V_{DDQ}$		V	1,2
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 * V_{DDQ}$		V	1,2
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 * V_{DDQ}$		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 * V_{DDQ}$		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
2. $V_{TT} = V_{DDQ}/2$.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = $-0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	$+0.2 * V_{DDQ}$		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	$-0.2 * V_{DDQ}$		V	1
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

1. RZQ of 240Ω ($\pm 1\%$) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
2. $V_{REF} = V_{DDQ}/2$; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM4G72D3RDQ4AG-D187E(I)

Table 17 - I_{DD} Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I _{DD0}	1674	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I _{DD1}	1818	mA	1, 2
Precharge power-down current; Slow exit	I _{DD2P0}	576	mA	1, 3
Precharge power-down current; Fast exit	I _{DD2P1}	792	mA	1, 3
Precharge quiet standby current	I _{DD2Q}	1152	mA	1, 3
Precharge standby current	I _{DD2N}	1152	mA	1, 3
Precharge standby ODT current	I _{DD2NT}	1224	mA	1, 2
Active power-down current	I _{DD3P}	1224	mA	1, 3
Active standby current	I _{DD3N}	1368	mA	1, 3
Burst read operating current	I _{DD4R}	2394	mA	1, 2
Burst write operating current	I _{DD4W}	2430	mA	1, 2
Refresh current	I _{DD5B}	4950	mA	1, 2
Self refresh temperature current: MAX T _{case} = 85°C	I _{DD6}	720	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T _{case} = 95°C	I _{DD6ET}	864	mA	1, 3
All banks interleaved read current	I _{DD7}	3060	mA	1, 2
Reset current	I _{DD8}	720	mA	1, 3

Notes:

1. Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.
2. One module rank in the active I_{DD}, the other rank in I_{DD2N}.
3. All DRAM in this I_{DD} conditions.

For part number IMM4G72D3RDQ4AG-D187E(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	Tcase = 0°C to 85°C	t _{CK(DLL_DIS)}	8	-	ns
	Tcase => 85°C to 95°C		8	-	
Clock periods average: DLL enable mode (CL = 7, CWL = 5)		t _{CK(avg)}	1.875	2.5	ns
High pulse width average		t _{CH(avg)}	0.47	0.53	t _{CK(avg)}
Low pulse width average		t _{CL(avg)}	0.47	0.53	t _{CK(avg)}
Clock period jitter	DLL locked	t _{JITper}	-90	90	ps
	DLL locking	t _{JIT(per,lock)}	-80	80	ps
Clock absolute period		t _{CK(abs)}	t _{CK(avg) Min} + t _{JITper Min}	t _{CK(avg) Max} + t _{JITper Max}	ps
Clock absolute high pulse width		t _{CH(abs)}	0.43	-	t _{CK(avg)}
Clock absolute low pulse width		t _{CL(abs)}	0.43	-	t _{CK(avg)}
Cycle-to-cycle jitter	DLL locked	t _{JITcc}	-	180	ps
	DLL locking	t _{JIT(cc,lock)}	-	160	ps
Cumulative error across	2 cycles	t _{ERR(2per)}	-132	132	ps
	3 cycles	t _{ERR(3per)}	-157	157	ps
	4 cycles	t _{ERR(4per)}	-175	175	ps
	5 cycles	t _{ERR(5per)}	-188	188	ps
	6 cycles	t _{ERR(6per)}	-200	200	ps
	7 cycles	t _{ERR(7per)}	-209	209	ps
	8 cycles	t _{ERR(8per)}	-217	217	ps
	9 cycles	t _{ERR(9per)}	-224	224	ps
	10 cycles	t _{ERR(10per)}	-231	231	ps
	11 cycles	t _{ERR(11per)}	-237	237	ps
	12 cycles	t _{ERR(12per)}	-242	242	ps
		n = 13,...49, 50 cycles	t _{ERR(nper)}	(1+0.68ln[n]) * t _{JITper Min}	(1+0.68ln[n]) * t _{JITper Max}
DQ Input Timing					
Data setup time to DQS, /DQS	Base (specification)	t _{DS(AC175)}	25	-	ps
Data setup time to DQS, /DQS	Base (specification)	t _{DS(AC150)}	75	-	ps
Data hold time from DQS, /DQS	Base (specification)	t _{DH(DC100)}	100	-	ps
Minimum data pulse width		t _{DIPW}	490	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		t _{DQSQ}	-	150	ps
DQ output hold time from DQS, /DQS		t _{QH}	0.38	-	t _{CK(avg)}
DQ Low-Z time from CK, /CK		t _{LZ(DQ)}	-600	300	ps
DQ High-Z time from CK, /CK		t _{HZ(DQ)}	-	300	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		t _{DQSS}	-0.25	0.25	t _{CK(avg)}
DQS, /DQS differential input low pulse width		t _{DQSL}	0.45	0.55	t _{CK(avg)}
DQS, /DQS falling setup to CK, /CK rising		t _{DSS}	0.2	-	t _{CK(avg)}
DQS, /DQS falling hold from CK, /CK rising		t _{DSSH}	0.2	-	t _{CK(avg)}
DQS, /DQS differential input high pulse width		t _{DQSH}	0.45	0.55	t _{CK(avg)}
DQS, /DQS differential WRITE preamble		t _{WPRE}	0.9	-	t _{CK(avg)}
DQS, /DQS differential WRITE postamble		t _{WPST}	0.3	-	t _{CK(avg)}

For part number IMM4G72D3RDQ4AG-D187E(I)

Parameter / Condition		Symbol	Min	Max	Units
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		t_{DQSCK}	-300	300	ps
DQS, /DQS differential output high time		t_{QSH}	0.38	-	$t_{CK}(avg)$
DQS, /DQS differential output low time		t_{QSL}	0.38	-	$t_{CK}(avg)$
DQS, /DQS Low-Z time (RL-1)		$t_{LZ}(DQS)$	-600	300	ps
DQS, /DQS High-Z time (RL+BL/2)		$t_{HZ}(DQS)$	-	300	ps
DQS, /DQS differential READ preamble		t_{RPRE}	0.9	-	$t_{CK}(avg)$
DQS, /DQS differential READ postamble		t_{RPST}	0.3	-	$t_{CK}(avg)$
Command and Address Timing					
DLL locking time		t_{DLLK}	512	-	nCK
CTRL, CMD, ADDR setup to CK, /CK	Base (specification)	$t_{IS}(AC175)$	125	-	ps
CTRL, CMD, ADDR setup to CK, /CK	Base (specification)	$t_{IS}(AC150)$	275	-	ps
CTRL, CMD, ADDR hold from CK, /CK	Base (specification)	$t_{IH}(DC100)$	200	-	ps
Minimum CTRL, CMD, ADDR pulse width		t_{IPW}	780	-	ps
ACTIVATE to internal READ or WRITE delay		t_{RCD}	13.125	-	ns
PRECHARGE command period		t_{RP}	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		t_{RAS}	37.5	$9 * t_{REFI}$	ns
ACTIVATE-to-ACTIVATE command period		t_{RC}	50.625	-	ns
ACTIVATE-to-ACTIVATE minimum period (1KB page size)		t_{RRD}	greater of 4nCK or 7.5ns	-	-
ACTIVATE-to-ACTIVATE minimum period (2KB page size)		t_{RRD}	greater of 4nCK or 10ns	-	-
Four ACTIVATE windows (1KB page size)		t_{FAW}	37.5	-	ns
Four ACTIVATE windows (2KB page size)		t_{FAW}	50	-	ns
Write recovery time		t_{WR}	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		t_{WTR}	greater of 4nCK or 7.5ns	-	-
READ-to-PRECHARGE time		t_{RTP}	greater of 4nCK or 7.5ns	-	-
/CAS-to-/CAS command delay		t_{CCD}	4	-	nCK
Auto precharge write recovery + precharge time		t_{DAL}	$WR + t_{RP} / t_{CK}(avg)$	-	nCK
MODE REGISTER SET command cycle time		t_{MRD}	4	-	nCK
MODE REGISTER SET command update delay		t_{MOD}	greater of 12nCK or 15ns	-	-
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		t_{MPRR}	1	-	nCK
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	t_{ZQinit}	greater of 512nCK or 640ns	-	-
	Normal operation	t_{ZQoper}	greater of 256nCK or 320ns	-	-
ZQCS command: Short calibration time		t_{ZQCS}	greater of 64nCK or 80ns	-	-
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		t_{XPR}	greater of 5nCK or $t_{RFC}(min)+10ns$	-	-
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		t_{RFC}	260	-	ns

For part number IMM4G72D3RDQ4AG-D187E(I)

Parameter / Condition		Symbol	Min	Max	Units
Maximum refresh period	T _{case} ≤ 85°C	-	64 (1X)		ms
	T _{case} > 85°C		32 (2X)		
Maximum average periodic refresh	T _{case} ≤ 85°C	t _{REFI}	7.8 (64ms/8192)		us
	T _{case} > 85°C		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		t _{XS}	greater of 5 nCK or t _{RFC} Min+10ns	-	-
Exit self refresh to commands requiring a locked DLL		t _{XSDLL}	t _{DLLK} Min	-	nCK
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		t _{CKESR}	t _{CKE} Min + 1nCK	-	-
Valid clocks after self refresh entry or power down entry		t _{CKSRE}	greater of 5nCK or 10ns	-	-
Valid clocks before self refresh exit, power-down exit, or reset exit		t _{CKSRX}	greater of 5nCK or 10ns	-	-
Power-Down Timing					
CKE MIN pulse width		t _{CKE}	greater of 3nCK or 7.5ns	-	-
Command pass disable delay		t _{CPDED}	1	-	nCK
Power-down entry to power exit timing		t _{PD}	t _{CKE} Min	9 * t _{REFI}	-
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		t _{ACTPDEN}	1	-	nCK
PRECHARGE/PRECHARGE ALL command to power-down entry		t _{PRPDEN}	1	-	nCK
REFRESH command to power-down entry		t _{REFPDEN}	1	-	nCK
MRS command to power-down entry		t _{MRSPDEN}	t _{MOD} Min	-	nCK
READ/READ with auto precharge command to power-down entry		t _{RDPDEN}	RL + 4 + 1	-	nCK
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	t _{WRPDEN}	WL + 4 + t _{WR} /t _{CK} (avg)	-	nCK
	BC4MRS	t _{WRPDEN}	WL + 2 + t _{WR} /t _{CK} (avg)	-	nCK
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	t _{WRAPDEN}	WL + 4 + t _{WR} + 1	-	nCK
	BC4MRS	t _{WRAPDEN}	WL + 2 + t _{WR} + 1	-	nCK
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		t _{XP}	greater of 3nCK or 7.5ns	-	-
Precharge power-down with DLL off to commands requiring a locked DLL		t _{XPDLL}	greater of 10nCK or 24ns	-	-
ODT Timing					
RTT turn-on from ODTL on reference		t _{AON}	-300	300	ps
RTT turn-off from ODTL off reference		t _{AOFF}	0.3	0.7	t _{CK} (avg)
Asynchronous RTT turn-on delay (power-down with DLL off)		t _{AOONPD}	2	8.5	ns
Asynchronous RTT turn-off delay (power-down with DLL off)		t _{AOFFPD}	2	8.5	ns
ODT HIGH time with WRITE command and BL8		ODTH8	6	-	nCK
ODT HIGH time without WRITE command or WRITE command and BC4		ODTH4	4	-	nCK
Dynamic ODT Timing					
RTT dynamic change skew		t _{ADC}	0.3	0.7	t _{CK} (avg)
Write Leveling Timing					
First DQS, /DQS rising edge		t _{WLMRD}	40	-	nCK
DQS, /DQS delay		t _{WLDQSEN}	25	-	nCK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing		t _{WLS}	245	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing		t _{WLH}	245	-	ps
Write leveling output delay		t _{WLO}	0	9	ns
Write leveling output error		t _{WLOE}	0	2	ns

For part number IMM4G72D3RDQ4AG-D187E(I)

Table 19 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of SPD Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116	92
1	SPD Revision	Revision 1.2	12
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	Registered DIMM	01
4	SDRAM Density and Banks	4Gbits, 8banks	04
5	SDRAM Addressing	Row 16, Col 11	22
6	Module Nominal Voltage, V _{DD}	1.5V	00
7	Module Organization	4 Ranks, 4bits	18
8	Module Memory Bus Width	ECC, 72bits	0B
9	Fine Timebase (FTB) Dividend / Divisor	2.5ps	52
10	Medium Timebase (MTB) Dividend	1ns	01
11	Medium Timebase (MTB) Divisor	8	08
12	SDRAM Minimum Cycle Time (t _{CKmin})	1.875ns	0F
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	5,6,7,8	1E
15	CAS Latencies Supported, Most Significant Byte	-	00
16	Minimum CAS Latency Time (t _{AAmin})	13.125ns	69
17	Minimum Write Recovery Time (t _{WRmin})	15ns	78
18	Minimum RAS# to CAS# Delay Time (t _{RCDmin})	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (t _{RRDmin})	7.5ns	3C
20	Minimum Row Precharge Time (t _{RPmin})	13.125ns	69
21	Upper Nibbles for t _{RAS} and t _{RC}	-	11
22	Minimum Active to Precharge Time (t _{RASmin}), Least Significant Byte	37.5ns	2C
23	Minimum Active to Active/Refresh Time (t _{RCmin}), Least Significant Byte	50.625ns	95
24	Minimum Refresh Recovery Time (t _{RFCmin}), Least Significant Byte	260ns	20
25	Minimum Refresh Recovery Time (t _{RFCmin}), Most Significant Byte	-	08
26	Minimum Internal Write to Read Command Delay Time (t _{WTRmin})	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (t _{RTPmin})	7.5ns	3C
28	Upper Nibble for t _{FAW}	-	01
29	Minimum Four Activate Window Delay Time (t _{FAWmin})	37.5ns	2C
30	SDRAM Optional Features	DLL off, RZQ/7, RZQ/6	83
31	SDRAM Thermal and Refresh Options	ASR, 0°C=95°C, req. 2x Refresh	05
32	Module Thermal Sensor	Thermal Sensor incorporated	80
33	SDRAM Device Type	Dual Die Package	A1
34	Fine Offset for SDRAM Minimum Cycle Time (t _{CKmin})	-0ns	00
35	Fine Offset for Minimum CAS Latency Time (t _{AAmin})	-0ns	00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (t _{RCDmin})	-0ns	00
37	Fine offset for minimum Row Precharge Delay Time (t _{RPmin})	-0ns	00

Byte NO.	Description	Note	Hex
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (t_{RCmin})	-0ns	00
39-40	Reserved, General Section	-	00
41	SDRAM Maximum Activate Count (MAC) Value	8192* t_{REFI} , Untested MAC	00
42-59	Reserved, General Section	-	00
60	Raw Card Extension, Module Nominal Height	29< Height <=30 mm	0F
61	Module Maximum Thickness	1< tF <=2 mm, 1< tB <=2 mm	11
62	Reference Raw Card	Raw card AB1	35
63	DIMM Module Attributes	2 Rows DRAM, 2 Registers	0A
64	RDIMM Thermal Heat Spreader Solution	No Heat Spreader incorporated	00
65-66	Register Manufacturer's JEDEC ID Code	-	00
67	Register Revision Number	Undefined	FF
68	Register Type	SSTE32882	00
69	RC1 (MS Nibble) / RC0 (LS Nibble)	-	00
70	RC3 (MS nibble) / RC2 (LS Nibble) – Drive Strength, Command/Address	Moderate Drive	50
71	RC5 (MS Nibble) / RC4 (LS Nibble) – Drive Strength, Control and Clock	Clock: Moderate Drive, Control: Light Drive	50
72	RC7 (MS Nibble) / RC6 (LS Nibble)	-	00
73	RC9 (MS Nibble) / RC8 (LS Nibble)	-	08
74	RC11 (MS Nibble) / RC10 (LS Nibble)	-	00
75	RC13 (MS Nibble) / RC12 (LS Nibble)	-	00
76	RC15 (MS Nibble) / RC14 (LS Nibble)	-	00
77-116	Reserved	-	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	I'M	04 9E
119	Module ID: Module Manufacturing Location	-	00
120-121	Module ID: Module Manufacturing Date	Manufacturer's data	-
122-125	Module ID: Module Serial Number	Manufacturer's data	-
126-127	SPD Cyclical Redundancy Code (CRC)	-	D3 28
128-145	Module Part Number	Manufacturer's data	-
146-147	Module Revision Code	-	00
148-149	DRAM Manufacturer's JEDEC ID Code	-	00
150-175	Manufacturer's Specific Data	Manufacturer's data	-
176-255	Open for Customer Use	-	00

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	May, 2021
2.0	Revise SPD Description in Table 19	Jun, 2021

Contents

Features	2
Table 1 - Ordering Information for RoHS Compliant Product	3
Table 2 - Operating Voltage	3
Table 3 – Temperature Grade	3
Table 4 – Speed Grade	3
Table 5 – Memory Chip Information	3
Part Number Decoder	4
Table 6 - Addressing	4
Table 7 - Pin Assignment	5
Table 8 - Pin Description	6
Module Dimension	7
Figure 1 – 240 Pin DDR3 SDRAM Registered DIMM	7
Table 9 - PCB Dimension	7
Figure 2 – Functional Block Diagram (Page 1 of 7)	8
Figure 3 – Functional Block Diagram (Page 2 of 7)	9
Figure 4 – Functional Block Diagram (Page 3 of 7)	10
Figure 5 – Functional Block Diagram (Page 4 of 7)	11
Figure 6 – Functional Block Diagram (Page 5 of 7)	12
Figure 7 – Functional Block Diagram (Page 6 of 7)	13
Figure 8 – Functional Block Diagram (Page 7 of 7)	14
Electrical Parameter	15
Table 10 - Absolute Maximum DC Ratings	15
Table 11 - DC Electrical Characteristics and Operating Conditions	15
Table 12 - DC Electrical Characteristics and Input Conditions	16
Table 13 - Input Switching Conditions	17
Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)	18
Table 15 - Single-Ended Output Driver Characteristics	18
Table 16 - Differential Output Driver Characteristics	19
Table 17 - I _{DD} Specifications with Conditions and Operation Current	20
Table 18 - AC Timing Parameter and Operating Conditions	21
Table 19 - SPD Information	24
Revision History	26
Contents	27
List of Tables	28
List of Figures	28

List of Tables

Table 1 - Ordering Information for RoHS Compliant Product	3
Table 2 - Operating Voltage	3
Table 3 – Temperature Grade	3
Table 4 – Speed Grade	3
Table 5 – Memory Chip Information	3
Table 6 - Addressing	4
Table 7 - Pin Assignment	5
Table 8 - Pin Description	6
Table 9 - PCB Dimension	7
Table 10 - Absolute Maximum DC Ratings	15
Table 11 - DC Electrical Characteristics and Operating Conditions	15
Table 12 - DC Electrical Characteristics and Input Conditions	16
Table 13 - Input Switching Conditions	17
Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)	18
Table 15 - Single-Ended Output Driver Characteristics	18
Table 16 - Differential Output Driver Characteristics	19
Table 17 - I _{DD} Specifications with Conditions and Operation Current	20
Table 18 - AC Timing Parameter and Operating Conditions	21
Table 19 - SPD Information	24

List of Figures

Figure 1 – 240 Pin DDR3 SDRAM Registered DIMM	7
Figure 2 – Functional Block Diagram (Page 1 of 7)	8
Figure 3 – Functional Block Diagram (Page 2 of 7)	9
Figure 4 – Functional Block Diagram (Page 3 of 7)	10
Figure 5 – Functional Block Diagram (Page 4 of 7)	11
Figure 6 – Functional Block Diagram (Page 5 of 7)	12
Figure 7 – Functional Block Diagram (Page 6 of 7)	13
Figure 8 – Functional Block Diagram (Page 7 of 7)	14