Datasheet | Rev. 2.0 | 2021

IMM4G72D3(L)LRQ4AG (Die Revision D)
32GByte (4G x 72 Bit)

32GB DDR3 Load Reduced DIMM
RoHS Compliant Product

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures.

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Features

- 240-Pin Load Reduced Dual-In-Line Memory Module
- Capacity: 32GB
- Memory Buffer
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC3-12800: 5, 6, 7, 8, 9, 10, 11
  - PC3-10600: 5, 6, 7, 8, 9, 10
- Programmable CAS Write Latency (CWL):
  - PC3-12800: 5, 6, 7, 8
  - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.35mm (1.19inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM4G72D3xLRQ4AG-Dzzzy	32GB	4Gx72	4	32GB DDR3 Load Reduced DIMM

Notes:
x: Operating Voltage
y: Operating Temperature
zzz: Speed Grade

Table 2 - Operating Voltage

Part Number	Operating Voltage
Blank	V_{DD}, V_{DDQ} = 1.5V (1.425V-1.575V)
L	V_{DD}, V_{DDQ} = 1.35V (1.283V-1.45V) Backward compatible to V_{DD}, V_{DDQ} = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade

Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < T_{case} <= 95 °C.

Table 4 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM4G72D3(L)LRQ4AG-Dzzzy	I'M	IM8G04D3FDDG	1.35V/1.5V	1Gx4x2 DDP	Lead Free

Part Number Decoder

IM M 4G72 D3 (L) LR Q 4 A G - D 125 (I)

I'M Module

DRAM Brand
M = I'M

Module Configuration
4G72 = 4Gx72 (32GB)

Memory Type
D3 = DDR3

DDR3L option
Blank = 1.5V
L = 1.35V (1.5V Compatible)

Module Form-Factor
LR = Load Reduced DIMM (LRDIMM)

Number of Ranks
Q = Quad Rank

DRAM Bit width
4 = using x4 components

Module PCB Revision
A = Revision A

RoHS compliance
G = Green / RoHS

IC Revision
D = Revision D

Speed Grade
125 = DDR3-1600 CL11
15E = DDR3-1333 CL9

Temperature Grade
Blank = Commercial Temperature (0°C to 95°C T_{case})
I = Industrial Temperature (-40°C to 95°C T_{case})

Table 6 - Addressing

Parameter	32GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1Gx4x2 DDP)
Column address	2K A[9:0], A11
Module rank address	4 /S[3:0]
Number of devices	36

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{REFDQ}	121	V_{SS}	61	A2	181	A1
2	V_{SS}	122	D4	62	V_{DD}	182	V_{DD}
3	D0	123	D5	63	CK1	183	V_{DD}
4	D1	124	V_{SS}	64	/CK1	184	CK0
5	V_{SS}	125	DQS9	65	V_{DD}	185	/CK0
6	/DQS0	126	/DQS9	66	V_{DD}	186	V_{DD}
7	DQS0	127	V_{SS}	67	V_{REFCA}	187	/EVENT
8	VSS	128	D6	68	PAR_IN	188	A0
9	D2	129	D7	69	V_{DD}	189	V_{DD}
10	D3	130	V_{SS}	70	A10, AP	190	BA1
11	V_{SS}	131	D12	71	BA0	191	V_{DD}
12	D8	132	D13	72	V_{DD}	192	/RAS
13	D9	133	V_{SS}	73	/WE	193	/S0
14	V_{SS}	134	DQS10	74	/CAS	194	V_{DD}
15	/DQS1	135	/DQS10	75	V_{DD}	195	ODT0
16	DQS1	136	V_{SS}	76	/S1	196	A13
17	V_{SS}	137	D14	77	ODT1, CKE3	197	V_{DD}
18	D10	138	D15	78	V_{DD}	198	/S3
19	D11	139	V_{SS}	79	/S2	199	V_{SS}
20	V_{SS}	140	D20	80	V_{SS}	200	D36
21	D16	141	D21	81	D32	201	D37
22	D17	142	V_{SS}	82	D33	202	V_{SS}
23	V_{SS}	143	DQS11	83	V_{SS}	203	DQS13
24	/DQS2	144	/DQS11	84	/DQS4	204	/DQS13
25	DQS2	145	V_{SS}	85	DQS4	205	V_{SS}
26	V_{SS}	146	D22	86	V_{SS}	206	D38
27	D18	147	D23	87	D34	207	D39
28	D19	148	V_{SS}	88	D35	208	V_{SS}
29	V_{SS}	149	D28	89	V_{SS}	209	D44
30	D24	150	D29	90	D40	210	D45
31	D25	151	V_{SS}	91	D41	211	V_{SS}
32	V_{SS}	152	DQS12	92	V_{SS}	212	DQS14
33	/DQS3	153	/DQS12	93	/DQS5	213	/DQS14
34	DQS3	154	V_{SS}	94	DQS5	214	V_{SS}
35	V_{SS}	155	D30	95	V_{SS}	215	D46
36	D26	156	D31	96	D42	216	D47
37	D27	157	V_{SS}	97	D43	217	V_{SS}
38	V_{SS}	158	CB4	98	V_{SS}	218	D52
39	CB0	159	CB5	99	D48	219	D53
40	CB1	160	V_{SS}	100	D49	220	V_{SS}
41	V_{SS}	161	DQS17	101	V_{SS}	221	DQS15
42	/DQS8	162	/DQS17	102	/DQS6	222	/DQS15
43	DQS8	163	V_{SS}	103	DQS6	223	V_{SS}
44	V_{SS}	164	CB6	104	V_{SS}	224	D54
45	CB2	165	CB7	105	D50	225	D55
46	CB3	166	V_{SS}	106	D51	226	V_{SS}
47	V_{SS}	167	CKE2	107	V_{SS}	227	D60
48	V_{TT}	168	/RESET	108	D56	228	D61
49	V_{TT}	169	CKE1	109	D57	229	V_{SS}
50	CKE0	170	V_{DD}	110	V_{SS}	230	DQS16
51	V_{DD}	171	A15	111	/DQS7	231	/DQS16
52	BA2	172	A14	112	DQS7	232	V_{SS}
53	/ERR_OUT	173	V_{DD}	113	V_{SS}	233	D62
54	V_{DD}	174	A12, /BC	114	D58	234	D63
55	A11	175	A9	115	D59	235	V_{SS}
56	A7	176	V_{DD}	116	V_{SS}	236	V_{DDSPD}
57	V_{DD}	177	A8	117	SA0	237	SA1
58	A5	178	A6	118	SCL	238	SDA
59	A4	179	V_{DD}	119	SA2	239	V_{SS}
60	V_{DD}	180	A3	120	V_{TT}	240	V_{TT}

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM core power supply	V_{REFDQ}	SDRAM I/O reference supply
V_{REFCA}	SDRAM command/address reference supply	V_{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE3	SDRAM clock enable lines
/S0-/S3	DIMM rank select lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS17	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS17	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	CB0-CB7	Data check bits input/output
SCL	EEPROM clock	SDA	EEPROM data line
SA0-SA2	EEPROM address input	V_{DDSPD}	EEPROM positive power supply
PAR_IN	Parity input	/EVENT	Temperature event
/ERR_OUT	Parity error output	/RESET	Register and SDRAM control pin
V_{TT}	Termination voltage	NC	Spare pins (no connect)

Module Dimension

Figure 1 - 240 Pin DDR3 SDRAM Load Reduced DIMM

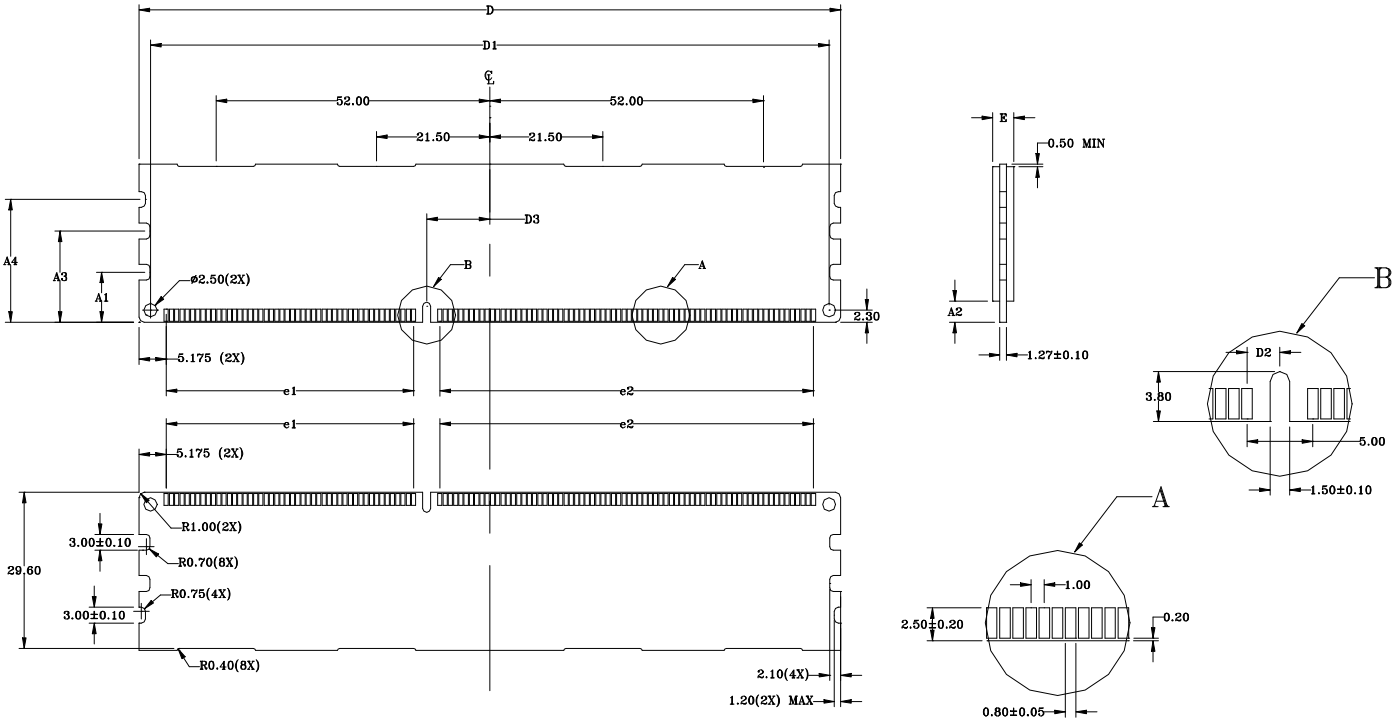


Table 9 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	30.20	30.35	30.50
A1		9.50 Basic	
A2	4.00		
A3		17.30 Basic	
A4		23.30 Basic	
D	133.20	133.35	133.50
D1		128.95 Basic	
D2		2.50 Basic	
D3		12.00 Basic	
e1		47.00 Basic	
e2		71.00 Basic	
E			4.80

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 - Functional Block Diagram (Page 1 of 6)

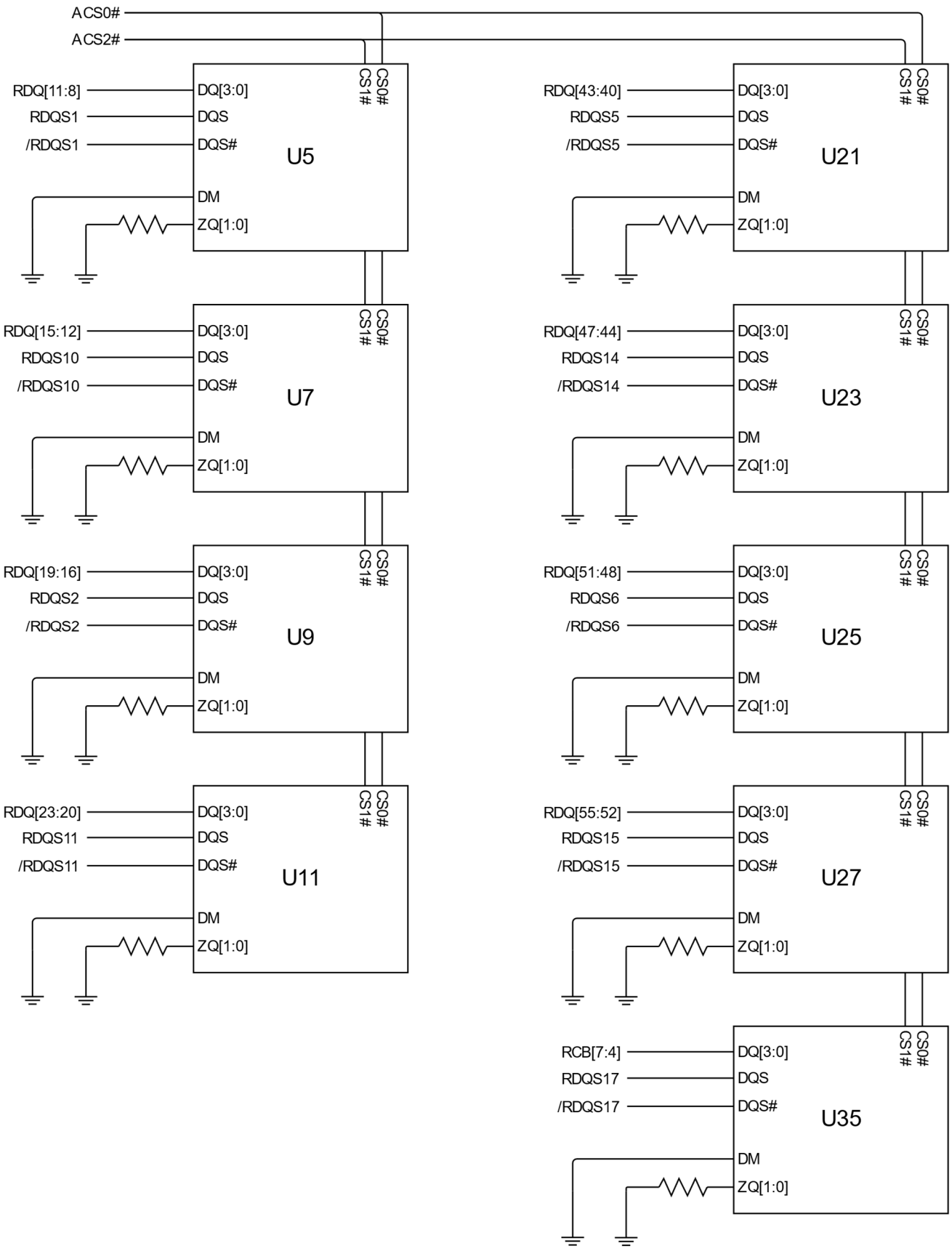


Figure 3 - Functional Block Diagram (Page 2 of 6)

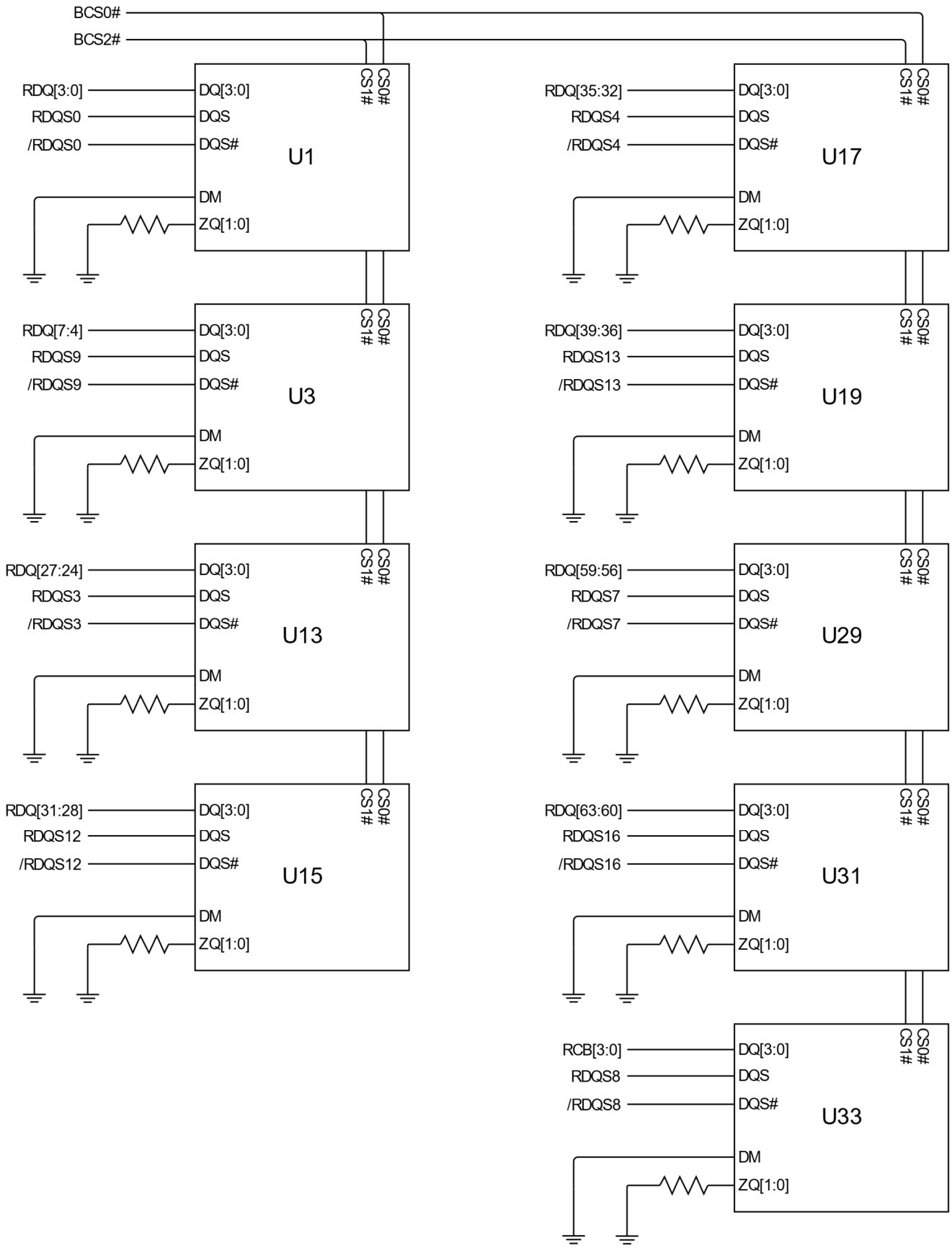


Figure 4 - Functional Block Diagram (Page 3 of 6)

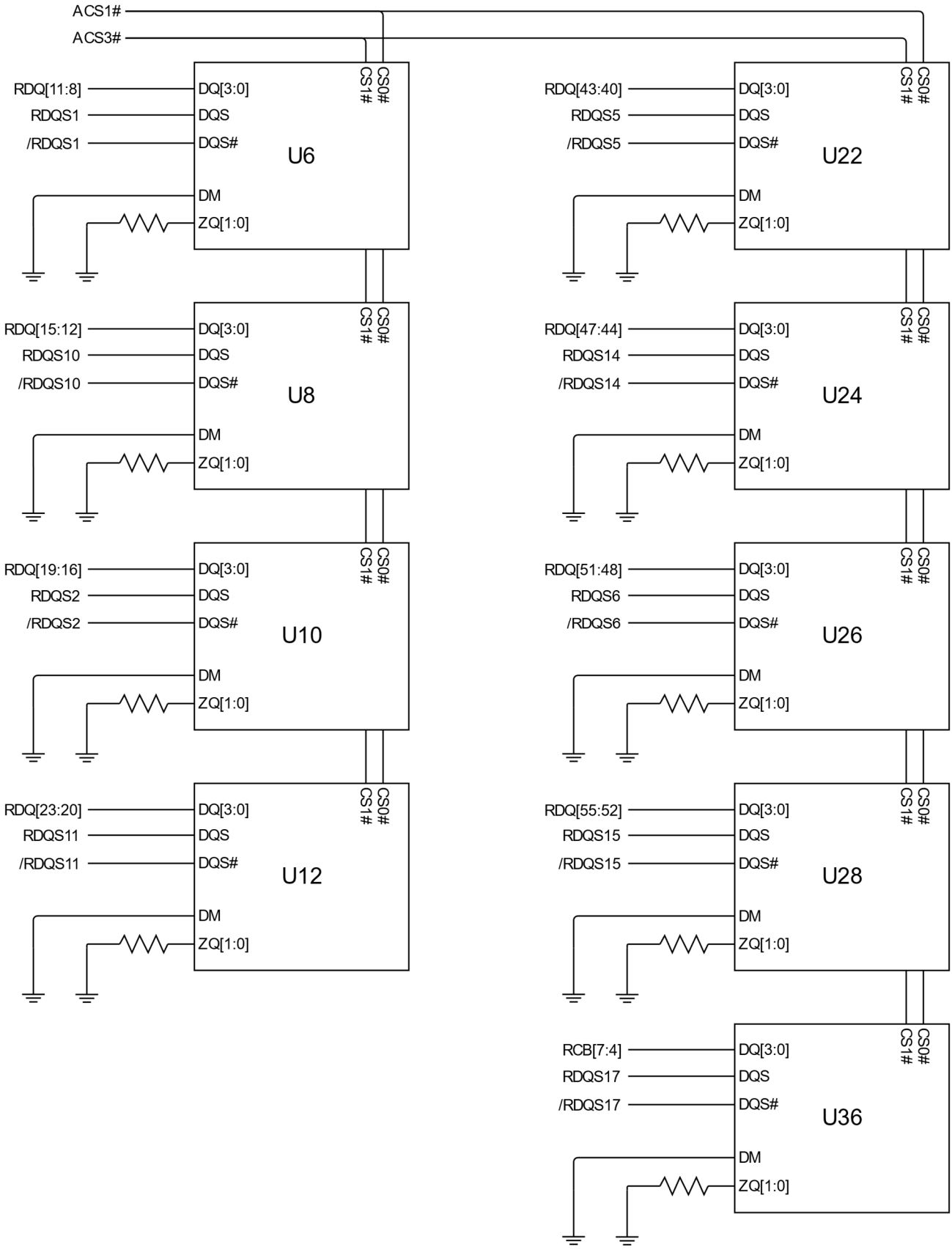


Figure 5 - Functional Block Diagram (Page 4 of 6)

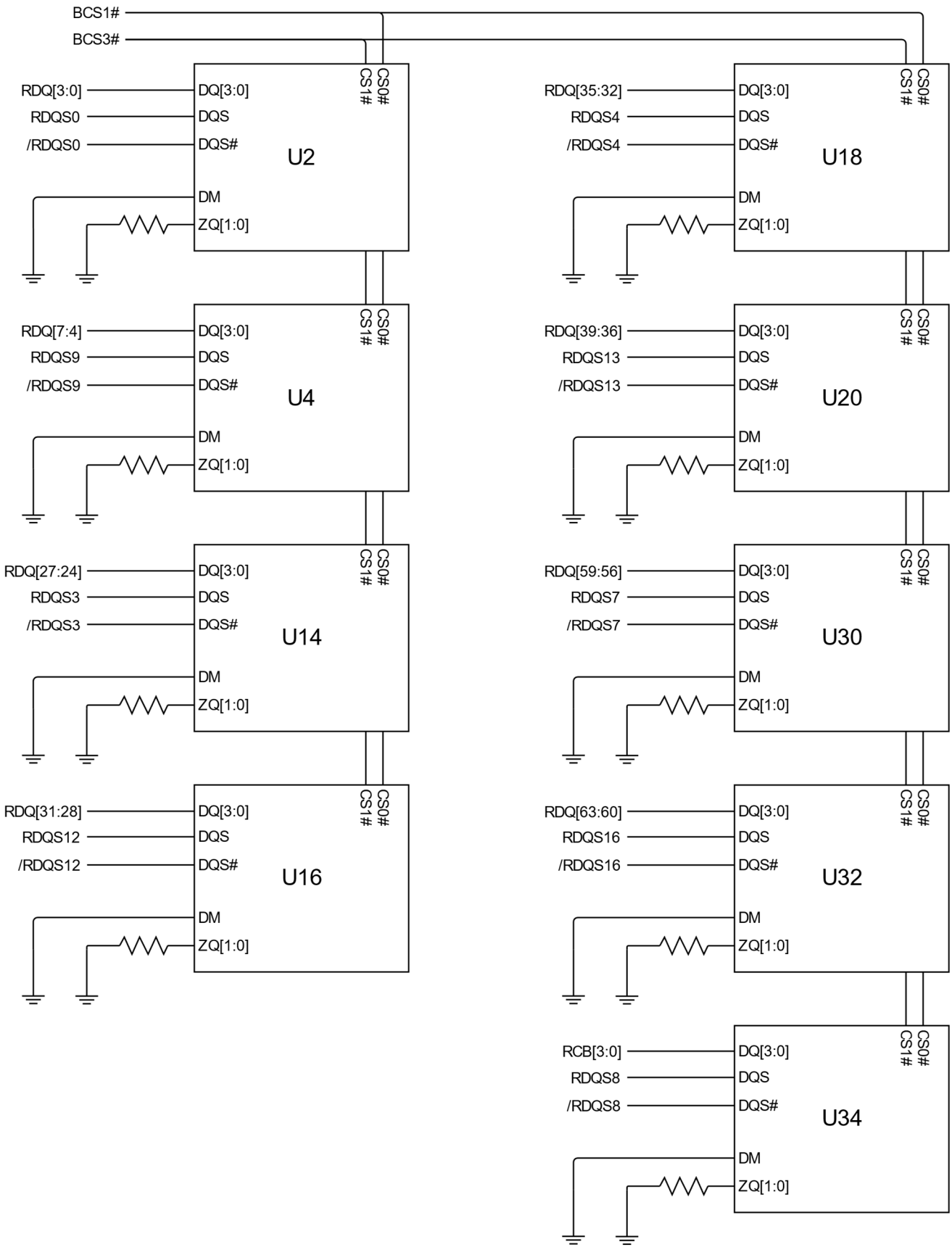


Figure 6 - Functional Block Diagram (Page 5 of 6)

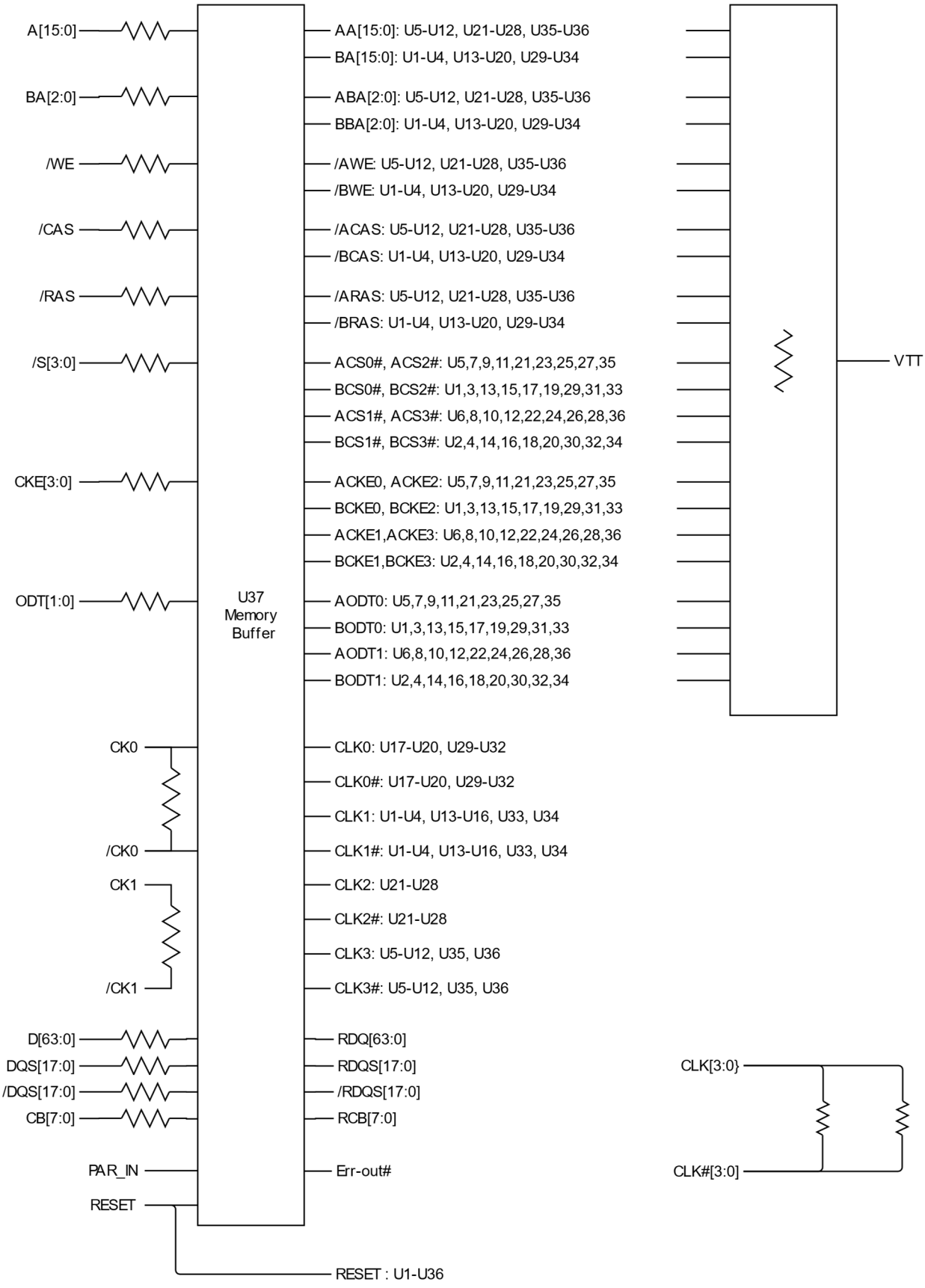
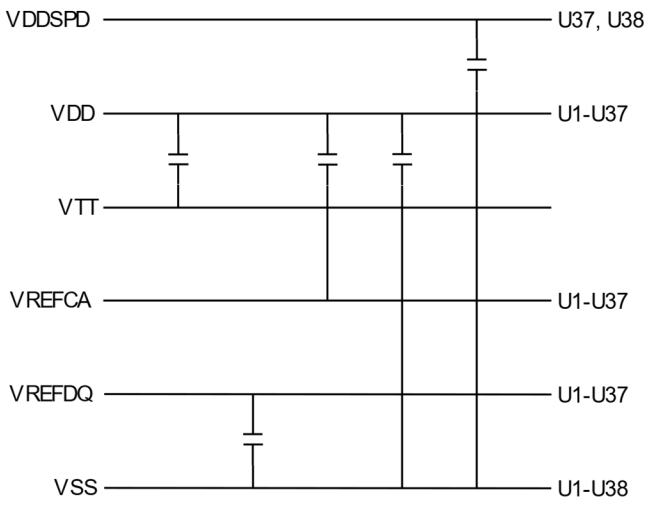
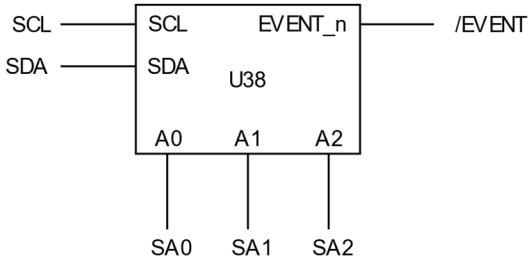


Figure 7 - Functional Block Diagram (Page 6 of 6)





Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD}, pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V_{DDQ}, pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature for Commercial temperature product	T_{case}	0 ~ 95	°C	2,4,5
DRAM Operation temperature for Industrial temperature product	T_{case}	-40 ~ 95	°C	2,4,5

Notes:

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3 V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must not be greater than 0.6 x V_{DDQ}, when V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

4 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.

5 Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V_{DDQ}				V	1,2
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V_{DDQ}				V	1,2,3

Notes:

1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD}. V_{SS} = V_{SSQ}.
2. V_{DD} and V_{DDQ} may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
3. Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
V_{IN} low; DC/commands/address buses (1.35V)	V_{IL}	V_{SS}	-	V_{REF} - 0.090	V	
V_{IN} low; DC/commands/address buses (1.5V)	V_{IL}	V_{SS}	-	V_{REF} - 0.100	V	
V_{IN} high; DC/commands/address buses (1.35V)	V_{IH}	V_{REF} + 0.090	-	V_{DD}	V	
V_{IN} high; DC/commands/address buses (1.5V)	V_{IH}	V_{REF} + 0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	0.50* V_{DDQ}	-	V	4

Notes:

1. $V_{REFCA(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1% × V_{DD} around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of $V_{REFCA(DC)}$.
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. $V_{REFDQ(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1% × V_{DD} around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of $V_{REFDQ(DC)}$.
4. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition		Symbol	Value		Units
			1.35V	1.5V	
Command and Address					
Input high AC voltage: Logic 1 @ 175mV	DDR3-1600, 1333	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	DDR3-1600, 1333	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	DDR3-1600, 1333	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	DDR3-1600, 1333	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	DDR3-1600, 1333	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	DDR3-1600, 1333	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	DDR3-1600, 1333	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	DDR3-1600, 1333	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	DDR3-1600, 1333	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	DDR3-1600, 1333	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	DDR3-1600, 1333	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	DDR3-1600, 1333	$V_{IL(AC175)max}$	-	-175	mV

Parameter / Condition		Symbol	Value		Units
			1.35V	1.5V	
DQ and DM					
Input high AC voltage: Logic 1	DDR3-1600, 1333	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	DDR3-1600, 1333	$V_{IH(AC135)min}$	135	135	mV
Input high DC voltage: Logic 1	DDR3-1600, 1333	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	DDR3-1600, 1333	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	DDR3-1600, 1333	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	DDR3-1600, 1333	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	DDR3-1600, 1333	$V_{IL(AC135)max}$	-135	-135	mV
Input low AC voltage: Logic 0	DDR3-1600, 1333	$V_{IL(AC150)max}$	-	-150	mV

Notes:
1. All voltages are referenced to V_{REF}. V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
2. Input setup timing parameters (t_{IS} and t_{DS}) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (t_{IH} and t_{DH}) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high - slew (1.35V)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high - slew (1.5V)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low - slew (1.35V)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low - slew (1.5V)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	2* ($V_{IH(AC)}$ - V_{REF})	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	2* ($V_{IL(AC)}$ - V_{REF})	mV	3
Single-ended high level for strobes	V_{SEH}	V_{DDQ}/2 + 175	-	mV	2
Single-ended high level for CK, /CK		V_{DD}/2 + 175	-	mV	2
Single-ended low level for strobes	V_{SEL}	-	V_{DDQ}/2 - 175	mV	3
Single-ended low level for CK, /CK		-	V_{DD}/2 - 175	mV	3

Notes:
1. Defines slew rate reference points, relative to input crossing voltages.
2. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
3. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)}$ = V_{TT} - 0.1 * V_{DDQ} and $V_{OH(AC)}$ = V_{TT} + 0.1 * V_{DDQ} (1.35V)	SRQ_{se}	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)}$ = V_{TT} - 0.1 * V_{DDQ} and $V_{OH(AC)}$ = V_{TT} + 0.1 * V_{DDQ} (1.5V)	SRQ_{se}	2.5	5	V/ns	1,2,3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	0.8 * V_{DDQ}		V	1,2
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	0.5 * V_{DDQ}		V	1,2
Single-ended DC low-level output voltage	$V_{OL(DC)}$	0.2 * V_{DDQ}		V	1,2
Single-ended AC high-level output voltage	$V_{OH(AC)}$	V_{TT} + 0.1 * V_{DDQ}		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	V_{TT} - 0.1 * V_{DDQ}		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:
1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
2. V_{TT} = V_{DDQ}/2.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = - 0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.35V)	SRQ_{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = - 0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.5V)	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 * V_{DDQ}		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	-0.2 * V_{DDQ}		V	1
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:
1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
2. V_{REF} = V_{DDQ}/2; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM4G72D3(L)LRQ4AG-D125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	1674	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1818	mA	1, 2
Precharge power-down current; Slow exit	I_{DD2P0}	576	mA	1, 3
Precharge power-down current; Fast exit	I_{DD2P1}	792	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	1152	mA	1, 3
Precharge standby current	I_{DD2N}	1152	mA	1, 3
Precharge standby ODT current	I_{DD2NT}	1224	mA	1, 3
Active power-down current	I_{DD3P}	1224	mA	1, 3
Active standby current	I_{DD3N}	1368	mA	1, 3
Burst read operating current	I_{DD4R}	2394	mA	1, 2
Burst write operating current	I_{DD4W}	2430	mA	1, 2
Refresh current	I_{DD5B}	4950	mA	1, 2
Self refresh temperature current: MAX T_c = 85°C	I_{DD6}	720	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T_c = 95°C	I_{DD6ET}	864	mA	1, 3
All banks interleaved read current	I_{DD7}	3060	mA	1, 2
Reset current	I_{DD8}	720	mA	1, 3

Notes:
1 Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.
2 One module rank in the active I_{DD}, the other rank in I_{DD2N}.
3 All ranks in this I_{DD} conditions.

For part number IMM4G72D3(L)LRQ4AG-D125(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T_C = 0°C to 85°C	t_{CK}(DLL_DIS)	8	-	ns
	T_C => 85°C to 95°C		8	-	
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		t_{CK}(avg)	1.25	1.5	ns
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		t_{CK}(avg)	1.5	1.875	ns
High pulse width average		t_{CH}(avg)	0.47	0.53	t_{CK}(avg)
Low pulse width average		t_{CL}(avg)	0.47	0.53	t_{CK}(avg)
Clock period jitter	DLL locked	t_{JITper}	70	70	ps
	DLL locking	$t_{JIT(per,lck)}$	-60	60	ps
Clock absolute period		t_{CK}(abs)	t_{CK}(avg) Min + t_{JITper} Min	t_{CK}(avg) Max + t_{JITper} Max	ps
Clock absolute high pulse width		t_{CH}(abs)	0.43	-	t_{CK}(avg)
Clock absolute low pulse width		t_{CL}(abs)	0.43	-	t_{CK}(avg)
Cycle-to-cycle jitter	DLL locked	t_{JITcc}	-	140	ps
	DLL locking	$t_{JIT(cc,lck)}$	-	120	ps
Cumulative error across	2 cycles	$t_{ERR(2per)}$	-103	103	ps
	3 cycles	$t_{ERR(3per)}$	-122	122	ps
	4 cycles	$t_{ERR(4per)}$	-136	136	ps
	5 cycles	$t_{ERR(5per)}$	-147	147	ps
	6 cycles	$t_{ERR(6per)}$	-155	155	ps
	7 cycles	$t_{ERR(7per)}$	-163	163	ps
	8 cycles	$t_{ERR(8per)}$	-169	169	ps
	9 cycles	$t_{ERR(9per)}$	-175	175	ps
	10 cycles	$t_{ERR(10per)}$	-180	180	ps
	11 cycles	$t_{ERR(11per)}$	-174	174	ps
	12 cycles	$t_{ERR(12per)}$	-188	188	ps
	n = 13,...49, 50 cycles	$t_{ERR(nper)}$	(1+0.68ln[n]) * t_{JITper} Min	(1+0.68ln[n]) * t_{JITper} Max	ps
DQ Input Timing					
Data setup time to DQS, /DQS (1.35V)	Base (specification)	$t_{DS(AC130)}$	25	-	ps
Data setup time to DQS, /DQS (1.5V)	Base (specification)	$t_{DS(AC135)}$	10	-	ps
Data hold time from DQS, /DQS (1.35V)	Base (specification)	$t_{DH(DC90)}$	55	-	ps
Data hold time from DQS, /DQS (1.5V)	Base (specification)	$t_{DH(DC100)}$	45	-	ps
Minimum data pulse width		t_{DIPW}	360	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		t_{DQSQ}	-	85	ps
DQ output hold time from DQS, /DQS		t_{QH}	0.38	-	t_{CK}(avg)
DQ Low-Z time from CK, /CK		$t_{LZ(DQ)}$	-390	195	ps
DQ High-Z time from CK, /CK		$t_{HZ(DQ)}$	-	195	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		t_{DQSS}	-0.27	0.27	t_{CK}(avg)
DQS, /DQS differential input low pulse width		t_{DQSL}	0.45	0.55	t_{CK}(avg)
DQS, /DQS falling setup to CK, /CK rising		t_{DSS}	0.18	-	t_{CK}(avg))
DQS, /DQS falling hold from CK, /CK rising		t_{DSH}	0.18	-	t_{CK}(avg)
DQS, /DQS differential input high pulse width		t_{DQSH}	0.45	0.55	t_{CK}(avg)
DQS, /DQS differential WRITE preamble		t_{WPRE}	0.9	-	t_{CK}(avg)
DQS, /DQS differential WRITE postamble		t_{WPST}	0.3	-	t_{CK}(avg)

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Parameter / Condition		Symbol	Min	Max	Units
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		t_{DQSCK}	-225	225	ps
DQS, /DQS differential output high time		t_{QSH}	0.45	-	t_{CK}(avg)
DQS, /DQS differential output low time		t_{QSL}	0.45	-	t_{CK}(avg)
DQS, /DQS Low-Z time (RL-1)		$t_{LZ(DQS)}$	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		$t_{HZ(DQS)}$	-	225	ps
DQS, /DQS differential READ preamble		t_{RPRE}	0.9		t_{CK}(avg)
DQS, /DQS differential READ postamble		t_{RPST}	0.3		t_{CK}(avg)
Command and Address Timing					
DLL locking time		t_{DLLK}	512	-	nCK
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	t_{IS}(AC160)	60	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	t_{IS}(AC135)	185	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	t_{IS}(AC175)	170	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	t_{IS}(AC150)	120	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V)	Base (specification)	t_{IH}(DC90)	130	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V)	Base (specification)	t_{IH}(DC100)	120	-	ps
Minimum CTRL, CMD, ADDR pulse width		t_{IPW}	560	-	ps
ACTIVATE to internal READ or WRITE delay		t_{RCD}	13.125	-	ns
PRECHARGE command period		t_{RP}	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		t_{RAS}	35	9 * t_{REFI}	ns
ACTIVATE-to-ACTIVATE command period		t_{RC}	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period (1KB page size)		t_{RRD}	greater of 4nCK or 6ns	-	-
ACTIVATE-to-ACTIVATE minimum period (2KB page size)		t_{RRD}	greater of 4nCK or 7.5ns	-	-
Four ACTIVATE windows (1KB page size)		t_{FAW}	30	-	ns
Four ACTIVATE windows (2KB page size)		t_{FAW}	40	-	ns
Write recovery time		t_{WR}	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		t_{WTR}	greater of 4nCK or 7.5ns	-	-
READ-to-PRECHARGE time		t_{RTP}	greater of 4nCK or 7.5ns	-	-
/CAS-to-/CAS command delay		t_{CCD}	4	-	t_{CK}
Auto precharge write recovery + precharge time		t_{DAL}	WR + t_{RP}/t_{CK}(avg)	-	t_{CK}
MODE REGISTER SET command cycle time		t_{MRD}	4	-	nCK
MODE REGISTER SET command update delay		t_{MOD}	greater of 12nCK or 15ns	-	-
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		t_{MPRR}	1	-	nCK
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	t_{ZQinit}	greater of 512nCK or 640ns	-	-
	Normal operation	t_{ZQoper}	greater of 256nCK or 320ns	-	-
ZQCS command: Short calibration time		t_{ZQCS}	greater of 64nCK or 80ns	-	-
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		t_{XPR}	greater of 5nCK or t_{RFC}(min)+10ns	-	-
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		t_{RFC}	260	-	ns

For part number IMM4G72D3(L)LRQ4AG-D125(I)

Parameter / Condition		Symbol	Min	Max	Units
Maximum refresh period	T_c<=85°C	-	64 (1X)		ms
	T_c>85°C		32 (2X)		
Maximum average periodic refresh	T_c<=85°C	t_{REFI}	7.8 (64ms/8192)		us
	T_c>85°C		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		t_{XS}	greater of 5 nCK or t_{RFC} Min+10ns	-	-
Exit self refresh to commands requiring a locked DLL		t_{XSDLL}	t_{DLLK} Min	-	nCK
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		t_{CKESR}	t_{CKE} Min + 1nCK	-	-
Valid clocks after self refresh entry or power down entry		t_{CKSRE}	greater of 5nCK or 10ns	-	-
Valid clocks before self refresh exit, power-down exit, or reset exit		t_{CKSRX}	greater of 5nCK or 10ns	-	-
Power-Down Timing					
CKE MIN pulse width		t_{CKE}	greater of 3nCK or 5ns	-	-
Command pass disable delay		t_{CPDED}	1	-	nCK
Power-down entry to power exit timing		t_{PD}	t_{CKE} Min	9 * t_{REFI}	-
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		$t_{ACTPDEN}$	1	-	nCK
PRECHARGE/PRECHARGE ALL command to power-down entry		t_{PRPDEN}	1	-	nCK
REFRESH command to power-down entry		$t_{REFPDEN}$	1	-	nCK
MRS command to power-down entry		$t_{MRSPDEN}$	t_{MOD} Min	-	nCK
READ/READ with auto precharge command to power-down entry		t_{RDPDEN}	RL + 4 + 1	-	nCK
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	t_{WRPDEN}	WL + 4 + t_{WR}/t_{CK}(avg)	-	nCK
	BC4MRS	t_{WRPDEN}	WL + 2 + t_{WR}/t_{CK}(avg)	-	nCK
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t_{WRAPDEN}$	WL + 4 + t_{WR} + 1	-	nCK
	BC4MRS	$t_{WRAPDEN}$	WL + 2 + t_{WR} + 1	-	nCK
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		t_{XP}	greater of 3nCK or 6ns	-	-
Precharge power-down with DLL off to commands requiring a locked DLL		t_{XPDLL}	greater of 10nCK or 24ns	-	-
ODT Timing					
RTT turn-on from ODTL on reference		t_{AON}	-225	225	ps
RTT turn-off from ODTL off reference		t_{AOF}	0.3	0.7	t_{CK}(avg)
Asynchronous RTT turn-on delay (power-down with DLL off)		t_{AONPD}	2	8.5	ns
Asynchronous RTT turn-off delay (power-down with DLL off)		t_{AOFPD}	2	8.5	ns
ODT HIGH time with WRITE command and BL8		ODTH8	6	-	nCK
ODT HIGH time without WRITE command or WRITE command and BC4		ODTH4	4	-	nCK
Dynamic ODT Timing					
RTT dynamic change skew		t_{ADC}	0.3	0.7	t_{CK}(avg)
Write Leveling Timing					
First DQS, /DQS rising edge		t_{WLMRD}	40	-	nCK
DQS, /DQS delay		$t_{WLDQSEN}$	25	-	nCK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing		t_{WLS}	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing		t_{WLH}	165	-	ps
Write leveling output delay		t_{WLO}	0	7.5	ns
Write leveling output error		t_{WLOE}	0	2	ns

For part number IMM4G72D3(L)LRQ4AG-D125(I)

Table 19 - SPD Information

Byte NO.	Description	Note		Hex	
		1.35V	1.5V	1.35V	1.5V
0	Number of SPD Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116		92	
1	SPD Revision	Revision 1.2		12	
2	Key Byte / DRAM Device Type	DDR3 SDRAM		0B	
3	Key Byte / Module Type	Load Reduced DIMM		0B	
4	SDRAM Density and Banks	4Gbits, 8banks		04	
5	SDRAM Addressing	Row 16 / Col 11		22	
6	Module Nominal Voltage, V_{DD}	1.35V/1.5V	1.5V	02	00
7	Module Organization	4 Rank, 4bits		18	
8	Module Memory Bus Width	ECC, 72bits		0B	
9	Fine Timebase (FTB) Dividend / Divisor	2.5ps		52	
10	Medium Timebase (MTB) Dividend	1ns		01	
11	Medium Timebase (MTB) Divisor	8		08	
12	SDRAM Minimum Cycle Time (t_{CK}min)	1.25ns		0A	
13	Reserved	-		00	
14	CAS Latencies Supported, Least Significant Byte	5,6,7,8,9,10,11		FE	
15	CAS Latencies Supported, Most Significant Byte	-		00	
16	Minimum CAS Latency Time (t_{AA}min)	13.125ns		69	
17	Minimum Write Recovery Time (t_{WR}min)	15ns		78	
18	Minimum RAS# to CAS# Delay Time (t_{RCD}min)	13.125ns		69	
19	Minimum Row Active to Row Active Delay Time (t_{RRD}min)	7.5ns		3C	
20	Minimum Row Precharge Time (t_{RP}min)	13.125ns		69	
21	Upper Nibbles for t_{RAS} and t_{RC}	-		11	
22	Minimum Active to Precharge Time (t_{RAS}min), Least Significant Byte	35ns		18	
23	Minimum Active to Active/Refresh Time (t_{RC}min), Least Significant Byte	48.125ns		81	
24	Minimum Refresh Recovery Time (t_{RFC}min), Least Significant Byte	260ns		20	
25	Minimum Refresh Recovery Time (t_{RFC}min), Most Significant Byte	-		08	
26	Minimum Internal Write to Read Command Delay Time (t_{WTR}min)	7.5ns		3C	
27	Minimum Internal Read to Precharge Command Delay Time (t_{RTP}min)	7.5ns		3C	
28	Upper Nibble for t_{FAW}	-		01	
29	Minimum Four Activate Window Delay Time (t_{FAW}min)	40ns		40	
30	SDRAM Optional Features	DLL off, RZQ/7, RZQ/6		83	
31	SDRAM Thermal and Refresh Options	ASR, 0°C-95°C, req. 2x Refresh		05	
32	Module Thermal Sensor	Thermal Sensor incorporated		80	
33	SDRAM Device Type	Dual Die Package		A1	
34	Fine Offset for SDRAM Minimum Cycle Time (t_{CK}min)	-0ns		00	
35	Fine Offset for Minimum CAS Latency Time (t_{AA}min)	-0ns		00	
36	Fine Offset for Minimum RAS# to CAS# Delay Time (t_{RCD}min)	-0ns		00	
37	Fine offset for minimum Row Precharge Delay Time (t_{RP}min)	-0ns		00	

Byte NO.	Description	Note	Hex
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (t_{RC}min)	-0ns	00
39-40	Reserved, General Section	-	00
41	SDRAM Maximum Activate Count (MAC) Value	8192*t_{REFI}, Untested MAC	00
42-59	Reserved. General Section	-	00
60	Module Nominal Height	30< Height <=31mm	10
61	Module Maximum Thickness	2< tF <=3 mm: 1< tB <=2 mm	12
62	Reference Raw Card Used	Raw Card C0	02
63	Module Attributes	2 Row of DRAM, Odd ranks are mirrored	09
64	memory Buffer Revision Number	Undefined	FF
65	Register vendor ID code, Least Significant Byte	-	00
66	Register vendor ID code, Most Significant Byte	-	00
67	F0RC3 / F0RC2 - Timing Control & Drive Strength, CA & CS	Clock: Moderate Drive, Control: Strong drive Not swapped, Standard	60
68	F0RC5 / F0RC4 - Drive Strength, ODT & CKE and Y	Moderate drive	55
69	F1RC11 / F1RC8 - Extended Delay for Y, CS and ODT & CKE	No delay	00
70	F1RC13 / F1RC12 - Additive Delay for CS and CA	Disabled	00
71	F1RC15 / F1RC14 - Additive Delay for ODT & CKE	Disabled	00
72	F3RC9 / F3RC8 - MDQ Termination and Drive Strength for 800 & 1066	RZQ/6, RZQ/2	02
73	F[3,4]RC11 / F[3,4]RC10 - Rank 0 & 1 RD & WR QxODT Control for 800 & 1066	F4RC11(QxODT1), F3RC11(QxODT0)	90
74	F[5,6]RC11 / F[5,6]RC10 - Rank 2 & 3 RD & WR QxODT Control for 800 & 1066	Not asserted	00
75	F[7,8]RC11 / F[7,8]RC10 - Rank 4 & 5 RD & WR QxODT Control for 800 & 1066	Not asserted	00
76	F[9,10]RC11 / F[9,10]RC10 - Rank 6 & 7 RD & WR QxODT Control for 800 & 1066	Not asserted	00
77	MR1,2 Registers for 800 & 1066	RZQ/2, Rtt_Nom disabled, RZQ/7	81
78	F3RC9 / F3RC8 - MDQ Termination and Drive Strength for 1333 & 1600	RZQ/7, RZQ/4	11
79	F[3,4]RC11 / F[3,4]RC10 - Rank 0 & 1 RD & WR QxODT Control for 1333 & 1600	F[3,4]RC11	F0
80	F[5,6]RC11 / F[5,6]RC10 - Rank 2 & 3 RD & WR QxODT Control for 1333 & 1600	F5RC11(QxODT1), F6RC11(QxODT0)	60
81	F[7,8]RC11 / F[7,8]RC10 - Rank 4 & 5 RD & WR QxODT Control for 1333 & 1600	Not asserted	00
82	F[9,10]RC11 / F[9,10]RC10 - Rank 6 & 7 RD & WR QxODT Control for 1333 & 1600	Not asserted	00
83	MR1,2 Registers for 1333 & 1600	RZQ/2, RZQ/4, RZQ/7	85
84	F3RC9 / F3RC8 - MDQ Termination and Drive Strength for 1866 & 2133	RZQ/9, RZQ/4	31
85	F[3,4]RC11 / F[3,4]RC10 - Rank 0 & 1 RD & WR QxODT Control for 1866 & 2133	F[3,4]RC11	F0
86	F[5,6]RC11 / F[5,6]RC10 - Rank 2 & 3 RD & WR QxODT Control for 1866 & 2133	F6RC11(QxODT0), F5RC11(QxODT1)	60
87	F[7,8]RC11 / F[7,8]RC10 - Rank 4 & 5 RD & WR QxODT Control for 1866 & 2133	Not asserted	00
88	F[9,10]RC11 / F[9,10]RC10 - Rank 6 & 7 RD & WR QxODT Control for 1866 & 2133	Not asserted	00

Byte NO.	Description	Note	Hex
89	MR1,2 Registers for 1866 & 2133	RZQ/2, RZQ/8, RZQ/7	95
90	Minimum Module Delay Time for 1.5 V	7.5 ns	3C
91	Maximum Module Delay Time for 1.5 V	9.5 ns	4C
92	Minimum Module Delay Time for 1.35 V	7.5 ns	3C
93	Maximum Module Delay Time for 1.35 V	9.5 ns	4C
94	Minimum Module Delay Time for 1.25 V	7.5 ns	3C
95	Maximum Module Delay Time for 1.25 V	9.5 ns	4C
96-101	Reserved	-	00
102-116	Memory Buffer Personality Bytes	Undefined	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	I'M	04 9E
119	Module ID: Module Manufacturing Location	-	00
120-121	Module ID: Module Manufacturing Date	Manufacturer's data	-
122-125	Module ID: Module Serial Number	Manufacturer's data	-
126-127	Cyclical Redundancy Code	-	E4 CB | 4F 4C
128-145	Module Part Number	Manufacturer's data	-
146-147	Module Revision Code	-	00
148-149	DRAM Manufacturer's JEDEC ID Code	-	00
150-175	Manufacturer's Specific Data	Manufacturer's data	-
176-255	Open For Customer Use	-	00

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	May, 2021
2.0	Revise SPD Description in Table 19	Jun, 2021

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