Datasheet | Rev. 1.0 | 2021

IMM2G72D3MRQ8AG (Die Revision D)
16GByte (2G x 72 Bit)

16GB DDR3 Registered Mini-DIMM
RoHS Compliant Product

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures.

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Features

- 244-Pin Registered Mini Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC3-8500: 5, 6, 7, 8
- Programmable CAS Write Latency (CWL):
  - PC3-8500: 5, 6
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) with EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.18inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G72D3xMRQ8AG-Dzzzy	16GB	2Gx72	4	16GB DDR3 Registered Mini-DIMM

Notes:
x: Operating Voltage
y: Operating Temperature
zzz: Speed Grade

Table 2 - Operating Voltage

Part Number	Operating Voltage
Blank	V_{DD}, V_{DDQ} = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade

Part Number	Temperature Grade	Tcase
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < T_{case} <= 95 °C.

Table 4 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
187E	PC3-8500 (DDR3-1066)	533MHz (1.875ns@CL=7)

Table 5 - Memory Chip Information

Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM2G72D3MRQ8AG-Dzzzy	I'M	IM8G08D3FDDG	1.35V/1.5V	512Mx8x2 DDP	Lead Free

Part Number Decoder

IM M 2G72 D3 ( ) MR Q 8 A G - D 187E (I)

I'M Module

DRAM Brand
M = I'M

Module Configuration
2G72 = 2Gx72 (16GB)

Memory Type
D3 = DDR3

DDR3L option
Blank = 1.5V

Module Form-Factor
MR = Registered Mini DIMM (Mini-RDIMM)

Number of Ranks
Q = Quad Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A

RoHS compliance
G = Green / RoHS

IC Revision
D = Revision D

Speed Grade
187E = DDR3-1066 CL7

Temperature Grade
Blank = Commercial Temperature
(0°C to 95°C T_{case})
I = Industrial Temperature
(-40°C to 95°C T_{case})

Table 6 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (512Mx8x2 DDP)
Column address	1K A[9:0]
Module rank address	4 /S[3:0]
Number of devices	18

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{TT}	123	V_{TT}	62	A2	184	A1
2	V_{REFDQ}	124	V_{SS}	63	V_{DD}	185	V_{DD}
3	V_{SS}	125	D4	64	CK1	186	CK0
4	D0	126	D5	65	/CK1	187	/CK0
5	D1	127	V_{SS}	66	V_{DD}	188	V_{DD}
6	V_{SS}	128	TDQS9, DM0	67	V_{REFCA}	189	V_{DD}
7	/DQS0	129	/TDQS9	68	V_{DD}	190	/EVENT
8	DQS0	130	V_{SS}	69	PAR_IN	191	A0
9	V_{SS}	131	D6	70	V_{DD}	192	V_{DD}
10	D2	132	D7	71	A10, AP	193	BA1
11	D3	133	V_{SS}	72	BA0	194	V_{DD}
12	V_{SS}	134	D12	73	V_{DD}	195	/RAS
13	D8	135	D13	74	/WE	196	/S0
14	D9	136	V_{SS}	75	/CAS	197	V_{DD}
15	V_{SS}	137	TDQS10, DM1	76	V_{DD}	198	ODT0
16	/DQS1	138	/TDQS10	77	/S1	199	A13
17	DQS1	139	V_{SS}	78	ODT1	200	V_{DD}
18	V_{SS}	140	D14	79	V_{DD}	201	/S3
19	D10	141	D15	80	/S2	202	NC
20	D11	142	V_{SS}	81	NC	203	V_{SS}
21	V_{SS}	143	D20	82	V_{SS}	204	D36
22	D16	144	D21	83	D32	205	D37
23	D17	145	V_{SS}	84	D33	206	V_{SS}
24	V_{SS}	146	TDQS11, DM2	85	V_{SS}	207	TDQS13, DM4
25	/DQS2	147	/TDQS11	86	/DQS4	208	/TDQS13
26	DQS2	148	V_{SS}	87	DQS4	209	V_{SS}
27	V_{SS}	149	D22	88	V_{SS}	210	D38
28	D18	150	D23	89	D34	211	D39
29	D19	151	V_{SS}	90	D35	212	V_{SS}
30	V_{SS}	152	D28	91	V_{SS}	213	D44
31	D24	153	D29	92	D40	214	D45
32	D25	154	V_{SS}	93	D41	215	V_{SS}
33	V_{SS}	155	TDQS12, DM3	94	V_{SS}	216	TDQS14, DM5
34	/DQS3	156	/TDQS12	95	/DQS5	217	/TDQS14
35	DQS3	157	V_{SS}	96	DQS5	218	V_{SS}
36	V_{SS}	158	D30	97	V_{SS}	219	D46
37	D26	159	D31	98	D42	220	D47
38	D27	160	V_{SS}	99	D43	221	V_{SS}
39	V_{SS}	161	CB4	100	V_{SS}	222	D52
40	CB0	162	CB5	101	D48	223	D53
41	CB1	163	V_{SS}	102	D49	224	V_{SS}
42	V_{SS}	164	TDQS17, DM8	103	V_{SS}	225	TDQS15, DM6
43	/DQS8	165	/TDQS17	104	/DQS6	226	/TDQS15
44	DQS8	166	V_{SS}	105	DQS6	227	V_{SS}
45	V_{SS}	167	CB6	106	V_{SS}	228	D54
46	CB2	168	CB7	107	D50	229	D55
47	CB3	169	V_{SS}	108	D51	230	V_{SS}
48	V_{SS}	170	NC	109	V_{SS}	231	D60
49	NC	171	NC	110	D56	232	D61
50	/RESET	172	CKE1	111	D57	233	V_{SS}
51	CKE0	173	V_{DD}	112	V_{SS}	234	TDQS16, DM7
52	V_{DD}	174	A15	113	/DQS7	235	/TDQS16
53	BA2	175	A14	114	DQS7	236	V_{SS}
54	/ERR_OUT	176	V_{DD}	115	V_{SS}	237	D62
55	V_{DD}	177	A12, /BC	116	D58	238	D63
56	A11	178	A9	117	D59	239	V_{SS}
57	A7	179	V_{DD}	118	V_{SS}	240	V_{DDSPD}
58	V_{DD}	180	A8	119	SA0	241	SA1
59	A5	181	A6	120	SCL	242	SDA
60	A4	182	V_{DD}	121	SA2	243	V_{SS}
61	V_{DD}	183	A3	122	V_{TT}	244	V_{TT}

Table 8 - Pin Description			
Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM core power supply	V_{REFDQ}	SDRAM I/O reference supply
V_{REFCA}	SDRAM command/address reference supply	V_{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S3	DIMM rank select lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS8	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS8	SDRAM data strobes (negative line of differential pair)
TDQS9-TDQS17	Termination data strobes (positive line of differential pair)	/TDQS9-/TDQS17	Termination data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	CB0-CB7	Data check bits input/output
DM0-DM8	Data masks	SDA	EEPROM data line
SCL	EEPROM clock	V_{DDSPD}	EEPROM positive power supply
SA0-SA2	EEPROM address input	/EVENT	Temperature event
PAR_IN	Parity input	/RESET	Register and SDRAM control pin
/ERR_OUT	Parity error output	V_{TT}	Termination voltage
NC	Spare pins (no connect)	-	-

Module Dimension

Figure 1 - 244 Pin DDR3 SDRAM Registered Mini-DIMM

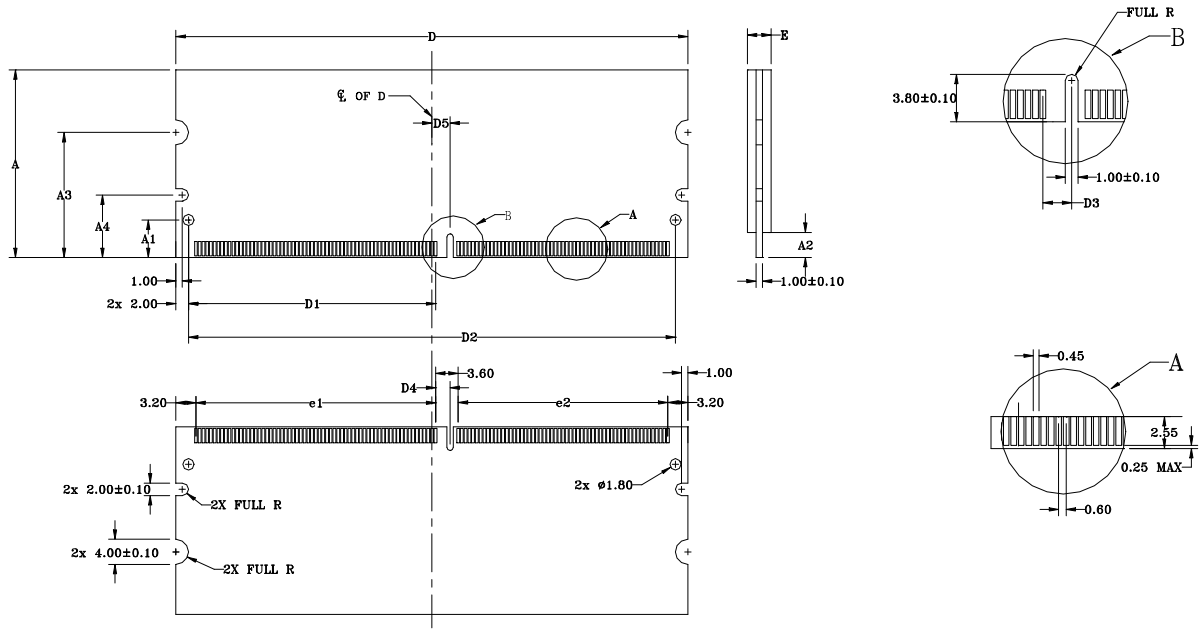


Table 9 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		6.00 Basic	
A2	4.00		
A3		20.00 Basic	
A4		10.00 Basic	
D	81.85	82.00	82.15
D1		39.60 Basic	
D2		78.00 Basic	
D3		2.30 Basic	
D4		2.30 Basic	
D5		2.90 Basic	
e1		38.40 Basic	
e2		33.60 Basic	
E			3.80

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 - Functional Block Diagram (Page 1 of 4)

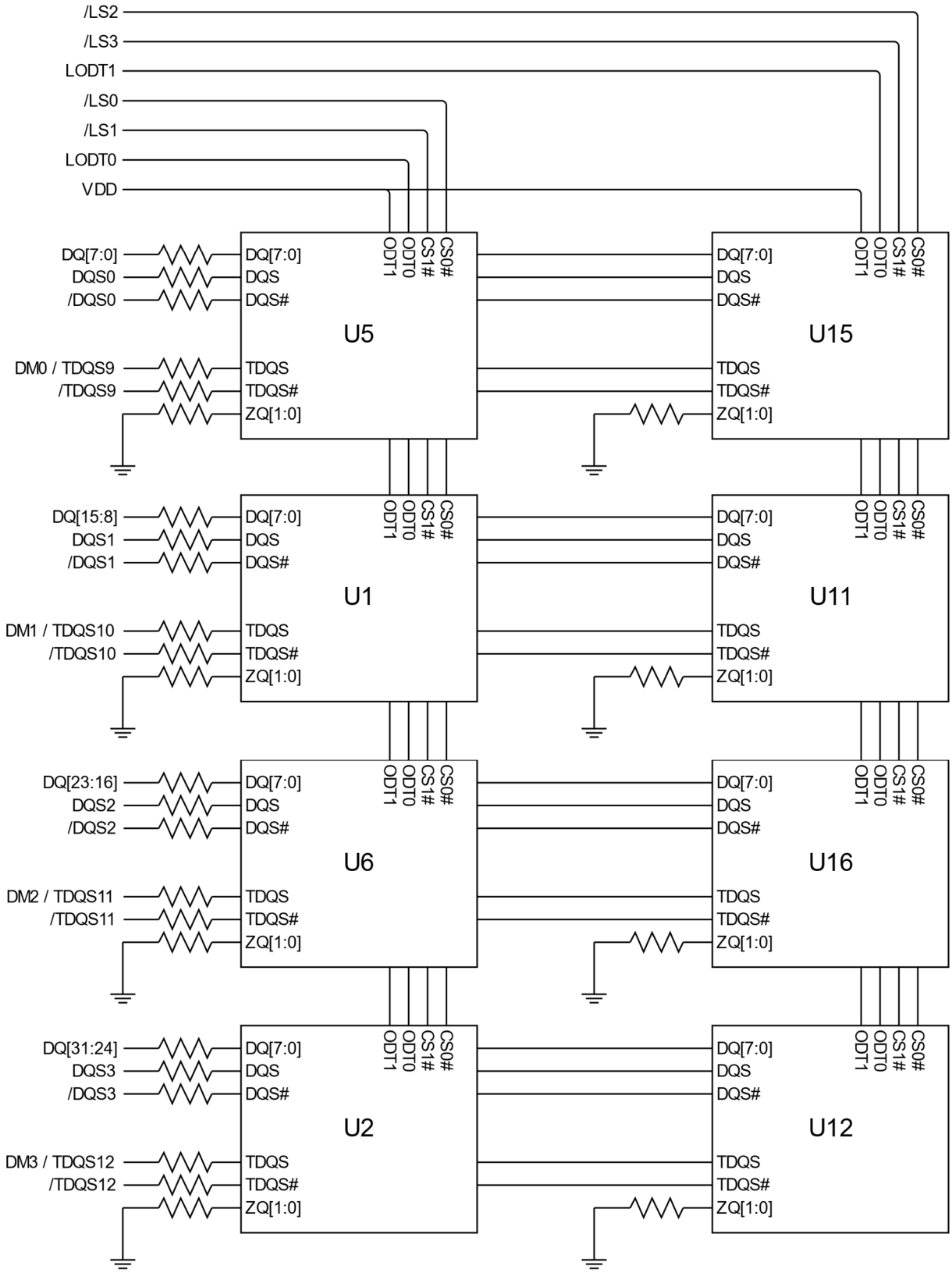


Figure 3 - Functional Block Diagram (Page 2 of 4)

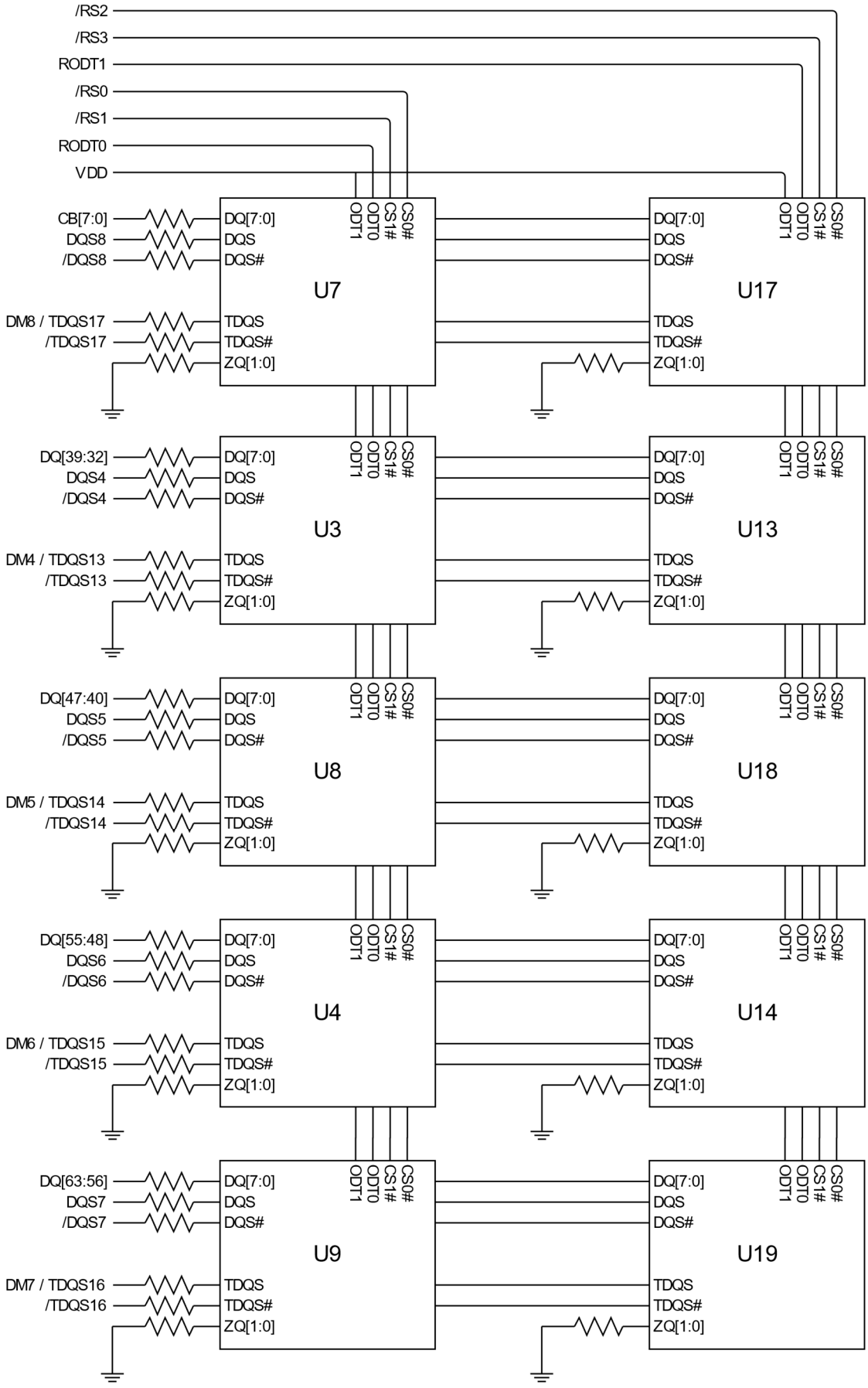


Figure 4 - Functional Block Diagram (Page 3 of 4)

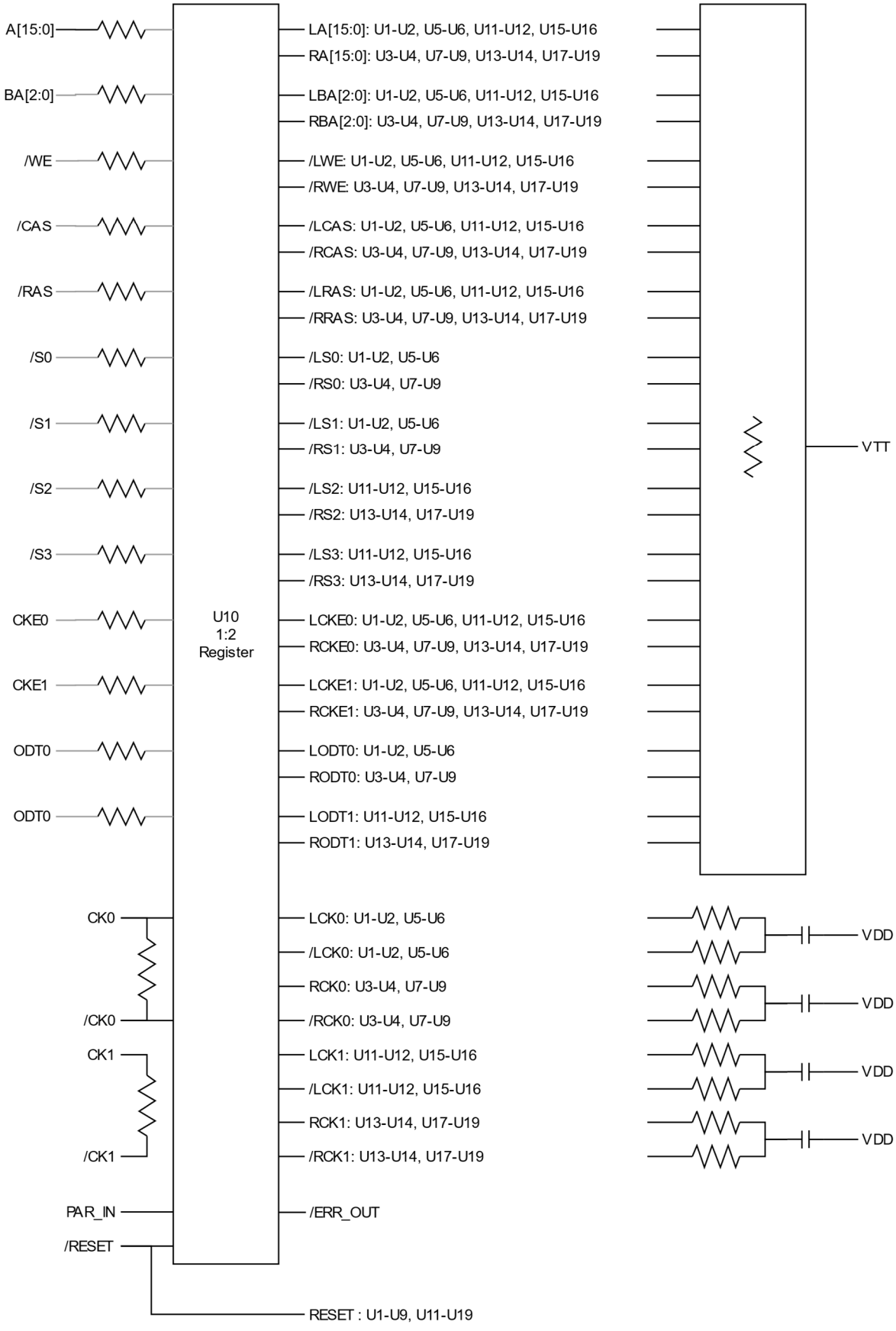
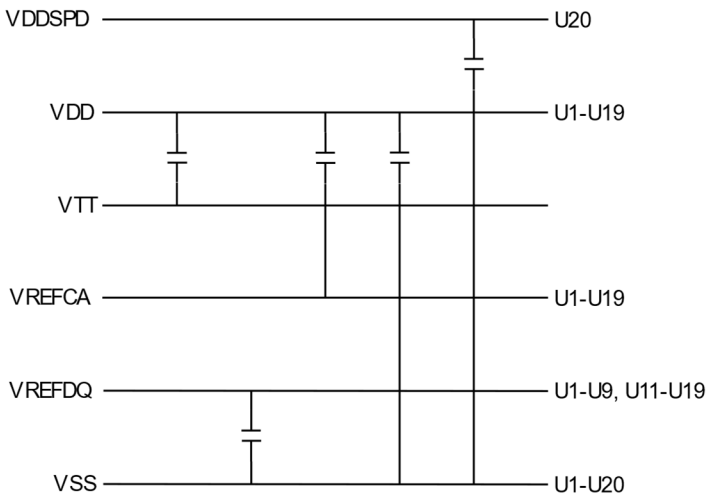
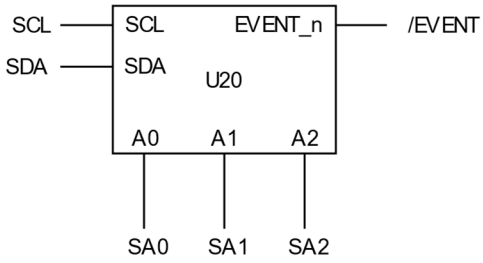


Figure 5 - Functional Block Diagram (Page 4 of 4)





Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on V_{DD}, pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V_{DDQ}, pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 150	°C	1,2
DRAM Operation temperature for Commercial temperature product	T_{case}	0 ~ 95	°C	2,4,6
DRAM Operation temperature for Industrial temperature product	T_{case}	-40 ~ 95	°C	2,5,6

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must not be greater than 0.6 x V_{DDQ}, when V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.
4. The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.
5. The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.
6. Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval t_{REFI} to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1,2
I/O supply voltage	V_{DDQ}				V	1,2

Notes:
1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD}. V_{SS} = V_{SSQ}.
2. V_{DD} and V_{DDQ} may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
V_{IN} low; DC/commands/address buses	V_{IL}	V_{SS}	-	-0.100	V	
V_{IN} high; DC/commands/address buses	V_{IH}	0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	0.50* V_{DDQ}	-	V	4

Notes:

1. $V_{REFCA(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1% × V_{DD} around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of $V_{REFCA(DC)}$.
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. $V_{REFDQ(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1% × V_{DD} around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of $V_{REFDQ(DC)}$.
4. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition		Symbol	Value	Units
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	DDR3-1066	$V_{IH(AC175)min}$	175	mV
Input high AC voltage: Logic 1 @ 150mV	DDR3-1066	$V_{IH(AC150)min}$	150	mV
Input high DC voltage: Logic 1 @ 100mV	DDR3-1066	$V_{IH(DC100)min}$	100	mV
Input low DC voltage: Logic 0 @ -100mV	DDR3-1066	$V_{IL(DC100)max}$	-100	mV
Input low AC voltage: Logic 0 @ -150mV	DDR3-1066	$V_{IL(AC150)max}$	-150	mV
Input low AC voltage: Logic 0 @ -175mV	DDR3-1066	$V_{IL(AC175)max}$	-175	mV

Parameter / Condition		Symbol	Value	Units
DQ and DM				
Input high AC voltage: Logic 1	DDR3-1066	$V_{IH(AC175)min}$	175	mV
Input high AC voltage: Logic 1	DDR3-1066	$V_{IH(AC150)min}$	150	mV
Input high AC voltage: Logic 1	DDR3-1066	$V_{IH(AC135)min}$	135	mV
Input high DC voltage: Logic 1	DDR3-1066	$V_{IH(DC100)min}$	100	mV
Input low DC voltage: Logic 0	DDR3-1066	$V_{IL(DC100)max}$	-100	mV
Input low AC voltage: Logic 0	DDR3-1066	$V_{IL(AC135)max}$	-135	mV
Input low AC voltage: Logic 0	DDR3-1066	$V_{IL(AC150)max}$	-150	mV
Input low AC voltage: Logic 0	DDR3-1066	$V_{IL(AC175)max}$	-175	mV

Notes:
1. All voltages are referenced to V_{REF}. V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
2. Input setup timing parameters (t_{IS} and t_{DS}) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (t_{IH} and t_{DH}) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high AC	$V_{IH,diff(AC)}$	2* ($V_{IH(AC)}$ - V_{REF})	-	mV	2
Differential input voltage logic low AC	$V_{IL,diff(AC)}$	-	2* ($V_{IL(AC)}$ - V_{REF})	mV	3
Single-ended high level for strobes	V_{SEH}	V_{DDQ}/2 + 175	-	mV	
Single-ended high level for CK, /CK		V_{DD}/2 + 175	-	mV	
Single-ended low level for strobes	V_{SEL}	-	V_{DDQ}/2 - 175	mV	
Single-ended low level for CK, /CK		-	V_{DD}/2 - 175	mV	

Notes:
1. Defines slew rate reference points, relative to input crossing voltages.
2. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
3. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{TT}$ - 0.1 * V_{DDQ} and $V_{OH(AC)} = V_{TT}$ + 0.1 * V_{DDQ}	SRQ_{se}	2.5	5	V/ns	1,2,3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	0.8 * V_{DDQ}		V	1,2
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	0.5 * V_{DDQ}		V	1,2
Single-ended DC low-level output voltage	$V_{OL(DC)}$	0.2 * V_{DDQ}		V	1,2
Single-ended AC high-level output voltage	$V_{OH(AC)}$	V_{TT} + 0.1 * V_{DDQ}		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	V_{TT} - 0.1 * V_{DDQ}		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:
1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
2. $V_{TT} = V_{DDQ}$/2.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = - 0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ}	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 * V_{DDQ}		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	-0.2 * V_{DDQ}		V	1
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:
1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
2. V_{REF} = V_{DDQ}/2; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM2G72D3MRQ8AG-D187E(I)

Table 17 - I_{DD} Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	837	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	963	mA	1, 2
Precharge power-down current; Slow exit	I_{DD2P0}	288	mA	1, 3
Precharge power-down current; Fast exit	I_{DD2P1}	396	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	576	mA	1, 3
Precharge standby current	I_{DD2N}	576	mA	1, 3
Precharge standby ODT current	I_{DD2NT}	612	mA	1, 2
Active power-down current	I_{DD3P}	612	mA	1, 3
Active standby current	I_{DD3N}	684	mA	1, 3
Burst read operating current	I_{DD4R}	1269	mA	1, 2
Burst write operating current	I_{DD4W}	1269	mA	1, 2
Refresh current	I_{DD5B}	2475	mA	1, 2
Self refresh temperature current: MAX T_{case} = 85°C	I_{DD6}	360	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T_{case} = 95°C	I_{DD6ET}	432	mA	1, 3
All banks interleaved read current	I_{DD7}	1530	mA	1, 2
Reset current	I_{DD8}	360	mA	1, 3

Notes:
1. Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.
2. One module rank in the active I_{DD}, the other rank in I_{DD2N}.
3. All DRAM in this I_{DD} conditions.

For part number IMM2G72D3MRQ8AG-D187E(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	Tcase = 0°C to 85°C	t_{CK}(DLL_DIS)	8	-	ns
	Tcase => 85°C to 95°C		8	-	
Clock periods average: DLL enable mode (CL = 7, CWL = 5)		t_{CK}(avg)	1.875	2.5	ns
High pulse width average		t_{CH}(avg)	0.47	0.53	t_{CK}(avg)
Low pulse width average		t_{CL}(avg)	0.47	0.53	t_{CK}(avg)
Clock period jitter	DLL locked	t_{JITper}	-90	90	ps
	DLL locking	$t_{JIT(per,lck)}$	-80	80	ps
Clock absolute period		t_{CK}(abs)	t_{CK}(avg) Min + t_{JITper} Min	t_{CK}(avg) Max + t_{JITper} Max	ps
Clock absolute high pulse width		t_{CH}(abs)	0.43	-	t_{CK}(avg)
Clock absolute low pulse width		t_{CL}(abs)	0.43	-	t_{CK}(avg)
Cycle-to-cycle jitter	DLL locked	t_{JITcc}	-	180	ps
	DLL locking	$t_{JIT(cc,lck)}$	-	160	ps
Cumulative error across	2 cycles	$t_{ERR(2per)}$	-132	132	ps
	3 cycles	$t_{ERR(3per)}$	-157	157	ps
	4 cycles	$t_{ERR(4per)}$	-175	175	ps
	5 cycles	$t_{ERR(5per)}$	-188	188	ps
	6 cycles	$t_{ERR(6per)}$	-200	200	ps
	7 cycles	$t_{ERR(7per)}$	-209	209	ps
	8 cycles	$t_{ERR(8per)}$	-217	217	ps
	9 cycles	$t_{ERR(9per)}$	-224	224	ps
	10 cycles	$t_{ERR(10per)}$	-231	231	ps
	11 cycles	$t_{ERR(11per)}$	-237	237	ps
	12 cycles	$t_{ERR(12per)}$	-242	242	ps
	n = 13,…49, 50 cycles	$t_{ERR(nper)}$	(1+0.68ln[n]) * t_{JITper} Min	(1+0.68ln[n]) * t_{JITper} Max	ps
DQ Input Timing					
Data setup time to DQS, /DQS	Base (specification)	$t_{DS(AC175)}$	25	-	ps
Data setup time to DQS, /DQS	Base (specification)	$t_{DS(AC150)}$	75	-	ps
Data hold time from DQS, /DQS	Base (specification)	$t_{DH(DC100)}$	100	-	ps
Minimum data pulse width		t_{DIPW}	490	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		t_{DQSQ}	-	150	ps
DQ output hold time from DQS, /DQS		t_{QH}	0.38	-	t_{CK}(avg)
DQ Low-Z time from CK, /CK		$t_{LZ(DQ)}$	-600	300	ps
DQ High-Z time from CK, /CK		$t_{HZ(DQ)}$	-	300	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		t_{DQSS}	-0.25	0.25	t_{CK}(avg)
DQS, /DQS differential input low pulse width		t_{DQSL}	0.45	0.55	t_{CK}(avg)
DQS, /DQS falling setup to CK, /CK rising		t_{DSS}	0.2	-	t_{CK}(avg)
DQS, /DQS falling hold from CK, /CK rising		t_{DSH}	0.2	-	t_{CK}(avg)
DQS, /DQS differential input high pulse width		t_{DQSH}	0.45	0.55	t_{CK}(avg)
DQS, /DQS differential WRITE preamble		t_{WPRE}	0.9	-	t_{CK}(avg)
DQS, /DQS differential WRITE postamble		t_{WPST}	0.3	-	t_{CK}(avg)

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Parameter / Condition		Symbol	Min	Max	Units
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		t_{DQSCK}	-300	300	ps
DQS, /DQS differential output high time		t_{QSH}	0.38	-	t_{CK}(avg)
DQS, /DQS differential output low time		t_{QSL}	0.38	-	t_{CK}(avg)
DQS, /DQS Low-Z time (RL-1)		$t_{LZ(DQS)}$	-600	300	ps
DQS, /DQS High-Z time (RL+BL/2)		$t_{HZ(DQS)}$	-	300	ps
DQS, /DQS differential READ preamble		t_{RPRE}	0.9		t_{CK}(avg)
DQS, /DQS differential READ postamble		t_{RPST}	0.3		t_{CK}(avg)
Command and Address Timing					
DLL locking time		t_{DLLK}	512	-	nCK
CTRL, CMD, ADDR setup to CK, /CK	Base (specification)	t_{IS}(AC175)	125	-	ps
CTRL, CMD, ADDR setup to CK, /CK	Base (specification)	t_{IS}(AC150)	275	-	ps
CTRL, CMD, ADDR hold from CK, /CK	Base (specification)	t_{IH}(DC100)	200	-	ps
Minimum CTRL, CMD, ADDR pulse width		t_{IPW}	780	-	ps
ACTIVATE to internal READ or WRITE delay		t_{RCD}	13.125	-	ns
PRECHARGE command period		t_{RP}	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		t_{RAS}	37.5	9 * t_{REFI}	ns
ACTIVATE-to-ACTIVATE command period		t_{RC}	50.625	-	ns
ACTIVATE-to-ACTIVATE minimum period (1KB page size)		t_{RRD}	greater of 4nCK or 7.5ns	-	-
ACTIVATE-to-ACTIVATE minimum period (2KB page size)		t_{RRD}	greater of 4nCK or 10ns	-	-
Four ACTIVATE windows (1KB page size)		t_{FAW}	37.5	-	ns
Four ACTIVATE windows (2KB page size)		t_{FAW}	50	-	ns
Write recovery time		t_{WR}	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		t_{WTR}	greater of 4nCK or 7.5ns	-	-
READ-to-PRECHARGE time		t_{RTP}	greater of 4nCK or 7.5ns	-	-
/CAS-to-/CAS command delay		t_{CCD}	4	-	nCK
Auto precharge write recovery + precharge time		t_{DAL}	WR + t_{RP}/ t_{CK}(avg)	-	nCK
MODE REGISTER SET command cycle time		t_{MRD}	4	-	nCK
MODE REGISTER SET command update delay		t_{MOD}	greater of 12nCK or 15ns	-	-
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		t_{MPRR}	1	-	nCK
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	t_{ZQinit}	greater of 512nCK or 640ns	-	-
	Normal operation	t_{ZQoper}	greater of 256nCK or 320ns	-	-
ZQCS command: Short calibration time		t_{ZQCS}	greater of 64nCK or 80ns	-	-
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		t_{XPR}	greater of 5nCK or t_{RFC}(min)+10ns	-	-
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		t_{RFC}	260	-	ns

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Parameter / Condition		Symbol	Min	Max	Units
Maximum refresh period	Tcase <= 85°C	-	64 (1X)		ms
	Tcase > 85°C		32 (2X)		
Maximum average periodic refresh	Tcase <= 85°C	t_{REFI}	7.8 (64ms/8192)		us
	Tcase > 85°C		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		t_{XS}	greater of 5 nCK or t_{RFC} Min+10ns	-	-
Exit self refresh to commands requiring a locked DLL		t_{XSDLL}	t_{DLLK} Min	-	nCK
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		t_{CKESR}	t_{CKE} Min + 1nCK	-	-
Valid clocks after self refresh entry or power down entry		t_{CKSRE}	greater of 5nCK or 10ns	-	-
Valid clocks before self refresh exit, power-down exit, or reset exit		t_{CKSRX}	greater of 5nCK or 10ns	-	-
Power-Down Timing					
CKE MIN pulse width		t_{CKE}	greater of 3nCK or 7.5ns	-	-
Command pass disable delay		t_{CPDED}	1	-	nCK
Power-down entry to power exit timing		t_{PD}	t_{CKE} Min	9 * t_{REFI}	-
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		$t_{ACTPDEN}$	1	-	nCK
PRECHARGE/PRECHARGE ALL command to power-down entry		t_{PRPDEN}	1	-	nCK
REFRESH command to power-down entry		$t_{REFPDEN}$	1	-	nCK
MRS command to power-down entry		$t_{MRSPDEN}$	t_{MOD} Min	-	nCK
READ/READ with auto precharge command to power-down entry		tRDPDEN	RL + 4 + 1	-	nCK
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	t_{WRPDEN}	WL + 4 + t_{WR}/t_{CK}(avg)	-	nCK
	BC4MRS	t_{WRPDEN}	WL + 2 + t_{WR}/t_{CK}(avg)	-	nCK
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t_{WRAPDEN}$	WL + 4 + t_{WR} + 1	-	nCK
	BC4MRS	$t_{WRAPDEN}$	WL + 2 + t_{WR} + 1	-	nCK
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		t_{XP}	greater of 3nCK or 7.5ns	-	-
Precharge power-down with DLL off to commands requiring a locked DLL		t_{XPDLL}	greater of 10nCK or 24ns	-	-
ODT Timing					
RTT turn-on from ODTL on reference		t_{AON}	-300	300	ps
RTT turn-off from ODTL off reference		t_{AOF}	0.3	0.7	t_{CK}(avg)
Asynchronous RTT turn-on delay (power-down with DLL off)		t_{AONPD}	2	8.5	ns
Asynchronous RTT turn-off delay (power-down with DLL off)		t_{AOFPD}	2	8.5	ns
ODT HIGH time with WRITE command and BL8		ODTH8	6	-	nCK
ODT HIGH time without WRITE command or WRITE command and BC4		ODTH4	4	-	nCK
Dynamic ODT Timing					
RTT dynamic change skew		t_{ADC}	0.3	0.7	t_{CK}(avg)
Write Leveling Timing					
First DQS, /DQS rising edge		t_{WLMRD}	40	-	nCK
DQS, /DQS delay		$t_{WLDQSEN}$	25	-	nCK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing		t_{WLS}	245	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing		t_{WLH}	245	-	ps
Write leveling output delay		t_{WLO}	0	9	ns
Write leveling output error		t_{WLOE}	0	2	ns

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Table 19 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of SPD Written / SPD Device Size / CRC Coverage	176, 256, 0-116	92
1	SPD Revision	Revision 1.2	12
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	Registered Mini-DIMM	05
4	SDRAM Density and Banks	4Gb 8banks	04
5	SDRAM Addressing	Row 16 / Col 10	21
6	Module Nominal Voltage, V_{DD}	1.5V	00
7	Module Organization	4Rank, x8	19
8	Module Memory Bus Width	ECC, 72bits	0B
9	Fine Timebase (FTB) Dividend / Divisor	2.5ps	52
10	Medium Timebase (MTB) Dividend	1ns	01
11	Medium Timebase (MTB) Divisor	8	08
12	SDRAM Minimum Cycle Time (t_{CK}min)	1.875ns	0F
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	5,6,7,8	1E
15	CAS Latencies Supported, Most Significant Byte	-	00
16	Minimum CAS Latency Time (t_{AA}min)	13.125ns	69
17	Minimum Write Recovery Time (t_{WR}min)	15ns	78
18	Minimum RAS# to CAS# Delay Time (t_{RCD}min)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (t_{RRD}min)	7.5ns	3C
20	Minimum Row Precharge Time (t_{RP}min)	13.125ns	69
21	Upper Nibbles for t_{RAS} and t_{RC}	-	11
22	Minimum Active to Precharge Time (t_{RAS}min), Least Significant Byte	37.5ns	2C
23	Minimum Active to Active/Refresh Time (t_{RC}min), Least Significant Byte	50.625ns	95
24	Minimum Refresh Recovery Time (t_{RFC}min), Least Significant Byte	260ns	20
25	Minimum Refresh Recovery Time (t_{RFC}min), Most Significant Byte	-	08
26	Minimum Internal Write to Read Command Delay Time (t_{WTR}min)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (t_{RTP}min)	7.5ns	3C
28	Upper Nibble for t_{FAW}	-	01
29	Minimum Four Activate Window Delay Time (t_{FAW}min)	37.5ns	2C
30	SDRAM Optional Features	DLL off, RZQ/7, RZQ/6	83
31	SDRAM Thermal and Refresh Options	ASR, 0°C-95°C, req. 2x Refresh	05
32	Module Thermal Sensor	Thermal Sensor incorporated	80
33	SDRAM Device Type	Dual Die Package	A1
34	Fine Offset for SDRAM Minimum Cycle Time (t_{CK}min)	-0ns	00
35	Fine Offset for Minimum CAS Latency Time (t_{AA}min)	-0ns	00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (t_{RCD}min)	-0ns	00
37	Fine offset for minimum Row Precharge Delay Time (t_{RP}min)	-0ns	00

Byte NO.	Description	Note	Hex
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (t_{RC}min)	-0ns	00
39-40	Reserved, General Section	-	00
41	SDRAM Maximum Activate Count (MAC) Value	8192*t_{REFI}, Untested MAC	00
42-59	Reserved. General Section	-	11
60	Raw Card Extension, Module Nominal Height	29<height<=30 mm	0F
61	Module Maximum Thickness	1< Tf <=2 mm, 1< Tb <=2 mm	11
62	Reference Raw Card	Non-JEDEC	1F
63	DIMM Module Attributes	1 Row of DRAM, 1 Register Used	05
64	RDIMM Thermal Heat Spreader Solution	No Heat Spreader incorporated	00
65-66	Register Manufacturer's JEDEC ID Code	-	00
67	Register Revision Number	Undefined	FF
68	Register Type	SSTE32882	00
69	RC1 (MS Nibble) / RC0 (LS Nibble)	-	00
70	RC3 (MS nibble) / RC2 (LS Nibble) – Drive Strength, Command/Address	Light Drive	00
71	RC5 (MS Nibble) / RC4 (LS Nibble) – Drive Strength, Control and Clock	Clock: Light Drive, Control: Light Drive	00
72	RC7 (MS Nibble) / RC6 (LS Nibble)	-	00
73	RC9 (MS Nibble) / RC8 (LS Nibble)	-	00
74	RC11 (MS Nibble) / RC10 (LS Nibble)	-	00
75	RC13 (MS Nibble) / RC12 (LS Nibble)	-	00
76	RC15 (MS Nibble) / RC14 (LS Nibble)	-	00
77-116	Reserved	-	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	I'M	04 9E
119	Module ID: Module Manufacturing Location	-	00
120-121	Module ID: Module Manufacturing Date	Manufacturer's data	-
122-125	Module ID: Module Serial Number	Manufacturer's data	-
126-127	SPD Cyclical Redundancy Code (CRC)	-	31 6A
128-145	Module Part Number	Manufacturer's data	-
146-147	Module Revision Code	-	00
148-149	DRAM Manufacturer's JEDEC ID Code	-	00
150-175	Manufacturer's Specific Data	Manufacturer's data	-
176-255	Open for Customer Use	-	00

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	Jun, 2021

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