

Datasheet | Rev. 1.0 | 2018

IMM2G72D3LMUD8AG (Die Revision C) 16GByte (2048M x 72 Bit)

16GB DDR3 ECC Unbuffered Mini-DIMM
RoHS Compliant Product

Remark:

Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures.

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Features

- 244-Pin Unbuffered Mini Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
 - PC3-12800: 5, 6, 7, 8, 9, 10, 11
 - PC3-10600: 5, 6, 7, 8, 9
- Programmable CAS Write Latency (CWL):
 - PC3-12800: 5, 6, 7, 8
 - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G72D3xMUD8AG-Czzzy	16GB	2Gx72	2	16GB DDR3 ECC Unbuffered Mini-DIMM

Notes:
 x: Operating Voltage
 y: Operating Temperature
 zzz: Speed Grade

Table 2 - Operating Voltage

Part Number	Operating Voltage
L	V _{DD} , V _{DDQ} = 1.35V (1.283V-1.45V) Backward compatible to V _{DD} , V _{DDQ} = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade

Part Number	Temperature Grade	T _{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < T_{case} <= 95 °C.

Table 4 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM2G72D3LMUD8AG-Czzzy	I'M	IM8G08D3FCBG	1.35V	1024Mx8	Lead Free

Part Number Decoder

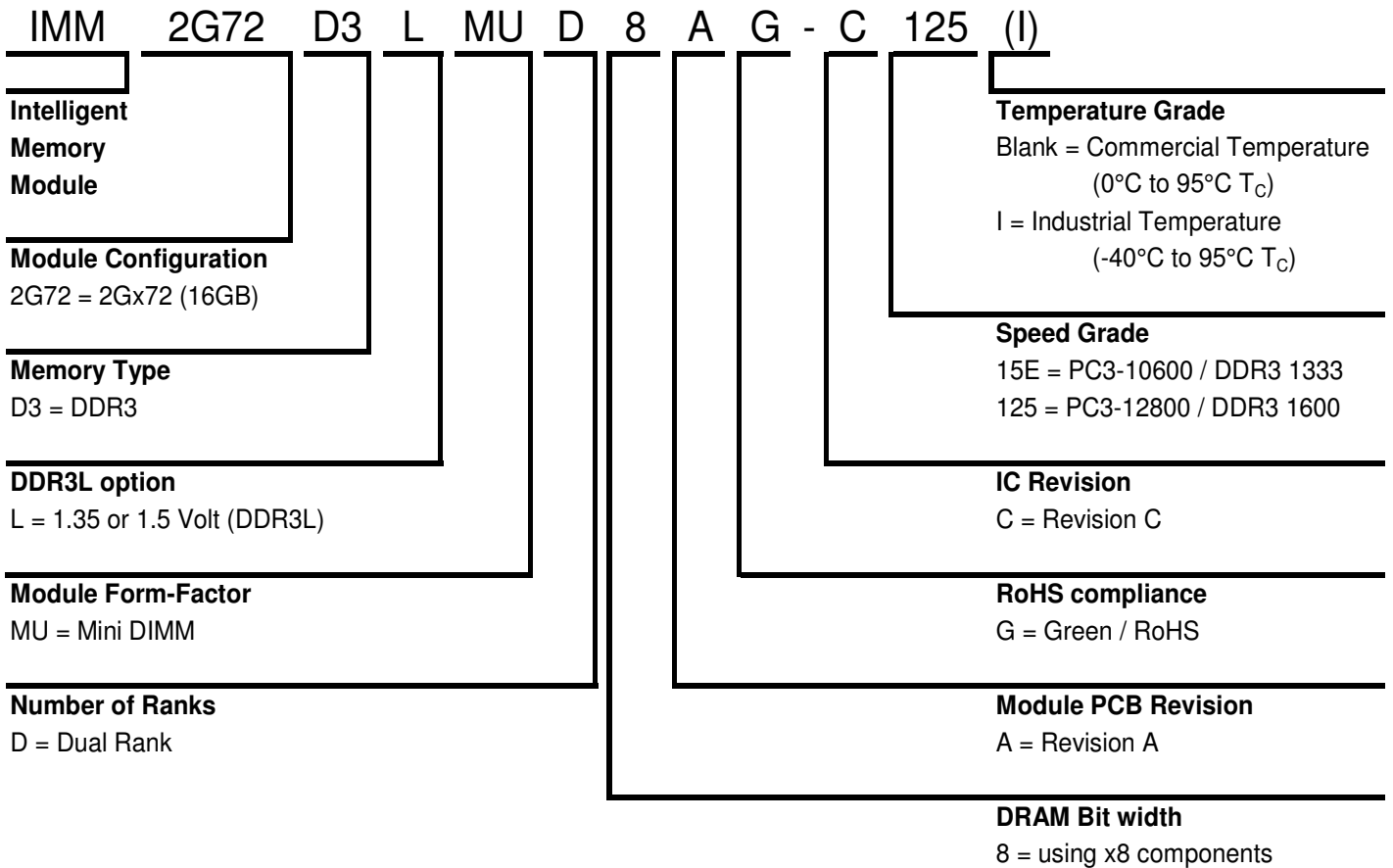


Table 6 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1024Mx8)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	18

Table 7 - Pin Assignment

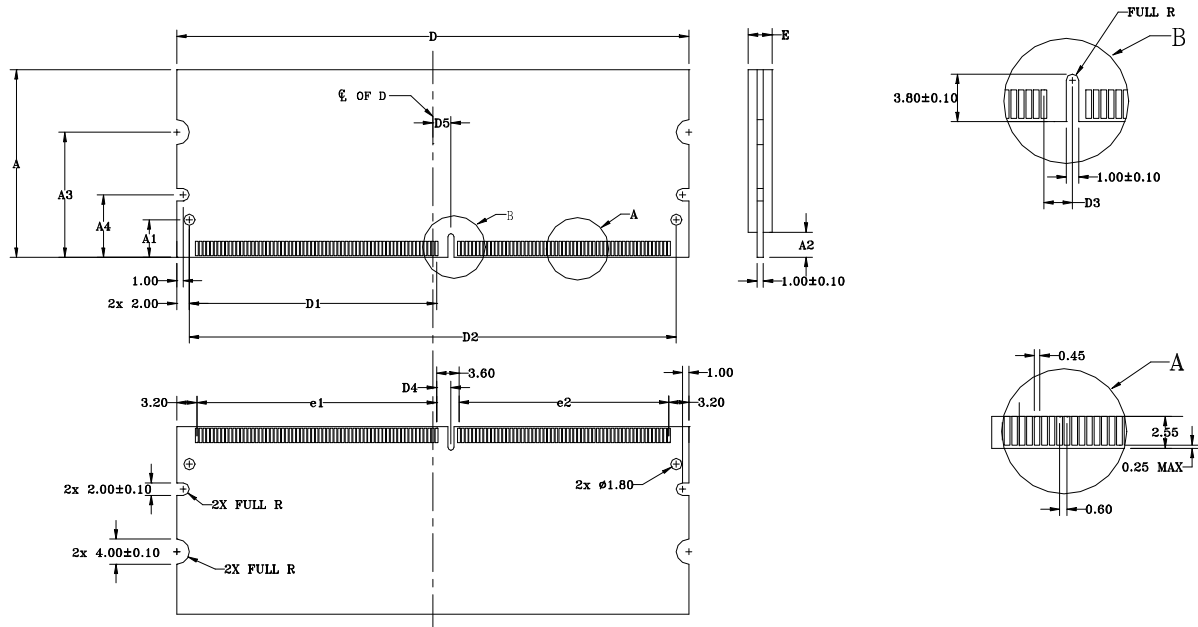
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V _{TT}	123	V _{TT}	62	A2	184	A1
2	V _{REFDQ}	124	V _{SS}	63	V _{DD}	185	V _{DD}
3	V _{SS}	125	DQ4	64	CK1	186	CK0
4	DQ0	126	DQ5	65	/CK1	187	/CK0
5	DQ1	127	V _{SS}	66	V _{DD}	188	V _{DD}
6	V _{SS}	128	DM0	67	V _{REFCA}	189	V _{DD}
7	/DQS0	129	NC	68	V _{DD}	190	/EVENT
8	DQS0	130	V _{SS}	69	NC	191	A0
9	V _{SS}	131	DQ6	70	V _{DD}	192	V _{DD}
10	DQ2	132	DQ7	71	A10/AP	193	BA1
11	DQ3	133	V _{SS}	72	BA0	194	V _{DD}
12	V _{SS}	134	DQ12	73	V _{DD}	195	/RAS
13	DQ8	135	DQ13	74	/WE	196	/S0
14	DQ9	136	V _{SS}	75	/CAS	197	V _{DD}
15	V _{SS}	137	DM1	76	V _{DD}	198	ODT0
16	/DQS1	138	NC	77	/S1	199	A13
17	DQS1	139	V _{SS}	78	ODT1	200	V _{DD}
18	V _{SS}	140	DQ14	79	V _{DD}	201	NC
19	DQ10	141	DQ15	80	NC	202	NC
20	DQ11	142	V _{SS}	81	NC	203	V _{SS}
21	V _{SS}	143	DQ20	82	V _{SS}	204	DQ36
22	DQ16	144	DQ21	83	DQ32	205	DQ37
23	DQ17	145	V _{SS}	84	DQ33	206	V _{SS}
24	V _{SS}	146	DM2	85	V _{SS}	207	DM4
25	/DQS2	147	NC	86	/DQS4	208	NC
26	DQS2	148	V _{SS}	87	DQS4	209	V _{SS}
27	V _{SS}	149	DQ22	88	V _{SS}	210	DQ38
28	DQ18	150	DQ23	89	DQ34	211	DQ39
29	DQ19	151	V _{SS}	90	DQ35	212	V _{SS}
30	V _{SS}	152	DQ28	91	V _{SS}	213	DQ44
31	DQ24	153	DQ29	92	DQ40	214	DQ45
32	DQ25	154	V _{SS}	93	DQ41	215	V _{SS}
33	V _{SS}	155	DM3	94	V _{SS}	216	DM5
34	/DQS3	156	NC	95	/DQS5	217	NC
35	DQS3	157	V _{SS}	96	DQS5	218	V _{SS}
36	V _{SS}	158	DQ30	97	V _{SS}	219	DQ46
37	DQ26	159	DQ31	98	DQ42	220	DQ47
38	DQ27	160	V _{SS}	99	DQ43	221	V _{SS}
39	V _{SS}	161	CB4	100	V _{SS}	222	DQ52
40	CB0	162	CB5	101	DQ48	223	DQ53
41	CB1	163	V _{SS}	102	DQ49	224	V _{SS}
42	V _{SS}	164	DM8	103	V _{SS}	225	DM6
43	/DQS8	165	NC	104	/DQS6	226	NC
44	DQS8	166	V _{SS}	105	DQS6	227	V _{SS}
45	V _{SS}	167	CB6	106	V _{SS}	228	DQ54
46	CB2	168	CB7	107	DQ50	229	DQ55
47	CB3	169	V _{SS}	108	DQ51	230	V _{SS}
48	V _{SS}	170	NC	109	V _{SS}	231	DQ60
49	NC	171	NC	110	DQ56	232	DQ61
50	/RESET	172	CKE1	111	DQ57	233	V _{SS}
51	CKE0	173	V _{DD}	112	V _{SS}	234	DM7
52	V _{DD}	174	A15	113	/DQS7	235	NC
53	BA2	175	A14	114	DQS7	236	V _{SS}
54	NC	176	V _{DD}	115	V _{SS}	237	DQ62
55	V _{DD}	177	A12, /BC	116	DQ58	238	DQ63
56	A11	178	A9	117	DQ59	239	V _{SS}
57	A7	179	V _{DD}	118	V _{SS}	240	VDDSPD
58	V _{DD}	180	A8	119	SA0	241	SA1
59	A5	181	A6	120	SCL	242	SDA
60	A4	182	V _{DD}	121	SA2	243	V _{SS}
61	V _{DD}	183	A3	122	V _{TT}	244	V _{TT}

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
V _{DD}	SDRAM core power supply	V _{REFDQ}	SDRAM I/O reference supply
V _{REFCA}	SDRAM command/address reference supply	V _{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS8	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS8	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM8	SDRAM data mask/high data strobes
CB0-CB7	DIMM ECC Check bit	NC	Spare Pins (no connect)
SCL	EEPROM clock	SDA	EEPROM data line
SA0-SA2	EEPROM address input	V _{DDSPD}	EEPROM positive power supply
/RESET	Reset Pin	V _{TT}	Termination Voltage

Module Dimension

Figure 1 - 244 Pin DDR3 SDRAM Unbuffered Mini-DIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1	6.00 Basic		
A2	4.00		
A3	20.00 Basic		
A4	10.00 Basic		
D	81.85	82.00	82.15
D1	39.60 Basic		
D2	78.00 Basic		
D3	2.30 Basic		
D4	2.30 Basic		
D5	2.90 Basic		
e1	38.40 Basic		
e2	33.60 Basic		
E			3.80

- Notes:
- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
 - Tolerances for all dimensions ±0.15 unless otherwise specified.
 - All dimensions are in millimeters.

Figure 2 - Functional Block Diagram (Page 1 of 2)

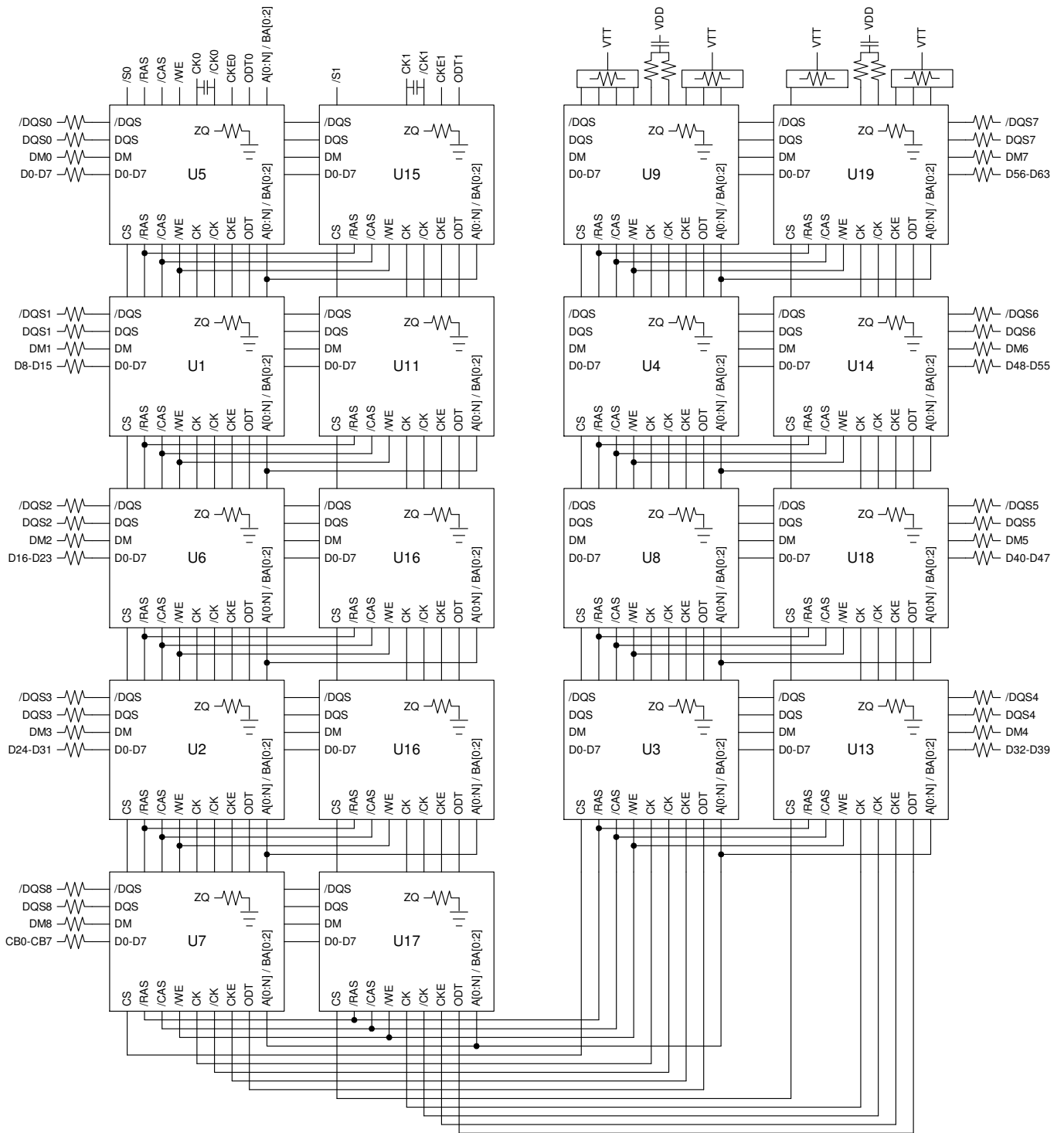
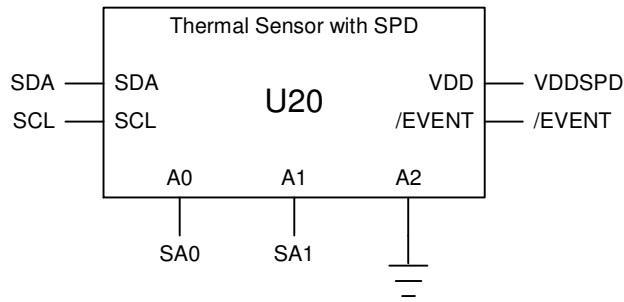
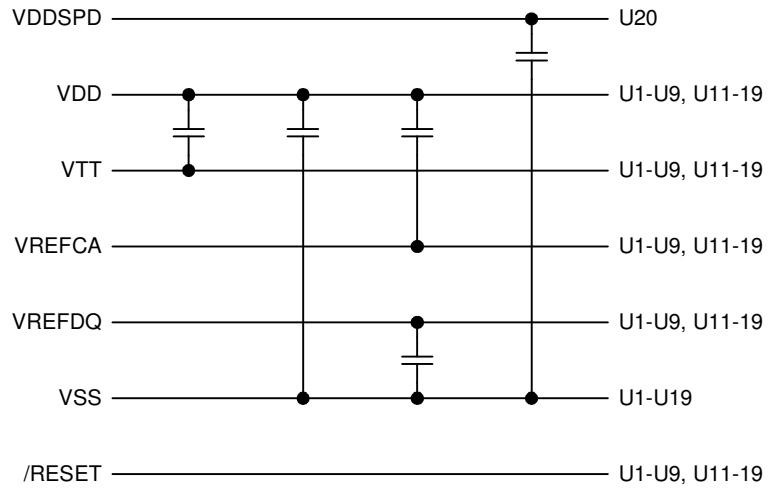


Figure 3 - Functional Block Diagram (Page 2 of 2)



Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V _{DD} , pin relative to V _{SS}	V _{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V _{DDQ} , pin relative to V _{SS}	V _{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V _{SS}	V _{IN} , V _{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T _{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature for Commercial temperature product	T _{case}	0 ~ 95	°C	2,4,5
DRAM Operation temperature for Industrial temperature product	T _{case}	-40 ~ 95	°C	2,4,5

- Notes:
- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
 - V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must not be greater than 0.6 x V_{DDQ}, when V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.
 - The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.
 - Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
Supply voltage	V _{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V _{DDQ}				V	1,2
Supply voltage	V _{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V _{DDQ}				V	1,2,3

- Notes:
- V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD}. V_{SS} = V_{SSQ}.
 - V_{DD} and V_{DDQ} may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
 - Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
V _{IN} low; DC/commands/address buses (1.35V)	V _{IL}	V _{SS}	-	-0.090	V	
V _{IN} low; DC/commands/address buses (1.5V)	V _{IL}	V _{SS}	-	-0.100	V	
V _{IN} high; DC/commands/address buses (1.35V)	V _{IH}	0.090	-	V _{DD}	V	
V _{IN} high; DC/commands/address buses (1.5V)	V _{IH}	0.100	-	V _{DD}	V	
Input reference voltage; command/address bus	V _{REFCA(DC)}	0.49* V _{DD}	0.50* V _{DD}	0.51* V _{DD}	V	1,2
I/O reference voltage DQ bus	V _{REFDQ(DC)}	0.49* V _{DD}	0.50* V _{DD}	0.51* V _{DD}	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V _{TT}	-	0.50* V _{DDq}	-	V	4

Notes:

- V_{REFCA(DC)} is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1% × V_{DD} around the V_{REFCA(DC)} value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of V_{REFCA(DC)}. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
- V_{REFDQ(DC)} is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1% × V_{DD} around the V_{REFDQ(DC)} value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of V_{REFDQ(DC)}.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		1.35V	1.5V	
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	$V_{IL(AC175)max}$	-	-175	mV

Parameter / Condition	Symbol	Value		Units
		1.35V	1.5V	
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	135	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-135	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)max}$	-160	-	mV

- Notes:
1. All voltages are referenced to V_{REF} . V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
 2. Input setup timing parameters (tIS and tDS) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
 3. Input hold timing parameters (tIH and tDH) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
 4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high - slew (1.35V)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high - slew (1.5V)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low - slew (1.35V)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low - slew (1.5V)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	$2 * (V_{IH(AC)} - V_{REF})$	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	$2 * (V_{IL(AC)} - V_{REF})$	mV	3
Single-ended high level for strobes (1.35V)	V_{SEH}	$V_{DDQ}/2 + 175$	-	mV	2
Single-ended high level for CK, /CK (1.35V)		$V_{DD}/2 + 175$	-	mV	2
Single-ended high level for strobes (1.5V)	V_{SEH}	$V_{DDQ}/2 + 175$	-	mV	2
Single-ended high level for CK, /CK (1.5V)		$V_{DD}/2 + 175$	-	mV	2
Single-ended low level for strobes (1.35V)	V_{SEL}	-	$V_{DDQ}/2 - 175$	mV	3
Single-ended low level for CK, /CK (1.35V)		-	$V_{DD}/2 - 175$	mV	3
Single-ended low level for strobes (1.5)	V_{SEL}	-	$V_{DDQ}/2 - 175$	mV	3
Single-ended low level for CK, /CK (1.5V)		-	$V_{DD}/2 - 175$	mV	3

Notes:

1. Defines slew rate reference points, relative to input crossing voltages.
2. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
3. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{TT} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{TT} + 0.1 * V_{DDQ}$ (1.35V)	SRQ_{se}	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{TT} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{TT} + 0.1 * V_{DDQ}$ (1.5V)	SRQ_{se}	2.5	5	V/ns	1,2,3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 * V_{DDQ}$		V	1,2
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	$0.5 * V_{DDQ}$		V	1,2
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 * V_{DDQ}$		V	1,2
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 * V_{DDQ}$		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 * V_{DDQ}$		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
2. $V_{TT} = V_{DDQ}/2$.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.35V)	SRQ_{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.5V)	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	$+0.2 * V_{DDQ}$		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	$-0.2 * V_{DDQ}$		V	1
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

- RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
- $V_{REF} = V_{DDQ}/2$; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM2G72D3LMUD8AG-C125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I _{DD0}	1251	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I _{DD1}	1485	mA	1, 2
Precharge power-down current; Slow exit	I _{DD2P0}	468	mA	1, 3
Precharge power-down current; Fast exit	I _{DD2P1}	900	mA	1, 3
Precharge quiet standby current	I _{DD2Q}	1224	mA	1, 3
Precharge standby current	I _{DD2N}	792	mA	1, 3
Precharge standby ODT current	I _{DD2NT}	1224	mA	1, 3
Active power-down current	I _{DD3P}	1008	mA	1, 3
Active standby current	I _{DD3N}	1296	mA	1, 3
Burst read operating current	I _{DD4R}	2151	mA	1, 2
Burst write operating current	I _{DD4W}	2295	mA	1, 2
Refresh current	I _{DD5B}	4329	mA	1, 2
Self refresh temperature current: MAX T _c = 85°C	I _{DD6}	540	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T _c = 95°C	I _{DD6ET}	720	mA	1, 3
All banks interleaved read current	I _{DD7}	3546	mA	1, 2
Reset current	I _{DD8}	414	mA	1, 3

Notes:

¹ Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.

² One module rank in the active IDD, the other rank in IDD2N.

³ All ranks in this IDD conditions.

For part number IMM2G72D3LMUD8AG-C125(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T _c = 0°C to 85°C	t ^{CK} (DLL_DIS)	8	-	ns
	T _c => 85°C to 95°C		8	-	
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		t ^{CK} (AVG)	1.25	<1.5	ns
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		t ^{CK} (AVG)	1.5	<1.875	ns
High pulse width average		t ^{CH} (AVG)	0.47	0.53	t ^{CK}
Low pulse width average		t ^{CL} (AVG)	0.47	0.53	t ^{CK}
Clock period jitter	DLL locked	t ^{JITper}	-70	70	ps
	DLL locking	t ^{JITper,lck}	-60	60	ps
Clock absolute period		t ^{CK} (ABS)	t ^{CK} (AVG) MIN + t ^{JITper} MIN	t ^{CK} (AVG) MAX + t ^{JITper} MAX	ps
Clock absolute high pulse width		t ^{CH} (ABS)	0.43	-	t ^{CK} (AVG)
Clock absolute low pulse width		t ^{CL} (ABS)	0.43	-	t ^{CK} (AVG)
Cycle-to-cycle jitter	DLL locked	t ^{JITcc}	140		ps
	DLL locking	t ^{JITcc,lck}	120		ps
Cumulative error across	2 cycles	t ^{ERR2per}	-103	103	ps
	3 cycles	t ^{ERR3per}	-122	122	ps
	4 cycles	t ^{ERR4per}	-136	136	ps
	5 cycles	t ^{ERR5per}	-147	147	ps
	6 cycles	t ^{ERR6per}	-155	155	ps
	7 cycles	t ^{ERR7per}	-163	163	ps
	8 cycles	t ^{ERR8per}	-169	169	ps
	9 cycles	t ^{ERR9per}	-175	175	ps
	10 cycles	t ^{ERR10per}	-180	180	ps
	11 cycles	t ^{ERR11per}	-184	184	ps
	12 cycles	t ^{ERR12per}	-188	188	ps
	n = 14,...49, 50 cycles	t ^{ERRnper}	(1+0.68ln[n]) * t ^{JITper} MIN	(1+0.68ln[n]) * t ^{JITper} Max	ps
DQ Input Timing					
Data setup time to DQS, /DQS (1.35V)	Base (specification)	t ^{DS} (AC135)	25	-	ps
					ps
Data setup time to DQS, /DQS (1.5V)	Base (specification)	t ^{DS} (AC150)	10	-	ps
					ps
Data hold time from DQS, /DQS (1.35V)	Base (specification)	t ^{DH} (DC90)	55	-	ps
					ps
Data hold time from DQS, /DQS (1.5V)	Base (specification)	t ^{DH} (DC100)	45	-	ps
					ps
Minimum data pulse width		t ^{DIPW}	360	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		t ^{DQSQ}	-	100	ps
DQ output hold time from DQS, /DQS		t ^{QH}	0.38	-	t ^{CK} (AVG)
DQ Low-Z time from CK, /CK		t ^{LZDQ}	-450	225	ps
DQ High-Z time from CK, /CK		t ^{HZDQ}	-	225	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		t ^{DQSS}	-0.27	0.27	t ^{CK}
DQS, /DQS differential input low pulse width		t ^{DQSL}	0.45	0.55	t ^{CK}

For part number IMM2G72D3LMUD8AG-C125(I)

Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		^t DSS	0.18	-	^t CK
DQS, /DQS falling hold from CK, /CK rising		^t DSH	0.18	-	^t CK
DQS, /DQS differential input high pulse width		^t DQSH	0.45	0.55	^t CK
DQS, /DQS differential WRITE preamble		^t WPRE	0.9	-	^t CK
DQS, /DQS differential WRITE postamble		^t WPST	0.3	-	^t CK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		^t DQSK	-225	225	ps
DQS, /DQS differential output high time		^t QSH	0.40	-	^t CK
DQS, /DQS differential output low time		^t QSL	0.40	-	^t CK
DQS, /DQS Low-Z time (RL-1)		^t LZDQS	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		^t HZDQS	-	225	ps
DQS, /DQS differential READ preamble		^t RPRE	0.9	greater of ^t LZ(DQS)(MIN) or ^t DQSK(DQS)(MAX)	^t CK
DQS, /DQS differential READ postamble		^t RPST	0.3	greater of ^t DQSK(MIN) + ^t QSH(MIN) or ^t HZ(DQS)(MAX)	^t CK
Command and Address Timing					
DLL locking time		^t DLLK	512	-	^t CK
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	^t IS (AC160)	60	-	ps
					ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	^t IS (AC135)	185	-	ps
					ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	^t IS (AC175)	45	-	ps
					ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	^t IS (AC150)	170	-	ps
					ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V)	Base (specification)	^t IH (DC90)	130	-	ps
					ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V)	Base (specification)	^t IH (DC100)	120	-	ps
					ps
Minimum CTRL, CMD, ADDR pulse width		^t IPW	560	-	ps
ACTIVATE to internal READ or WRITE delay		^t RCD	13.125	-	ns
PRECHARGE command period		^t RP	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		^t RAS	35	9 * ^t REFI	ns
ACTIVATE-to-ACTIVATE command period		^t RC	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period		^t RRD	greater of 4 ^t CK or 6ns	-	^t CK
Four ACTIVATE windows (1KB page size)		^t FAW	40	-	ns
Write recovery time		^t WR	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		^t WTR	greater of 4 ^t CK or 7.5ns	-	^t CK
READ-to-PRECHARGE time		^t RTP	greater of 4 ^t CK or 7.5ns	-	^t CK
/CAS-to-/CAS command delay		^t CCD	4 ^t CK	-	^t CK
Auto precharge write recovery + precharge time		^t DAL	WR + ^t RP/ ^t CK (AVG)	-	^t CK
MODE REGISTER SET command cycle time		^t MRD	4	-	^t CK
MODE REGISTER SET command update delay		^t MOD	greater of 12 ^t CK or 15ns	-	^t CK
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^t MPRR	1	-	^t CK

For part number IMM2G72D3LMUD8AG-C125(I)

Parameter / Condition		Symbol	Min	Max	Units
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	$t'ZQ_{init}$	512	-	$t'CK$
	Normal operation	$t'ZQ_{oper}$	256	-	$t'CK$
ZQCS command: Short calibration time		$t'ZQ_{cs}$	64	-	$t'CK$
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		$t'XPR$	greater of $5t'CK$ or $t'RFC(min)+10ns$	-	$t'CK$
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		$t'RFC$	300	-	ns
Maximum refresh period	$T_c \leq 85^\circ C$	-	64 (1X)		ms
	$T_c > 85^\circ C$	-	32 (2X)		
Maximum average periodic refresh	$T_c \leq 85^\circ C$	$t'REFI$	7.8 (64ms/8192)		us
	$T_c > 85^\circ C$		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		$t'XS$	greater of $5t'CK$ or $t'RFC+10ns$	-	$t'CK$
Exit self refresh to commands requiring a locked DLL		$t'XSDLL$	$t'DLLK (MIN)$	-	$t'CK$
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		$t'CKESR$	$t'CKE (MIN) + t'CK$	-	$t'CK$
Valid clocks after self refresh entry or power down entry		$t'CKSRE$	greater of $5t'CK$ or $10ns$	-	$t'CK$
Valid clocks before self refresh exit, power-down exit, or reset exit		$t'CKSRX$	greater of $5t'CK$ or $10ns$	-	$t'CK$
Power-Down Timing					
CKE MIN pulse width		$t'CKE (MIN)$	greater of $3t'CK$ or $5ns$		$t'CK$
Command pass disable delay		$t'CPDED$	1	-	$t'CK$
Power-down entry to power exit timing		$t'PD$	$t'CKE (MIN)$	$9 * t'REFI$	$t'CK$
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		$t'ACTPDEN$	MIN = 1		$t'CK$
PRECHARGE/PRECHARGE ALL command to power-down entry		$t'PRPDEN$	MIN = 1		$t'CK$
REFRESH command to power-down entry		$t'REFPDEN$	MIN = 1		$t'CK$
MRS command to power-down entry		$t'MRSPDEN$	MIN = $t'MOD (MIN)$		$t'CK$
READ/READ with auto precharge command to power-down entry		$t'RDPDEN$	MIN = $RL + 4 + 1$		$t'CK$
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t'WRPDEN$	MIN = $WL + 4 + t'WR/t'CK (AVG)$		$t'CK$
	BC4MRS	$t'WRPDEN$	MIN = $WL + 2 + t'WR/t'CK (AVG)$		$t'CK$
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t'WRAPDEN$	MIN = $WL + 4 + t'WR + 1$		$t'CK$
	BC4MRS	$t'WRAPDEN$	MIN = $WL + 2 + t'WR + 1$		$t'CK$
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		$t'XP$	greater of $3t'CK$ or $6ns$	-	$t'CK$
Precharge power-down with DLL off to commands requiring a locked DLL		$t'XPDLL$	greater of $10t'CK$ or $24ns$	--	$t'CK$

For part number IMM2G72D3LMUD8AG-C125(I)

Parameter / Condition	Symbol	Min	Max	Units
ODT Timing				
R _{TT} turn-on from ODTL on reference	^t AON	-225	225	ps
R _{TT} turn-off from ODTL off reference	^t AOF	0.3	0.7	CK
Asynchronous R _{TT} turn-on delay (power-down with DLL off)	^t AONPD	2	8.5	ns
Asynchronous R _{TT} turn-off delay (power-down with DLL off)	^t AOFPD	2	8.5	ns
ODT HIGH time with WRITE command and BL8	ODTH8	6	-	^t CK
ODT HIGH time without WRITE command or WRITE command and BC4	ODTH4	4	-	^t CK
Dynamic ODT Timing				
R _{TT} dynamic change skew	^t ADC	0.3	0.7	^t CK
Write Leveling Timing				
First DQS, /DQS rising edge	^t WLMRD	40	-	^t CK
DQS, /DQS delay	^t WLDQSEN	25	-	^t CK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	^t WLS	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	^t WLH	165	-	ps
Write leveling output delay	^t WLO	0	7.5	ns
Write leveling output error	^t WLOE	0	2	ns

For part number IMM2G72D3LMUD8AG-C125(I)

Table 19 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116	92
1	SPD Revision	1.2	12
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	Unbuffered Mini-DIMM	06
4	SDRAM Density and Banks	8Gb 8banks	05
5	SDRAM Addressing	Row 16 / Col 11	22
6	Module Nominal Voltage, V _{DD}	1.35V/1.5V	02
7	Module Organization	2Rank , x8	09
8	Module Memory Bus Width	ECC, 72bit	0B
9	Fine Timebase (FTB) Dividend and Divisor	2.5ps	52
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)	01
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9, 10, 11	FE
15	CAS Latencies Supported, Most Significant Byte	-	00
16	Minimum CAS Latency Time (tAamin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	7.5ns	3C
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibbles for tRAS and tRC	-	11
22	Minimum Active to Precharge Time (tRASmin), LSB	35ns	18
23	Minimum Active to Active/Refresh Time (tRCmin), LSB	48.125ns	81
24	Minimum Refresh Recovery Time (tRFCmin), LSB	300ns	60
25	Minimum Refresh Recovery Time (tRFCmin), MSB	300ns	09
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	40ns	01
29	Minimum Four Activate Window Delay Time (tFAWmin), LSB	40ns	40
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	0-95oC Op. Temp. w/2x refresh	05
32	Module Thermal Sensor	With TS	80
33	SDRAM Device Type	Non-Standard SDRAM	A1
34-59	Reserved, General Section	-	00
60	Module Nominal Height	29< Height <= 30	0F

Byte NO.	Description	Note	Hex
61	Module Maximum Thickness	1 < Tf <= 2 (mm); 1 < Tb <= 2 (mm)	11
62	Reference Raw Card Used	Non-Jedec/Trade	1F
63	Address Mapping from Edge Connector to DRAM	Non-Mirrored	00
64-116	Module Type Specific Section, Indexed by Key Byte	-	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Reserved	Reserved
119	Module ID: Module Manufacturing Location	Reserved	Reserved
120-121	Module ID: Module Manufacturing Date	Reserved	Reserved
122-125	Module ID: Module Serial Number	Reserved	Reserved
126-127	Cyclical Redundancy Code	-	60 FC
128-145	Module Part Number	Reserved	Reserved
146-147	Module Revision Code	Reserved	Reserved
148-149	DRAM Manufacturer's JEDEC ID Code	Reserved	Reserved
150-175	Manufacturer's Specific Data	Reserved	Reserved
176-255	Open For Customer Use	Reserved	Reserved

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	Mar, 2018

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