IM2516SDBDB
256Mbit SDRAM
4 BANKS X 4Mbit X 16

Ordering Speed Code	-6
	166 MHz
Clock Cycle time (min.) (t_{CK3})	6
Access time from CLK (max.) (t_{AC3})	5
Row Active time (min.) (t_{RAS})	42
Row Cycle time (min.) (t_{RC})	60

Features

- 4 banks x 4Mbit x 16 organization
- High speed data transfer rates up to 166 MHz
- Full Synchronous operation
- Internal pipelined architecture
- Programmable $\overline{CAS}$ Latency: 2, 3
- Burst Type: Sequential or Interleaved
- Programmable Burst Length:
  - 1, 2, 4, 8 or full page
- Burst stop function
- CKE Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 refresh cycles/64ms
- Available in 54 Pin TSOP II and 54-ball FBGA
- LVTTL Interface
- Single 3.3 V ± 0.3 V Power Supply
- Lead-free/RoHS
- Operating Temperature Range
  - Commercial Tambient = 0°C to +70°C
  - Industrial Tambient = -40°C to +85°C

Option	Marking
• Configuration	
- 16Mx16 (4 Banks x 4Mbit x 16)	2516
• Package	
- 54-ball FBGA (8mm x 8mm)	B
• Leaded/Lead-free	
- Leaded	<blank>
- Lead-free/RoHS	G
• Speed/Cycle Time	
- 6 ns @ CL3 (PC166)	-6
• Temperature	
- Commercial 0°C to +70°C Tambient	<blank>
- Industrial -40°C to +85°C Tambient	I

Example Part Number: IM2516SDBDBG-6I

Description

The IM2516SDBDB is a four bank Synchronous DRAM organized as 4 banks x 4Mbit x 16. The IM2516SDBDB achieves high speed data transfer rates up to 166 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 166 MHz is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

Part Number Information

IM 25 16 SD B D B G - 6 (I)

Intelligent Memory

IC capacity
25 = 256Mbit

DRAM I/O width
16 = x16

Memory Type
SD = SDRAM

Voltage
B = 3.3V

IC Revision
D = Revision D

Package
B = FBGA

RoHS-compliance
G = Green / RoHS
Blank = Leaded

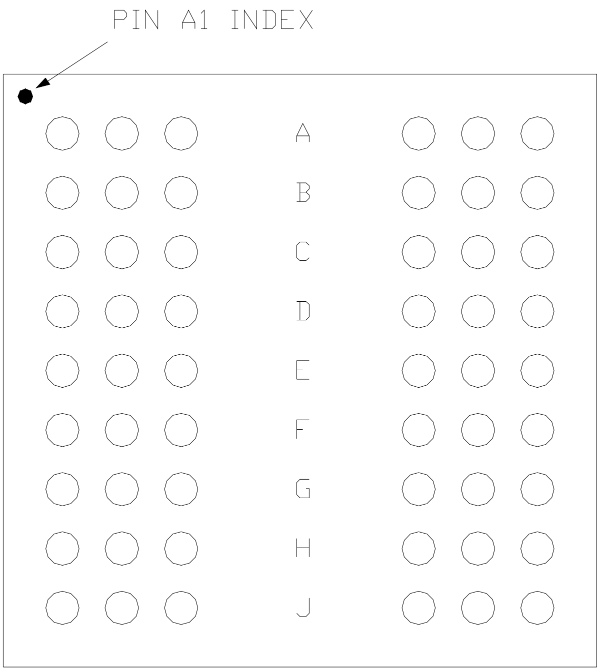
Speed Grade
6 = 166MHz CL3 (SDRAM)

Temperature range
Blank = Commercial Temperature 0°C to +70°C Tambient
I = Industrial Temperature -40°C to +85°C Tambient

Pin Configurations

54-ball FBGA (x16 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{SS}	DQ15	V_{SSQ}				V_{DDQ}	DQ0	V_{DD}	A
B	DQ14	DQ13	V_{DDQ}				V_{SSQ}	DQ2	DQ1	B
C	DQ12	DQ11	V_{SSQ}				V_{DDQ}	DQ4	DQ3	C
D	DQ10	DQ9	V_{DDQ}				V_{SSQ}	DQ6	DQ5	D
E	DQ8	NC	V_{SS}				V_{DD}	LDQM	DQ7	E
F	UDQM	CLK	CKE				$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$	F
G	A12	A11	A9				BA0	BA1	$\overline{CS}$	G
H	A8	A7	A6				A0	A1	A10	H
J	V_{SS}	A5	A4				A3	A2	V_{DD}	J



TOP VIEW
(See the ball through the package)

*Capacitance**

(at Tambient = 25°C, $V_{DD} = V_{DDQ}$ = 3.3 V ± 0.3 V)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	2	4	pF
Input/Output Capacitance	$C_{I/O}$	4	6	pF

*Note: These parameters are periodically sampled and not 100% tested.

*Absolute Maximum Ratings**

Operating temperature range:

Tambient: 0°C to +70°C for Commercial Temp.

Tambient: -40°C to +85°C for Industrial Temp.

Storage temperature range……………………………...….-55°C to +150°C

Input/output voltage…………………..……….…...……….-1.0 V to 4.6 V

Power supply voltage……………..……….….…………....-1.0 V to 4.6 V

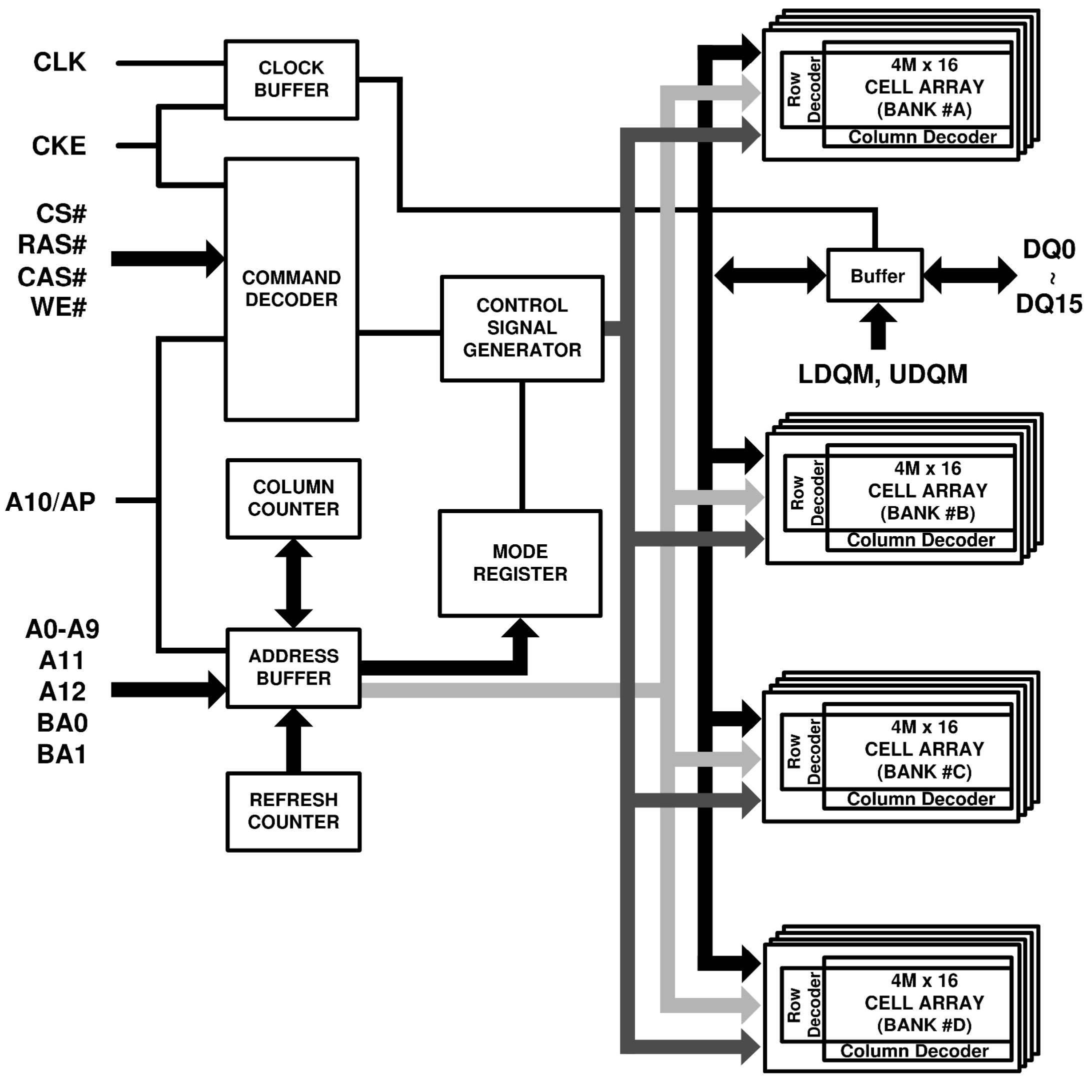
Power dissipation………………………………...………….….......1W

Data out current (short circuit)……………………….………….….50mA

Note: Stresses above those listed under “Absolute Maximum Ratings may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram

x16 Configuration



Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A12	Input	Level	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends from the SDRAM organization: • 4M x 16 SDRAM CA0–CA8. In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will BA0 and BA1 are used to define which bank to precharge.
BA0, BA1	Input	Level	-	Selects which bank is to be active.
DQx	Input Output	Level	-	Data Input/Output pins operate in the same manner as on conventional DRAMs.
LDQM, UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
V_{DD}, V_{SS}	Supply	-	-	Power and ground for the input buffers and the core logic.
V_{DDQ}, V_{SSQ}	Supply	-	-	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Command	State	CKE_{n-1}	CKE_n	DQM	BA0,1	A10	A0-9,11-12	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	V	V	L	Column address (A0 ~ A8)	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	V	V	H		L	H	L	L
Read	Active(3)	H	X	V	V	L	Column address (A0 ~ A8)	L	H	L	H
Read and AutoPrecharge	Active(3)	H	X	V	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
No-operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	H	X	X	X
								L	V	V	V
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

1. V=Valid, X=Don't Care, L=Low level, H=High level
2. CKE_n signal is input level when commands are provided.
   CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
   When this command is asserted in the burst cycle, device state is clock suspend mode.

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed V_{DD}+0.3 V on any of the input pins or V_{DD} supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 us is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of two Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is di- vided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cy- cle (interleaved or sequential), a $\overline{CAS}$ Latency Field to set the access time at clock cycle and a Operation mode field to differentiate between normal op- eration (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate com- mand after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation.

After the mode register is set, a Standby or NOP command is re- quired. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set op- eration. Address input data at this timing defines pa- rameters to be set as shown in the previous table.

Read and Write Operation

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.
SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column address- es are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first ad- dress is ‘2’, then the rest of the burst sequence is 3,
0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using sequential burst type. Full Page burst operation does not terminate once the burst length has been reached. (At the end of the page, it will wrap to the start address and continue.) In other words, unlike burst length of 2, 4, and 8, full page burst continues until it is terminated using another command.

Address Input for Mode Set (Mode Register Operation)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU*	0	RFU*			WBL	Test Mode		CAS Latency			BT	Burst Length		

A9	Write Burst Length
0	Burst
1	Single Bit

A8	A7	Test Mode
0	0	Normal
1	0	Vendor Use Only
0	1	Vendor Use Only

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
All other Reserved			

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	1	1	Full Page (Sequential)
All other Reserved			

*Note: RFU (Reserved for future use) should stay “0” during MRS cycle.

Similar to the page mode of conventional DRAM’s, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0 xx1	0, 1 1, 0	0, 1 1, 0
4	x00 x01 x10 x11	0, 1, 2, 3 1, 2, 3, 0 2, 3, 0, 1 3, 0, 1, 2	0, 1, 2, 3 1, 0, 3, 2 2, 3, 0, 1 3, 2, 1, 0
8	000 001 010 011 100 101 110 111	0 1 2 3 4 5 6 7 1 2 3 4 5 6 7 0 2 3 4 5 6 7 0 1 3 4 5 6 7 0 1 2 4 5 6 7 0 1 2 3 5 6 7 0 1 2 3 4 6 7 0 1 2 3 4 5 7 0 1 2 3 4 5 6	0 1 2 3 4 5 6 7 1 0 3 2 5 4 7 6 2 3 0 1 6 7 4 5 3 2 1 0 7 6 5 4 4 5 6 7 0 1 2 3 5 4 7 6 1 0 3 2 6 7 4 5 2 3 0 1 7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2....	not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ - before - $\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.
The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.
The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are dis- abled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (t_{RP}) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (t_{REF}) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for mode entry and exit.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for $\overline{CAS}$ latencies 2, two clocks for $\overline{CAS}$ latencies 3 and three clocks for $\overline{CAS}$ latencies 4. If CA10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} (Write recovery time) after the last data in. **Auto-Precharge** does not apply to full-page burst mode.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2, two clocks before the last data out for $\overline{CAS}$ latency = 3. Writes require a time delay twr from the last data out to apply the precharge command. A full-page burst may be truncated with a Precharge command to the same bank.

Bank Selection by Address Bits:

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	All Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory. The full-page burst is used in conjunction with Burst Terminate Command to generate arbitrary burst lengths.

Recommended D.C. Operating Conditions

V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	1
Input low voltage	V_{IL}	-0.3	0.8	V	1
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	-	V	
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	-	0.4	V	
Input leakage current (0 V < V_{IN} < V_{DD}, all other pins not under test = 0 V)	I_{IL}	-10	10	uA	
Output leakage current (Output disable, 0 V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-10	10	uA	

Notes:

1. All voltages are referenced to V_{SS}. Overshoot V_{IH} (Max) = 4.6 V for pulse width ≤ 3 ns. Undershoot V_{IL} (Min) = -1.0 V for pulse width ≤ 3 ns.

Operating Currents

V_{DD} = 3.3 V ± 0.3 V (Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter & Test Condition	Max.	Unit	Notes
		-6		
I_{DD1}	Operating Current $t_{RC} \geq t_{RC}$ (min), Outputs Open One bank active	60	mA	1
I_{DD2P}	Precharge Standby Current in power down mode t_{CK} = 15ns, CKE ≤ V_{IL} (max)	2	mA	
I_{DD2PS}	Precharge Standby Current in power down mode $t_{CK} = \infty$, CKE ≤ V_{IL} (max)	2	mA	
I_{DD2N}	Precharge Standby Current in non-power down mode t_{CK} = 15ns, CS# ≥ V_{IH} (min), CKE ≥ V_{IH}, Input signals are changed every 2clks	30	mA	
I_{DD2NS}	Precharge Standby Current in non-power down mode $t_{CK} = \infty$, CLK ≤ V_{IL} (max), CKE ≥ V_{IH}	18	mA	
I_{DD3NS}	Active Standby Current in non-power down mode CKE ≥ V_{IH} (min), CLK ≤ V_{IL} (max), $t_{CK} = \infty$	40	mA	
I_{DD3N}	Active Standby Current in non-power down mode t_{CK} = 15ns, CKE ≥ V_{IH} (min), CS# ≥ V_{IH} (min), Input signals are changed every 2clks	40	mA	
I_{DD4}	Operating Current (Burst mode) $t_{CK} = t_{CK}$ (min), Outputs Open, Multi-bank interleave	62	mA	1,2
I_{DD5}	Refresh Current $t_{RC} \geq t_{RC}$ (min)	80	mA	1
I_{DD6}	Self-Refresh Current CKE ≤ 0.2V; for other inputs V_{IH} ≥ VDD - 0.2V, V_{IL} ≤ 0.2V	2	mA	

Notes:

1. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during every 2 t_{CK}.
2. These parameters depend on output loading. Specified values are obtained with output open.

AC Characteristics

V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V

#	Symbol	Parameter	Limit Values		Unit	Notes
			-6			
			Min.	Max.		
1	t_{CK}	Clock Cycle Time $\overline{CAS}$ Latency = 2 $\overline{CAS}$ Latency = 3	 10 6	 - -	ns	2
2	t_{AC}	Access Time from Clock $\overline{CAS}$ Latency = 2 $\overline{CAS}$ Latency = 3	 - -	 6 5	ns	3
3	t_{RCD}	Row to Column Delay Time	18	-	ns	
4	t_{RP}	Row Precharge Time	18	-	ns	
5	t_{RAS}	Row Active Time	42	120K	ns	
6	t_{RC}	Row Cycle Time	60	-	ns	
7	t_{RRD}	Activate(a) to Activate(b) Command Period	12	-	ns	
8	t_{OH}	Data Output Hold Time	2.5	-	ns	2
9	t_{LZ}	Data Output to Low Impedance Time	0	-	ns	
10	t_{HZ}	Data Output to High Impedance Time	-	5	ns	1
11	t_{WR}	Write Recovery Time	12	-	ns	
12	t_{IS}	Data/Address/Control Input set-up time	1.5	-	ns	3
13	t_{IH}	Data/Address/Control Input hold time	0.8	-	ns	3
14	t_{PDE}	Power Down Exit set-up time	$t_{IS} + t_{CK}$	-	ns	
15	t_{REFI}	Refresh Interval Time	-	7.8	us	
16	t_{XSR}	Exit Self Refresh to any Command	$t_{IS} + t_{RC}$	-	ns	
17	t_{RFC}	Refresh cycle time	60	-	ns	
18	t_{MRD}	Mode register set cycle time	12	-	ns	
19	t_{CH}	Clock high time	2	-	ns	3
20	t_{CL}	Clock low time	2	-	ns	3

Notes:

1. t_{HZ} defines the time in which the outputs achieve the open circuit condition and are not at reference levels.
2. If clock rising time is longer than 1 ns, (t_R / 2 – 0.5) ns should be added to the parameter.
3. Assumed input rise and fall time t_T (t_R & t_F) = 1 ns
   If t_R or t_F is longer than 1 ns, transient time compensation should be considered, i.e., [(t_r + t_f) / 2 – 1] ns should be added to the parameter.

Timing Diagrams

1. Bank Activate Command Cycle

2. Burst Read Operation

3. Read Interrupted by a Read

4. Read to Write Interval

    4.1 Read to Write Interval
    4.2 Minimum Read to Write Interval
    4.3 Non-Minimum Read to Write Interval

5. Burst Write Operation

6. Write and Read Interrupt

    6.1 Write Interrupted by a Write
    6.2 Write Interrupted by Read

7. Burst Write & Read with Auto-Precharge

    7.1 Burst Write with Auto-Precharge
    7.2 Burst Read with Auto-Precharge

8. Burst Termination

    8.1 Termination of a Burst Write Operation
    8.2 Termination of a Burst Write Operation

9. AC- Parameters

    9.1 AC Parameters for a Write Timing
    9.2 AC Parameters for a Read Timing

10. Mode Register Set

11. Power on Sequence and Auto Refresh (CBR)

12. Power Down Mode

13. Self Refresh (Entry and Exit)

14. Auto Refresh (CBR)

Timing Diagrams (Cont'd)

15. Random Column Read (Page within same Bank)

    15.1 $\overline{CAS}$ Latency = 2
    15.2 $\overline{CAS}$ Latency = 3

16. Random Column Write (Page within same Bank)

    16.1 $\overline{CAS}$ Latency = 2
    16.2 $\overline{CAS}$ Latency = 3

17. Random Row Read (Interleaving Banks) with Precharge

    17.1 $\overline{CAS}$ Latency = 2
    17.2 $\overline{CAS}$ Latency = 3

18. Random Row Write (Interleaving Banks) with Precharge

    18.1 $\overline{CAS}$ Latency = 2
    18.2 $\overline{CAS}$ Latency = 3

19. Precharge Termination of a Burst

    19.1 $\overline{CAS}$ Latency = 2
    19.2 $\overline{CAS}$ Latency = 3

20. Full Page Burst Operation

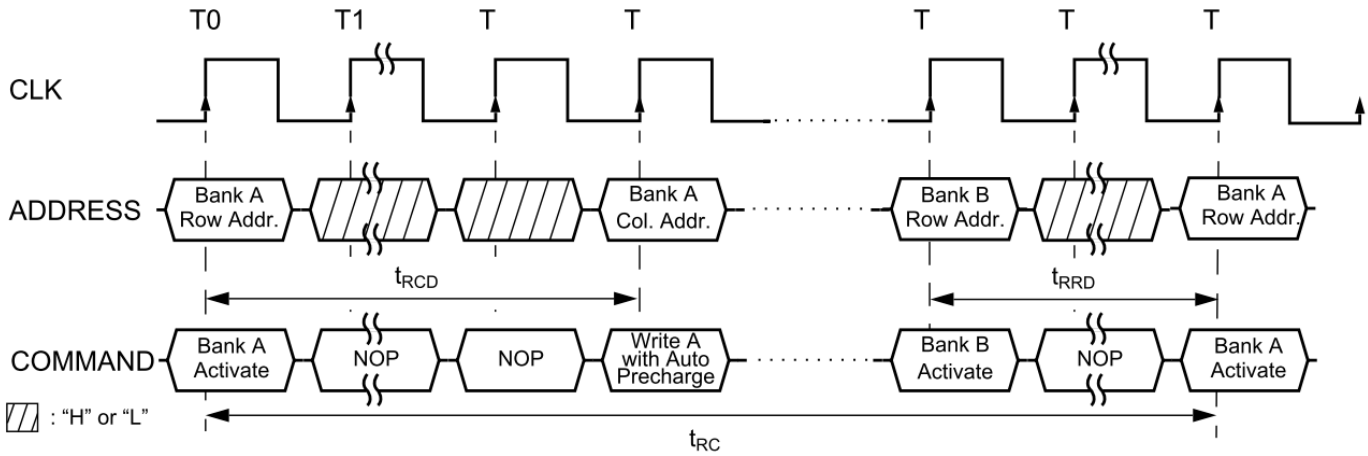
    20.1 Full Page Burst Read, $\overline{CAS}$ Latency = 2
    20.2 Full Page Burst Read, $\overline{CAS}$ Latency = 3

21. Full Page Burst Operation

    21.1 Full Page Burst Write, $\overline{CAS}$ Latency = 2
    21.2 Full Page Burst Write, $\overline{CAS}$ Latency = 3

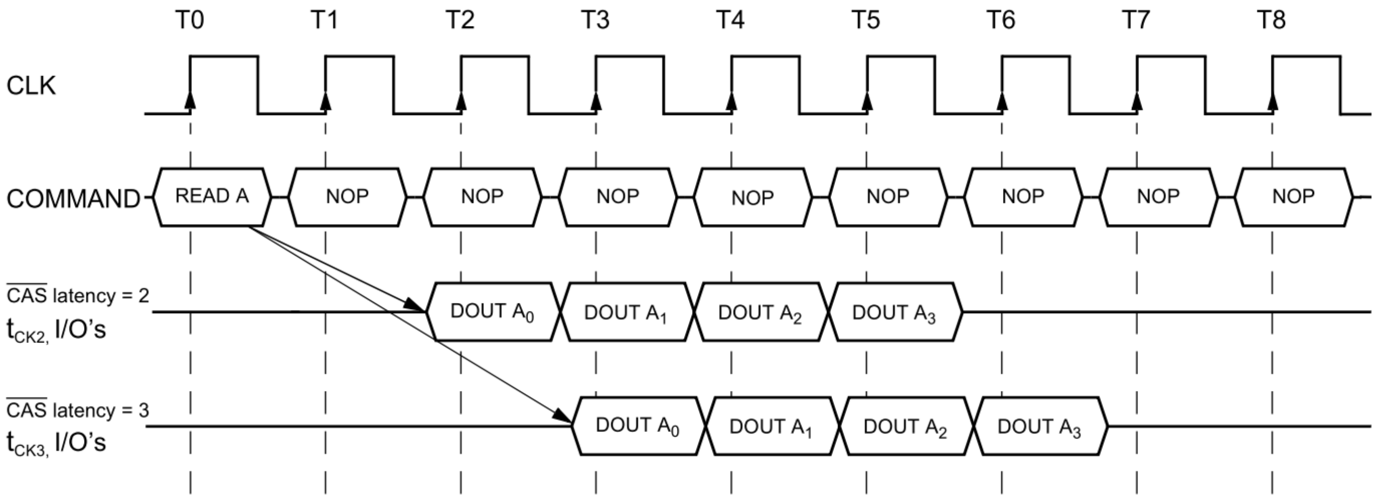
1. Bank Activate Command Cycle

($\overline{CAS}$ latency = 3)



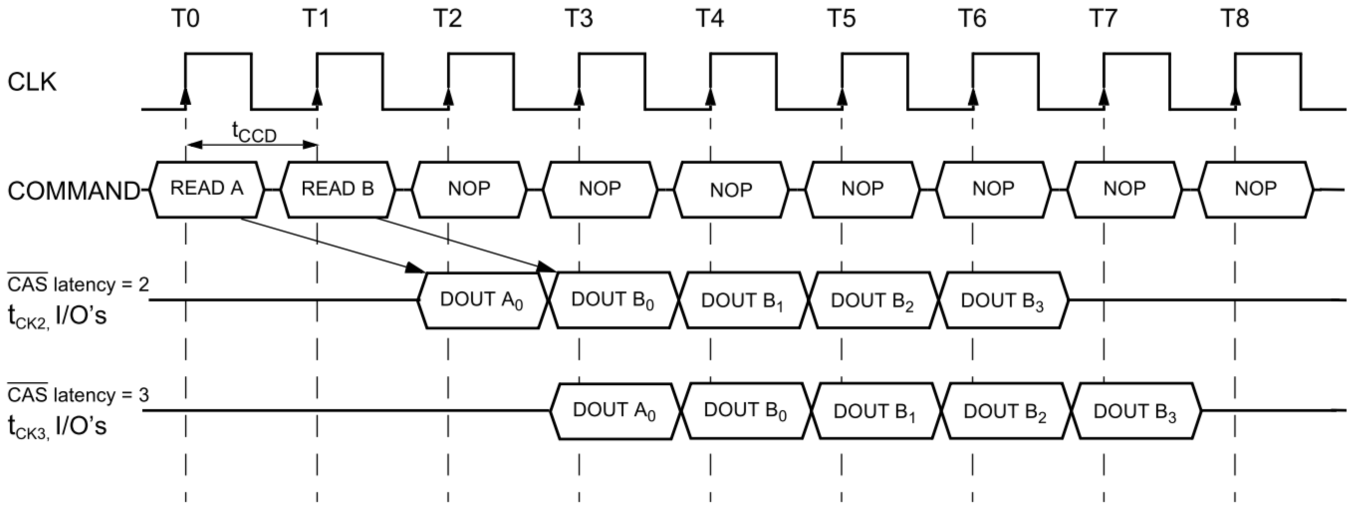
2. Burst Read Operation

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



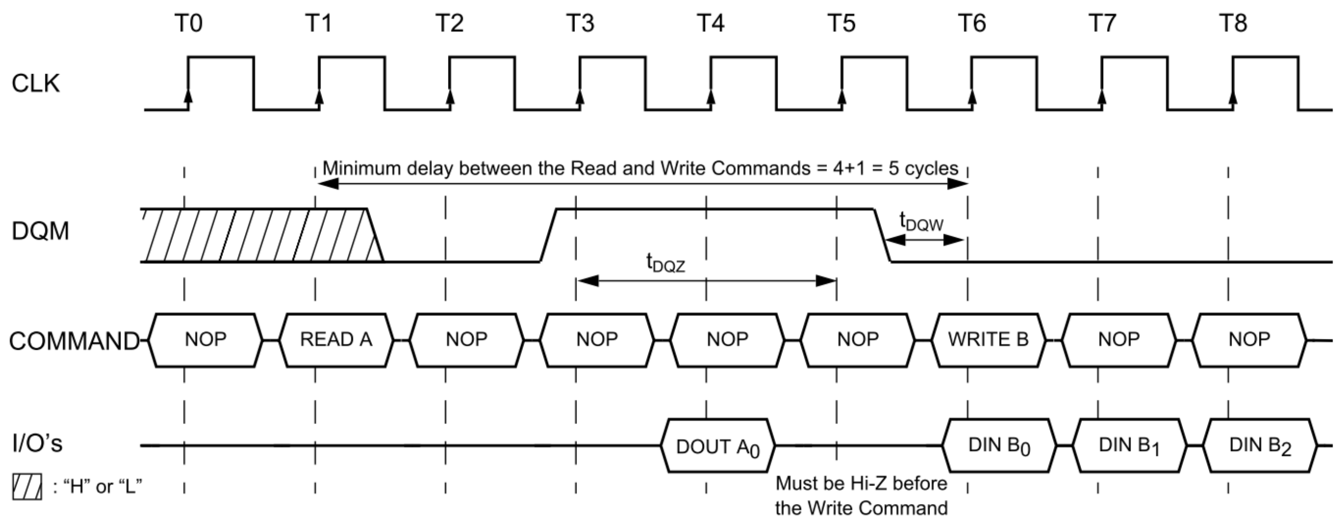
3. Read Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



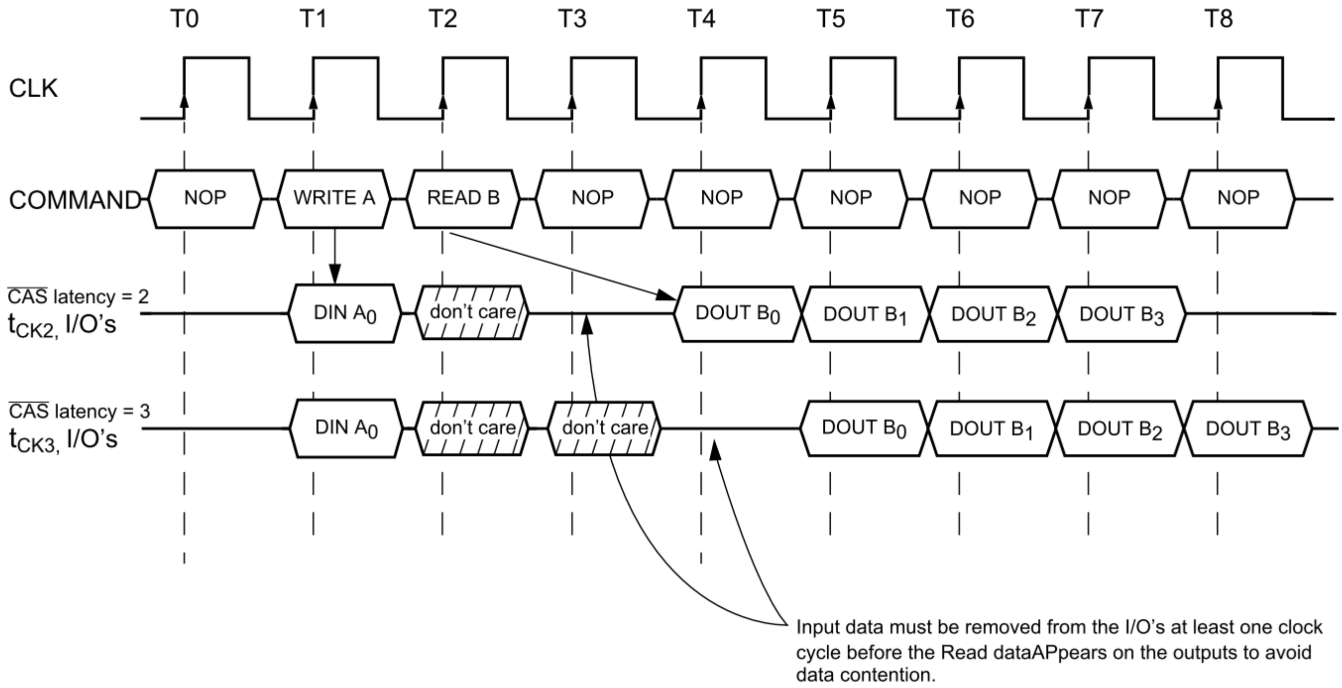
4.1 Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 3)



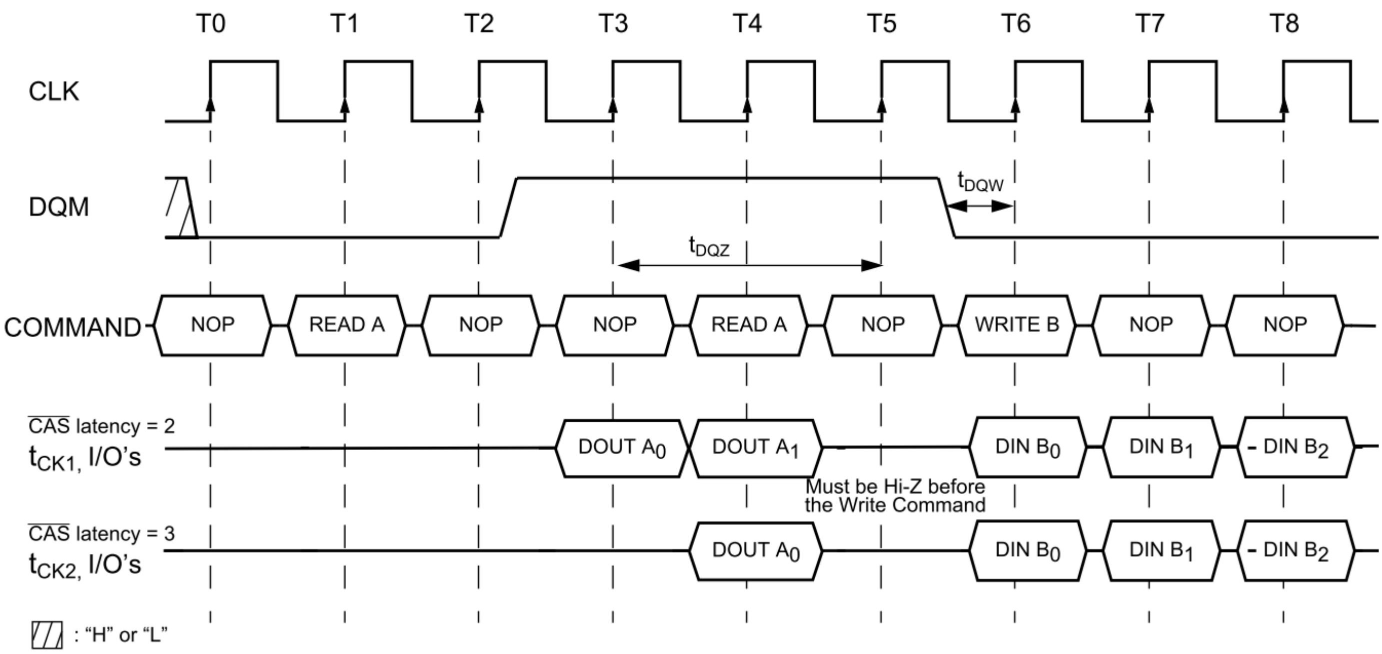
4.2 Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2)



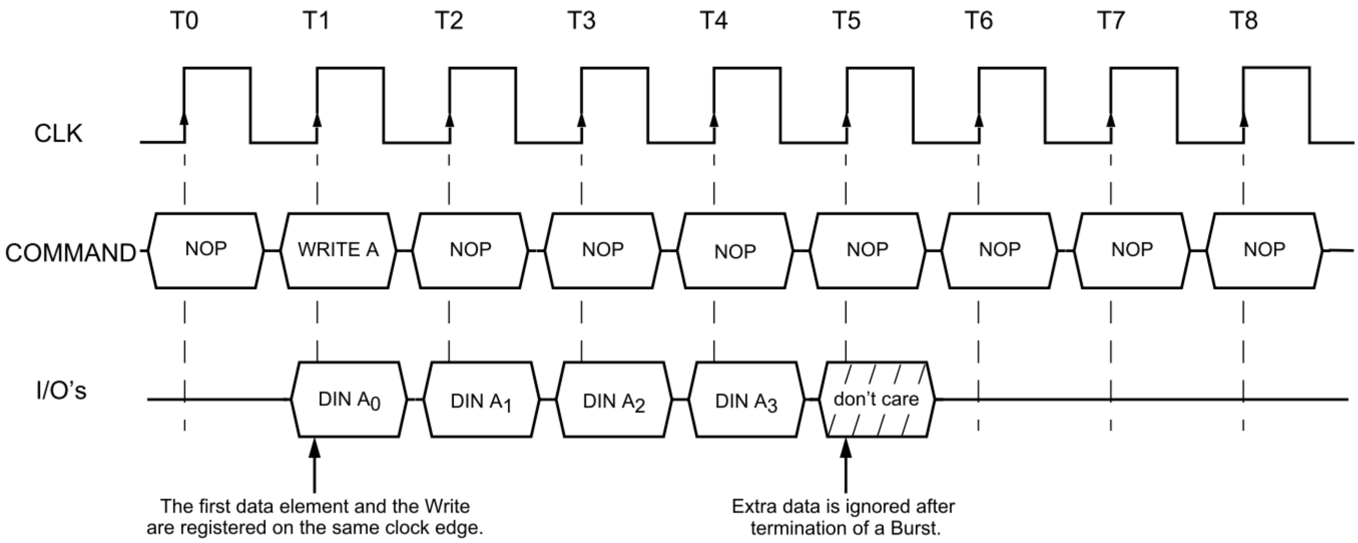
4.3 Non-Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



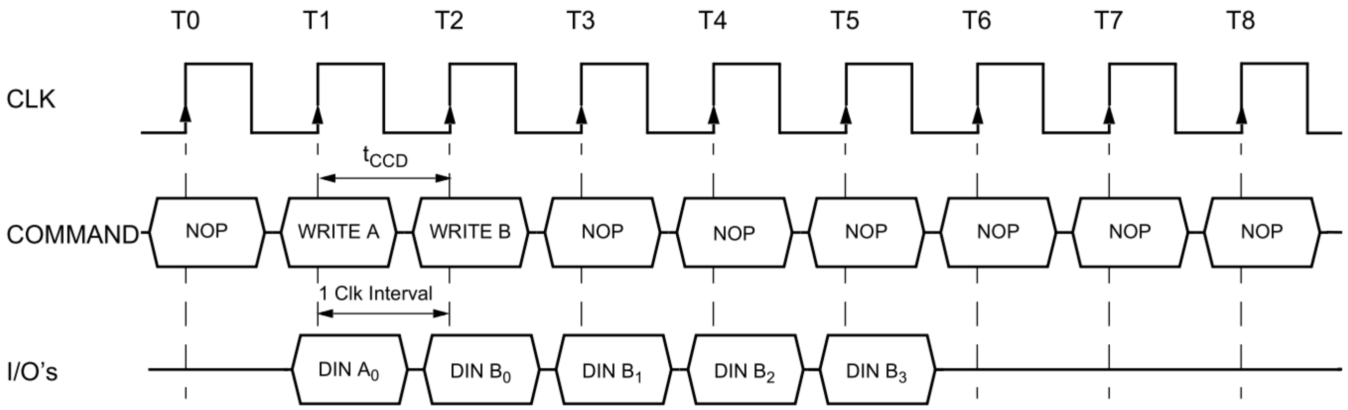
5. Burst Write Operation

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



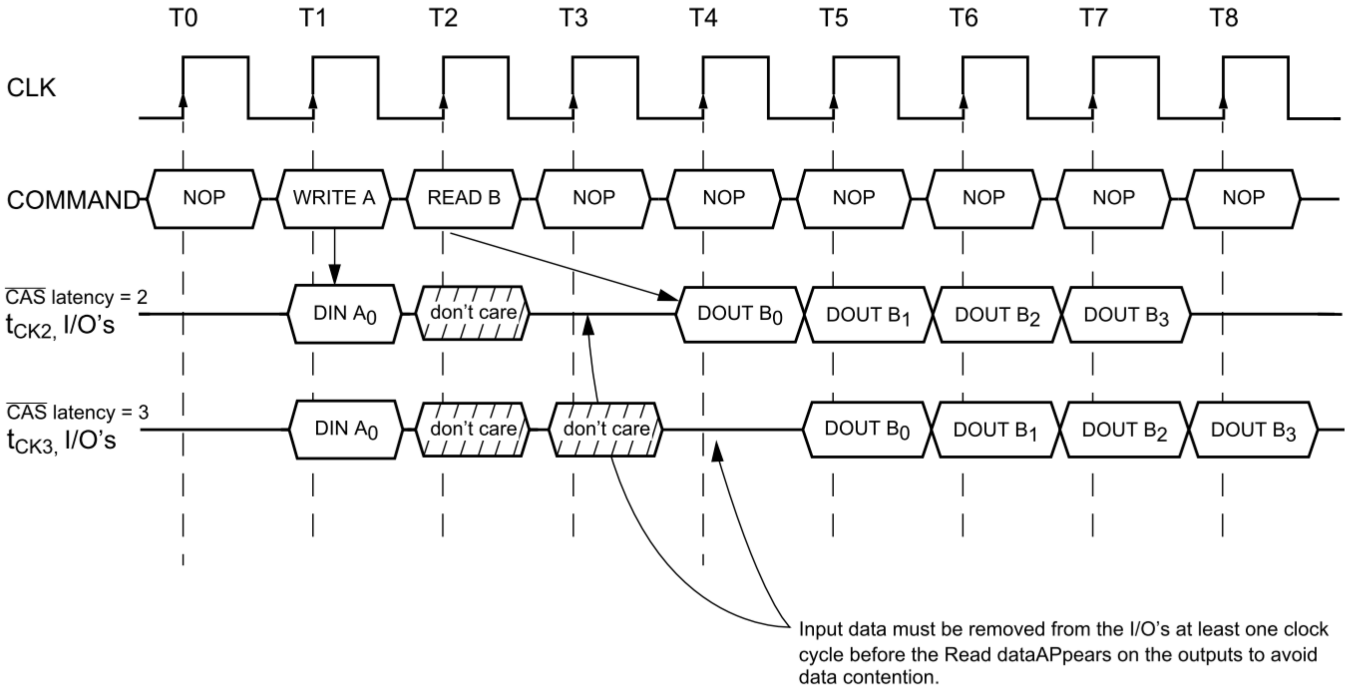
6.1 Write Interrupted by a Write

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



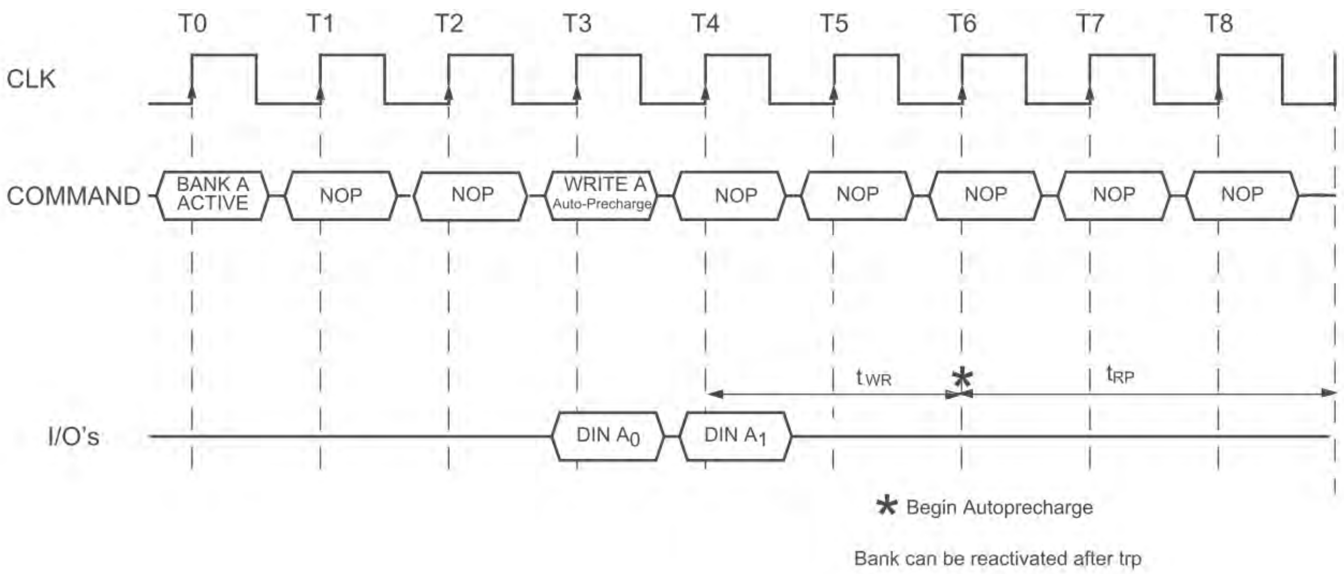
6.2 Write Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



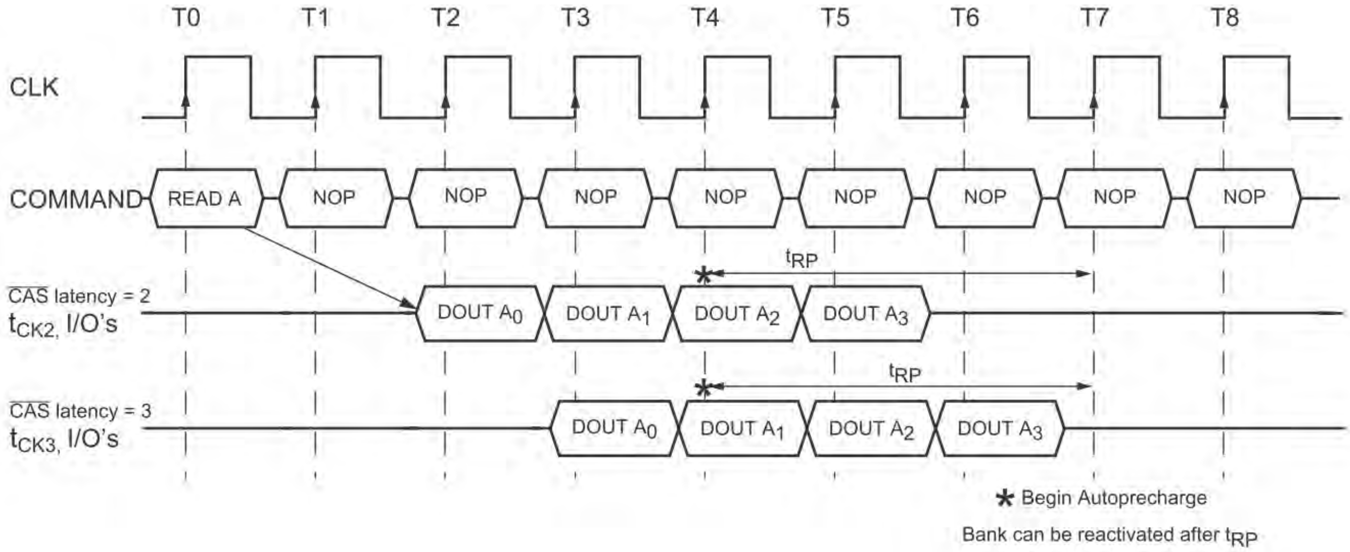
7.1 Burst Write with Auto-Precharge

Burst Length = 2, $\overline{CAS}$ latency = 2, 3)



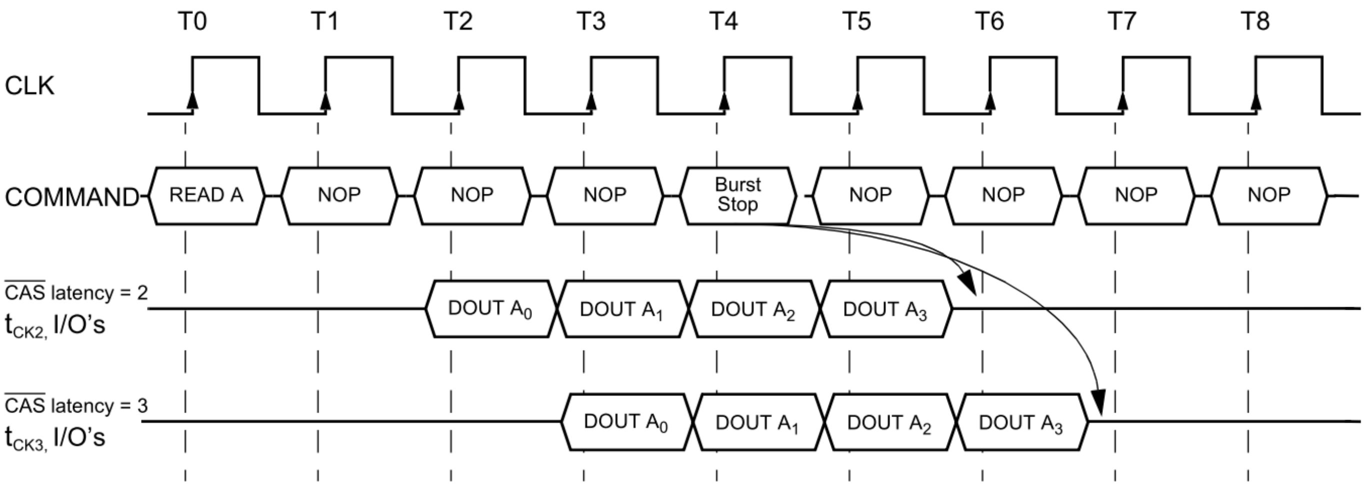
7.2 Burst Read with Auto-Precharge

Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



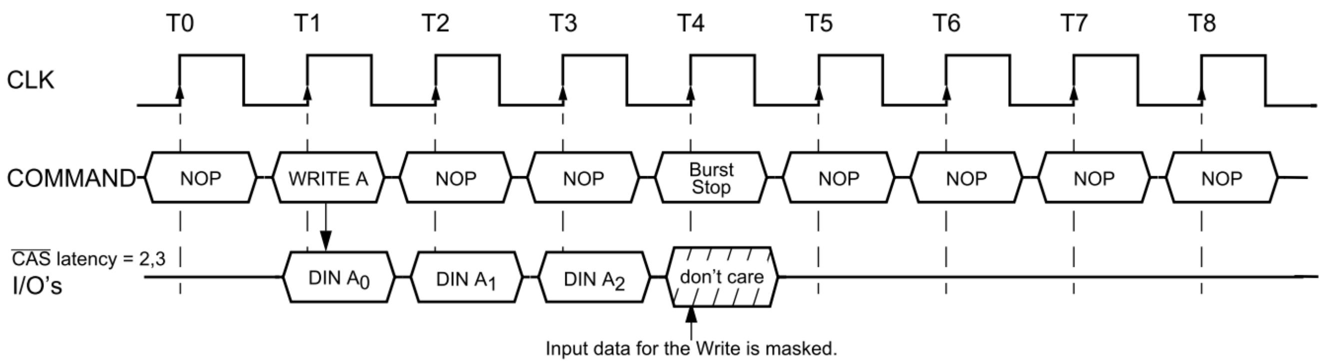
8.1 Termination of a Burst Read Operation

($\overline{CAS}$ latency = 2, 3)



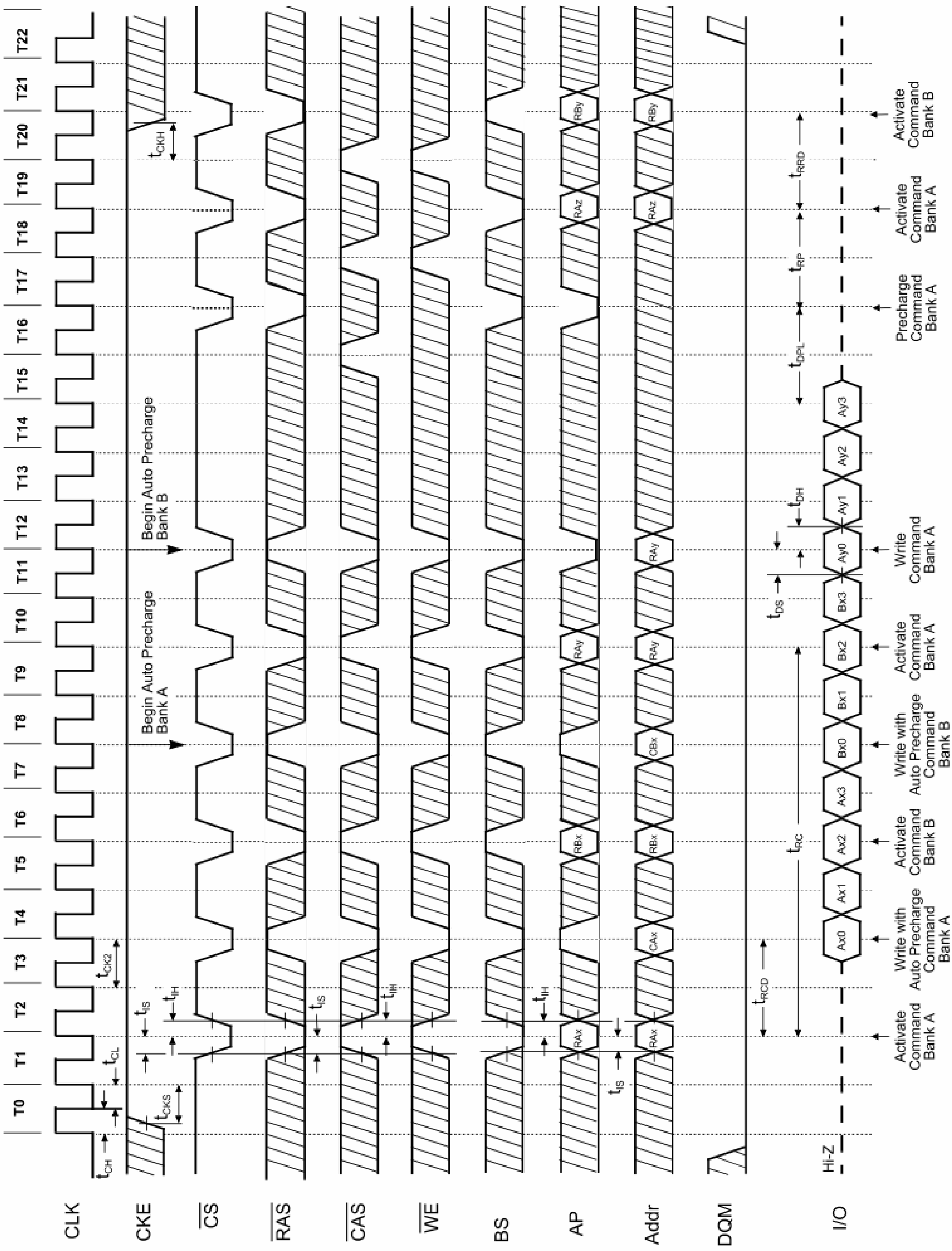
8.2 Termination of a Burst Write Operation

($\overline{CAS}$ latency = 2, 3)



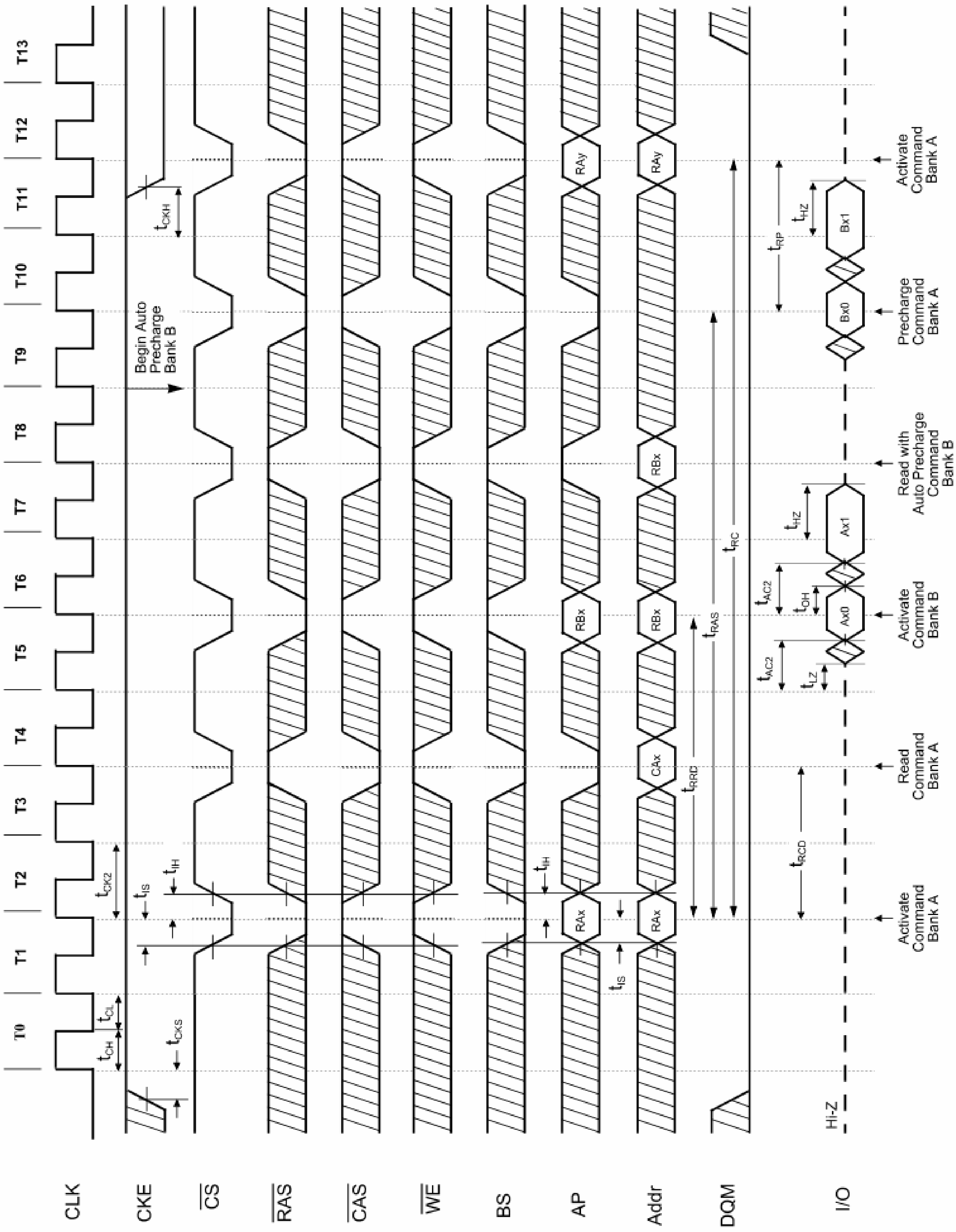
9.1 AC Parameters for Write Timing

Burst Length = 4, $\overline{CAS}$ Latency = 2

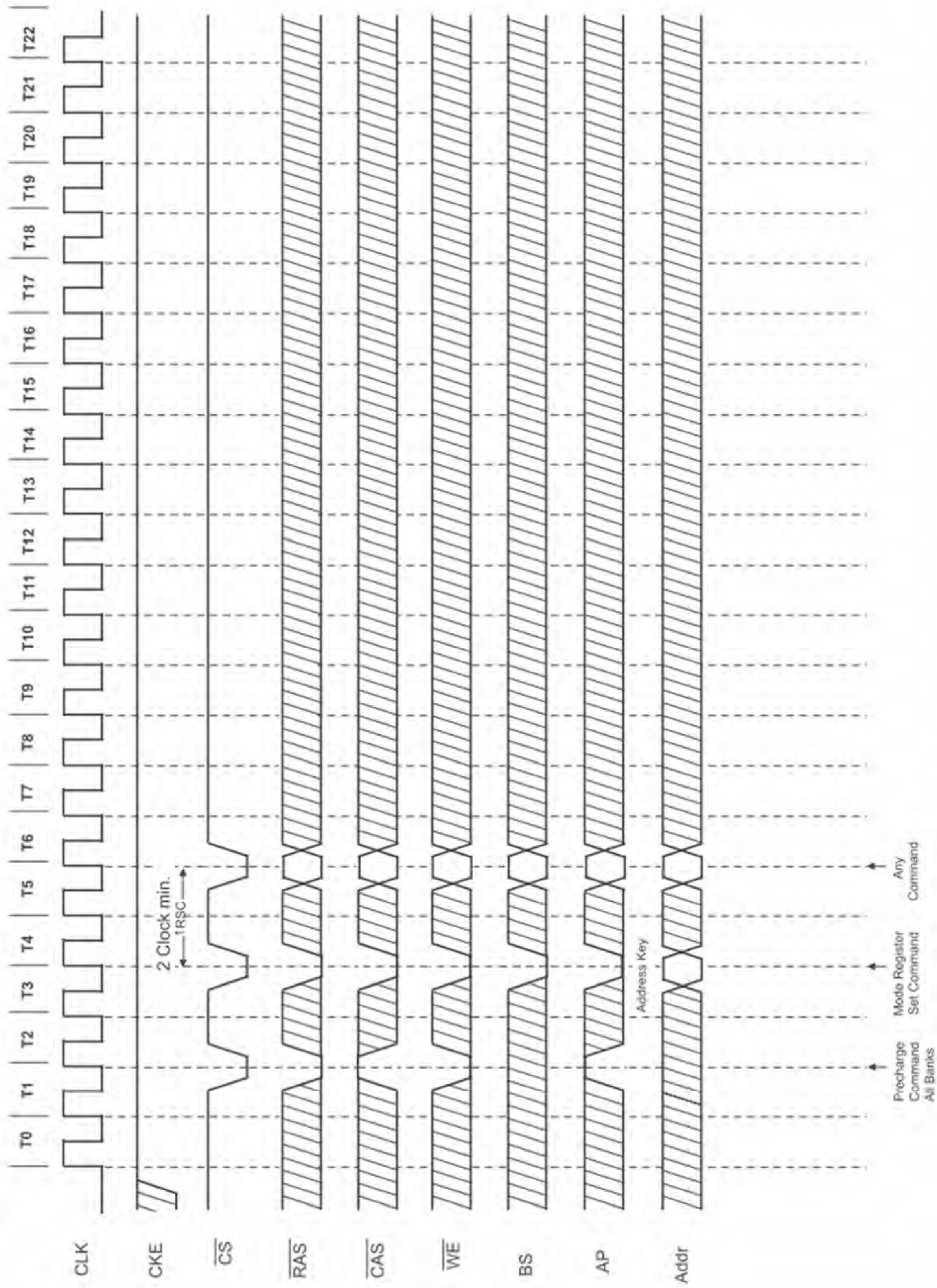


9.2 AC Parameters for Read Timing

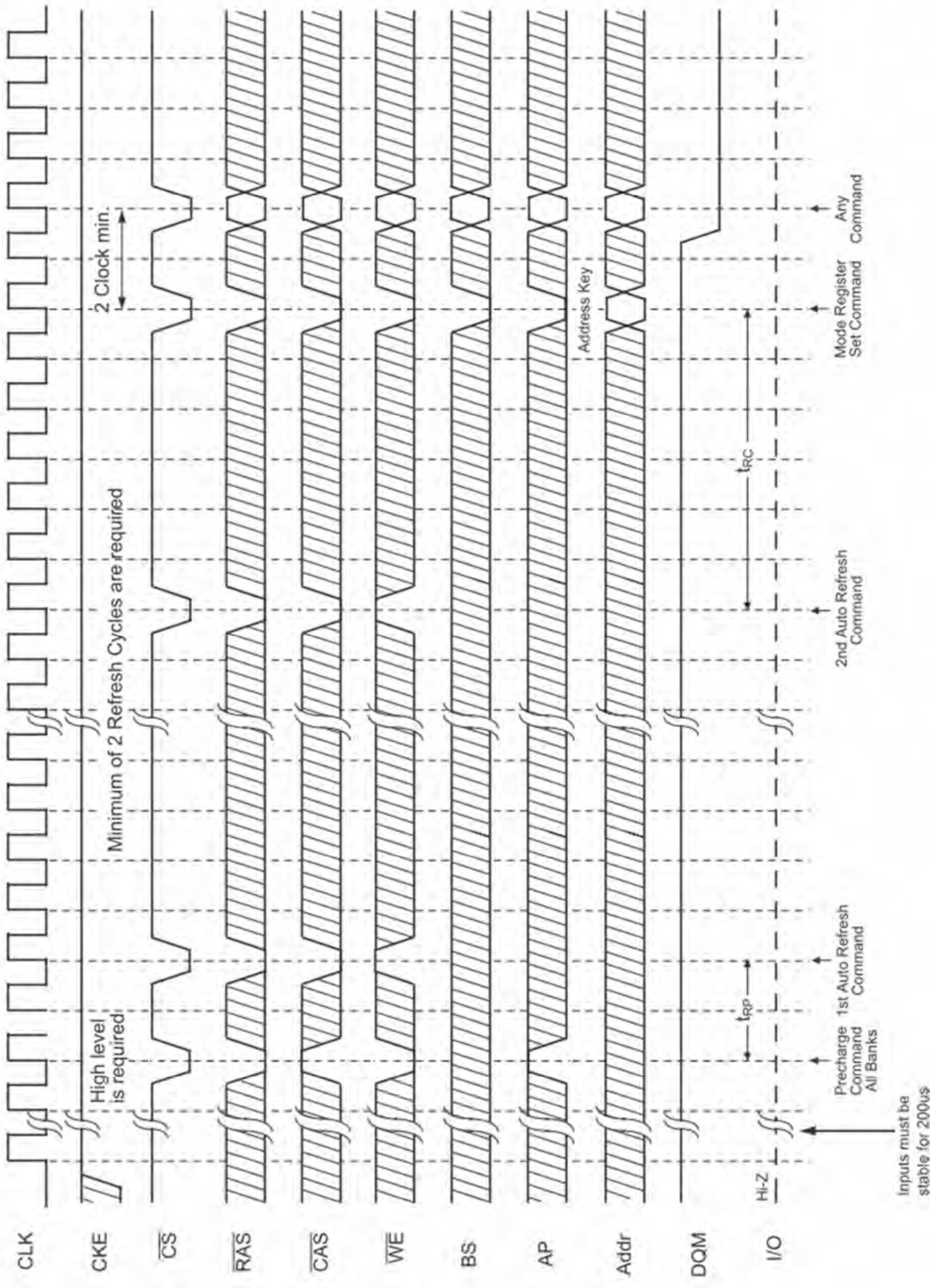
Burst Length = 2, $\overline{CAS}$ Latency = 2



10. Mode Register Set

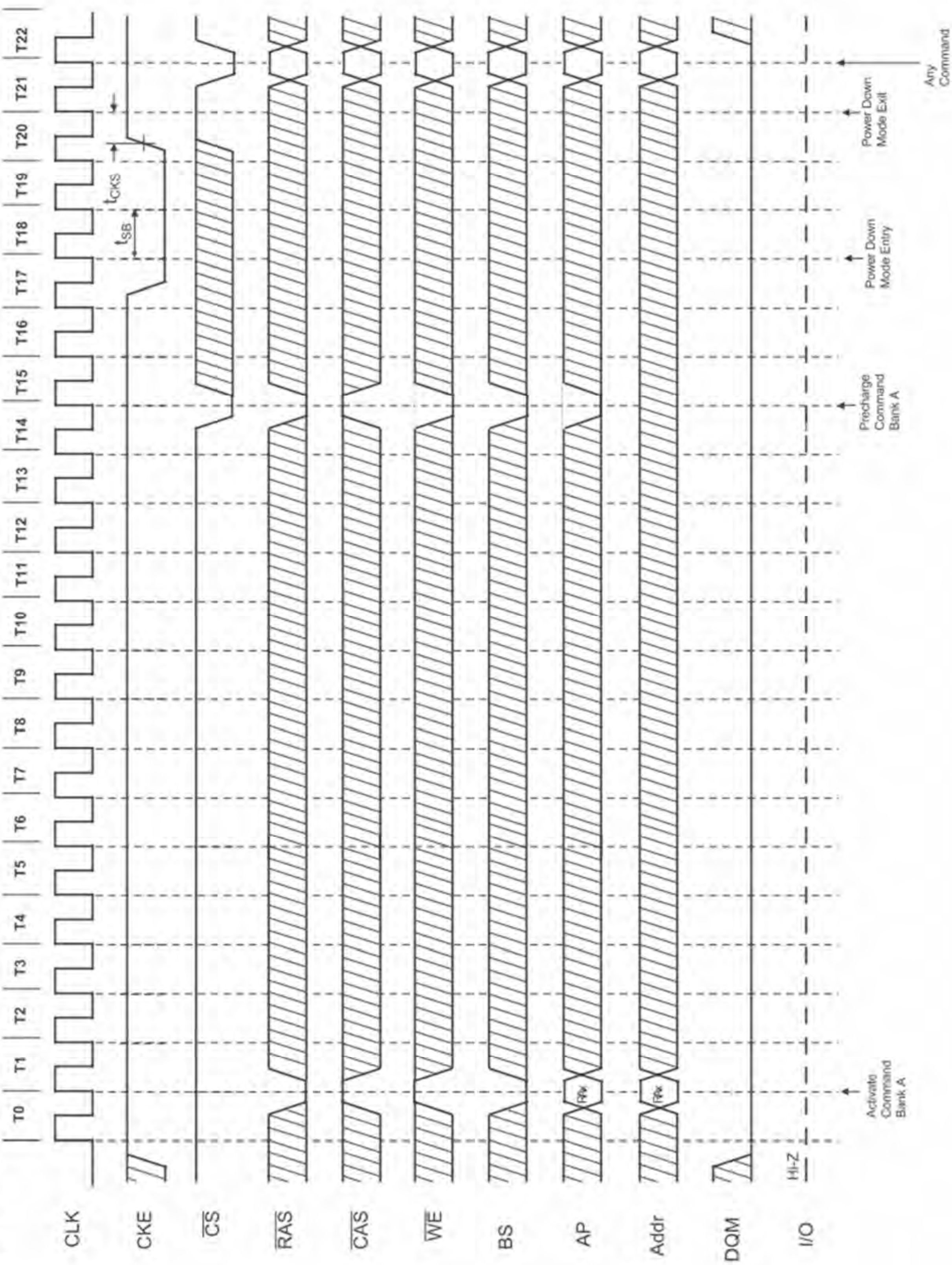


11. Power on Sequence and Auto Refresh (CBR)

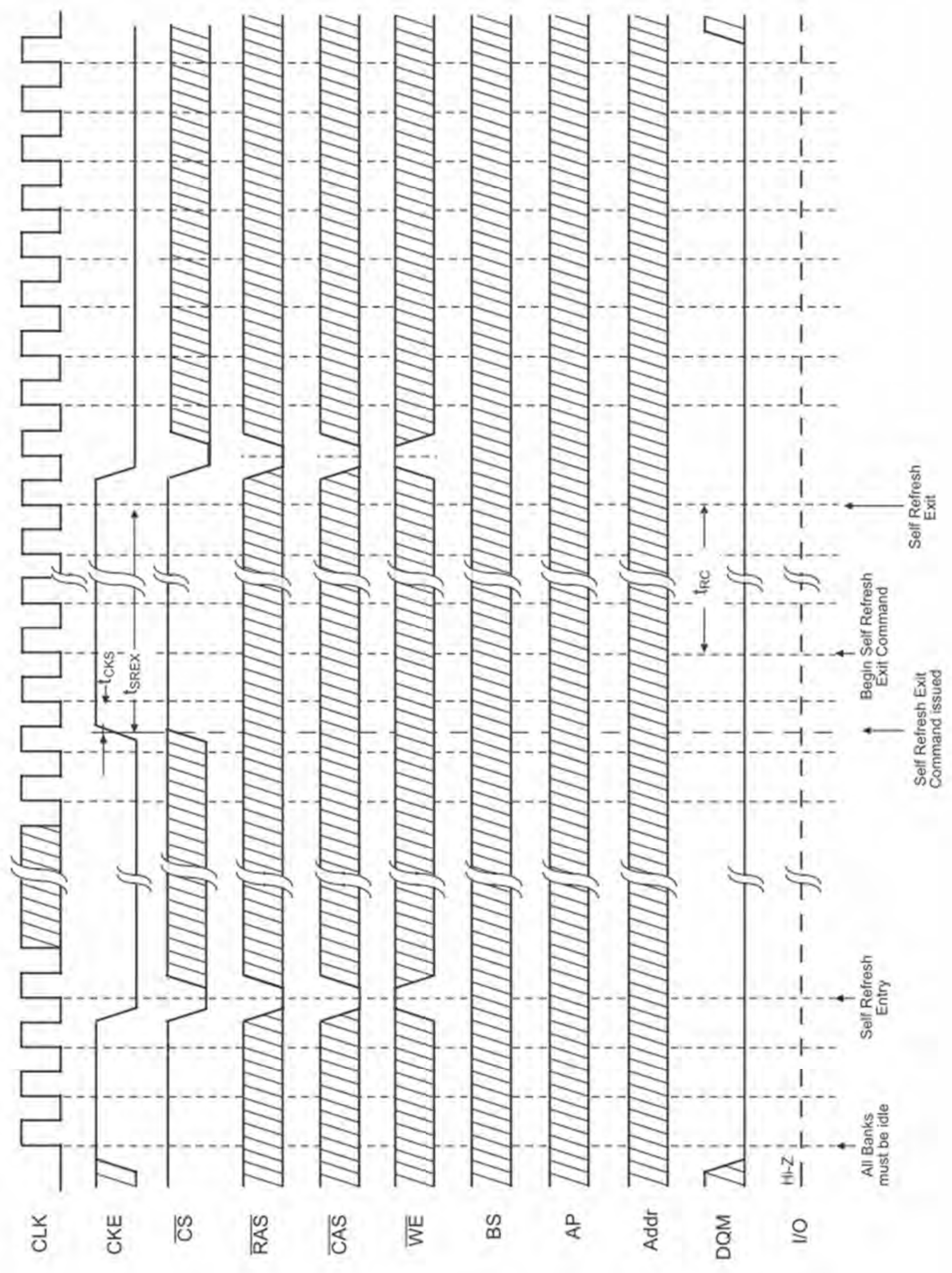


12. Power Down Mode

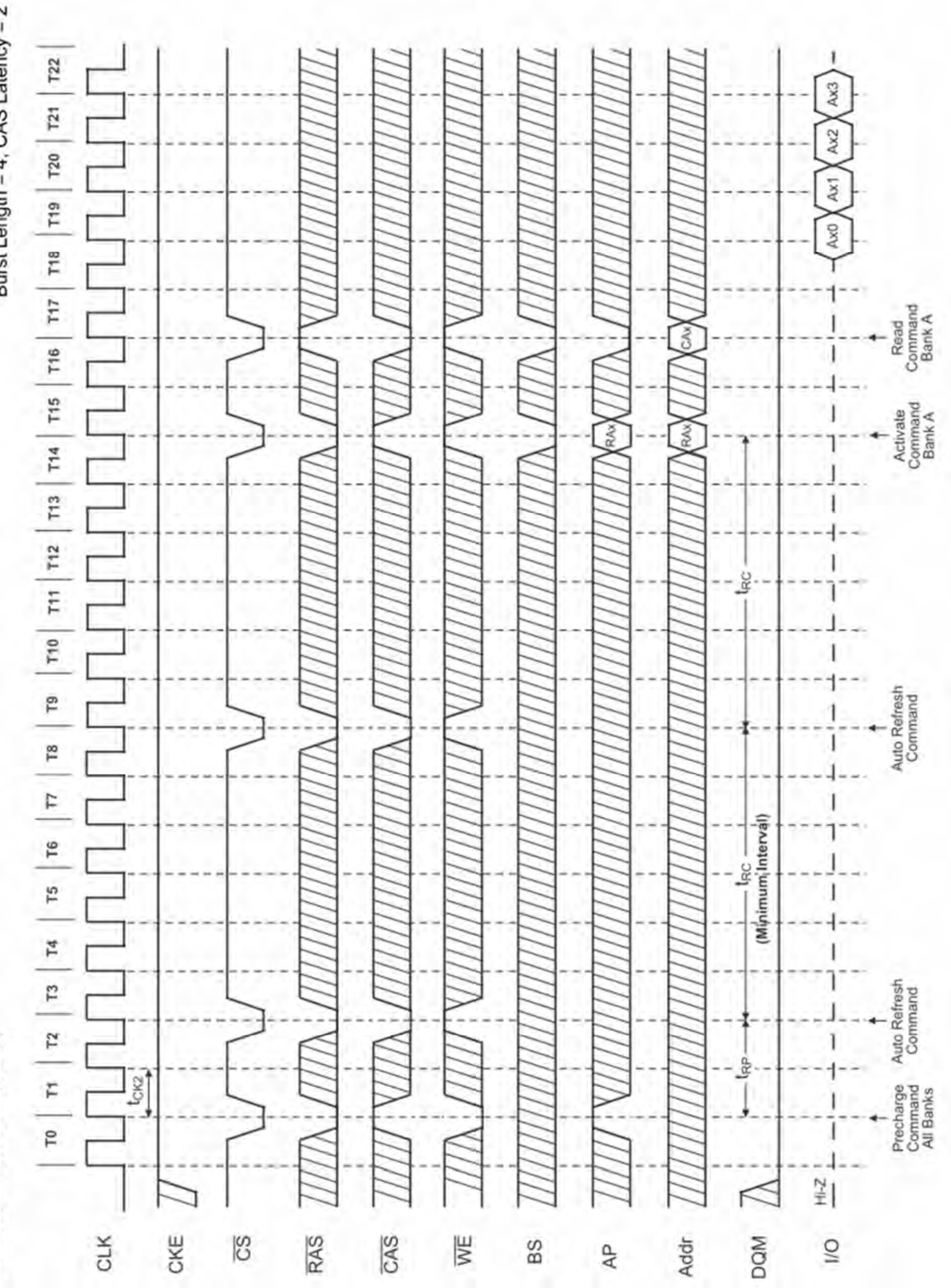
Burst Length = 4, $\overline{CAS}$ Latency = 2



13. Self Refresh (Entry and Exit)

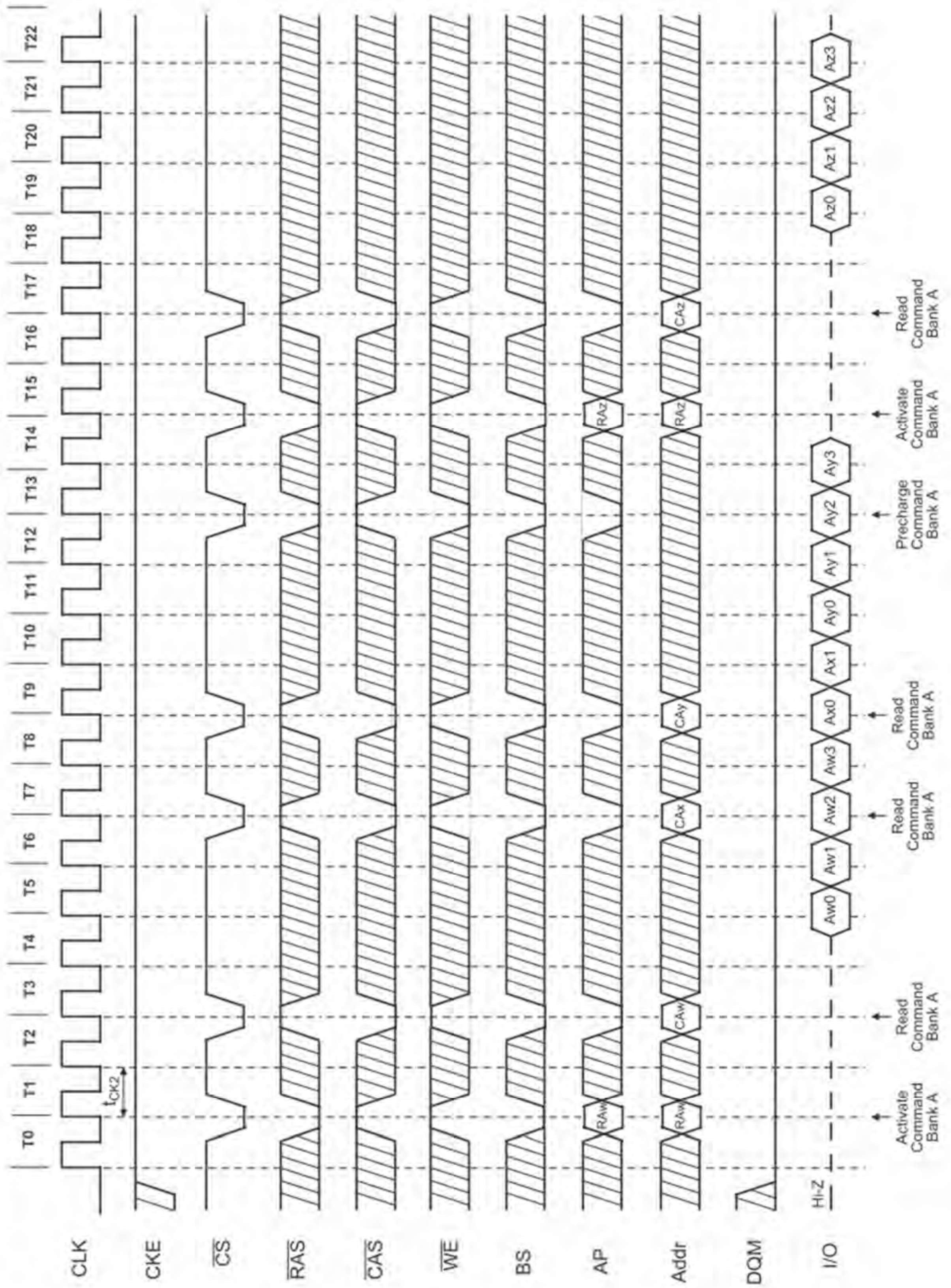


14. Auto Refresh (CBR)



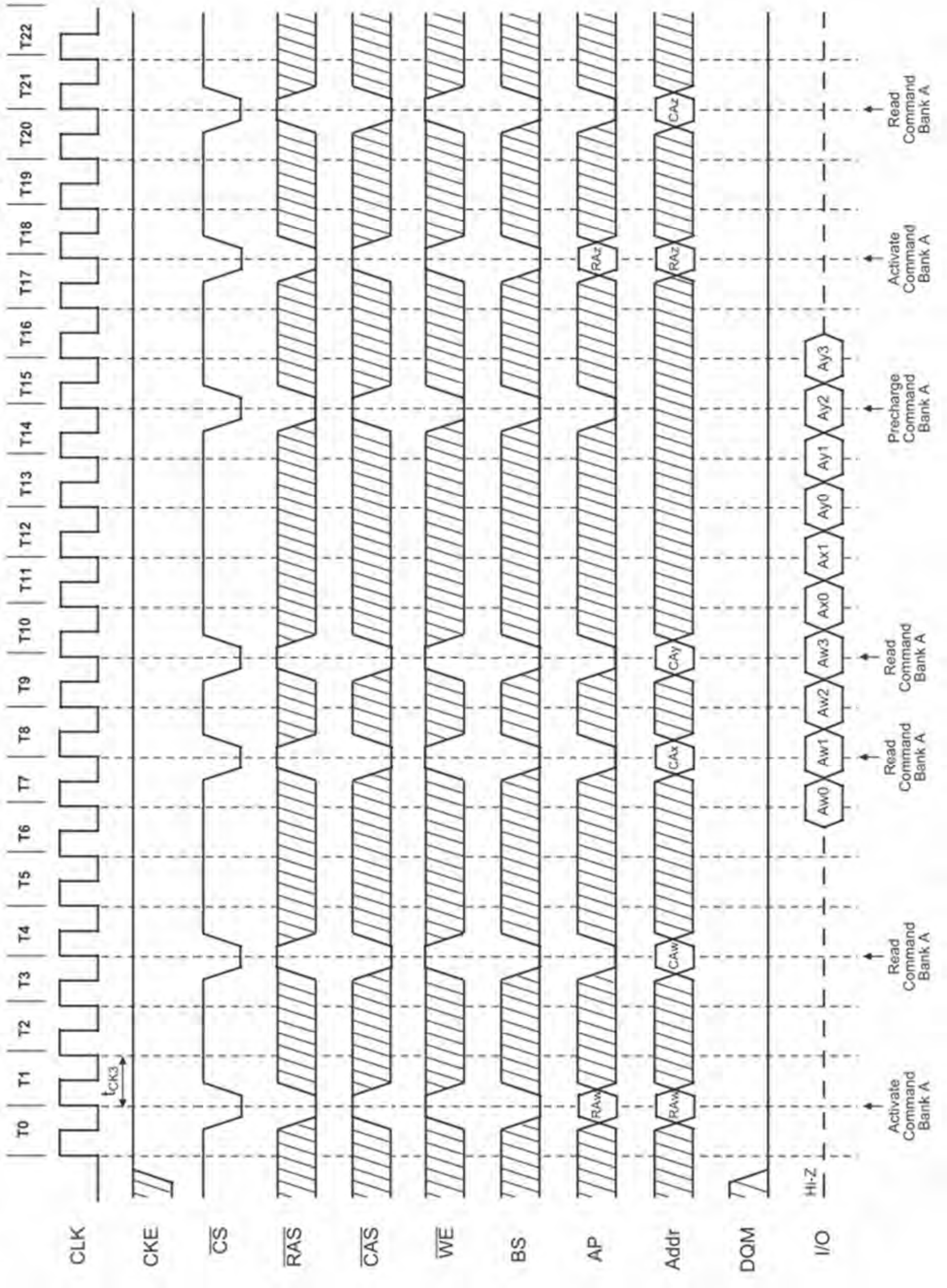
15.1 Random Column Read (Page within same Bank) (1 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 2



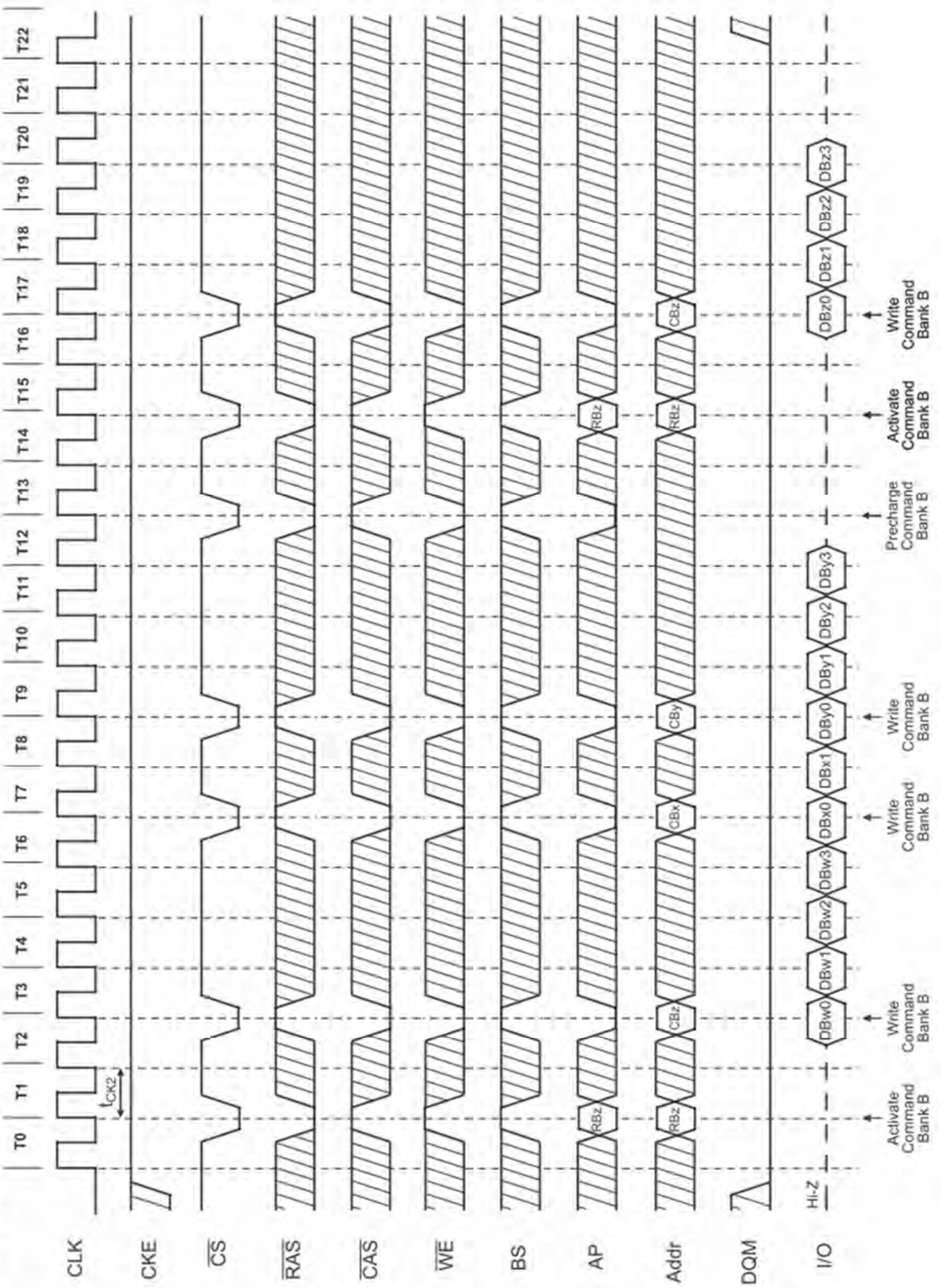
15.2 Random Column Read (Page within same Bank) (2 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 3



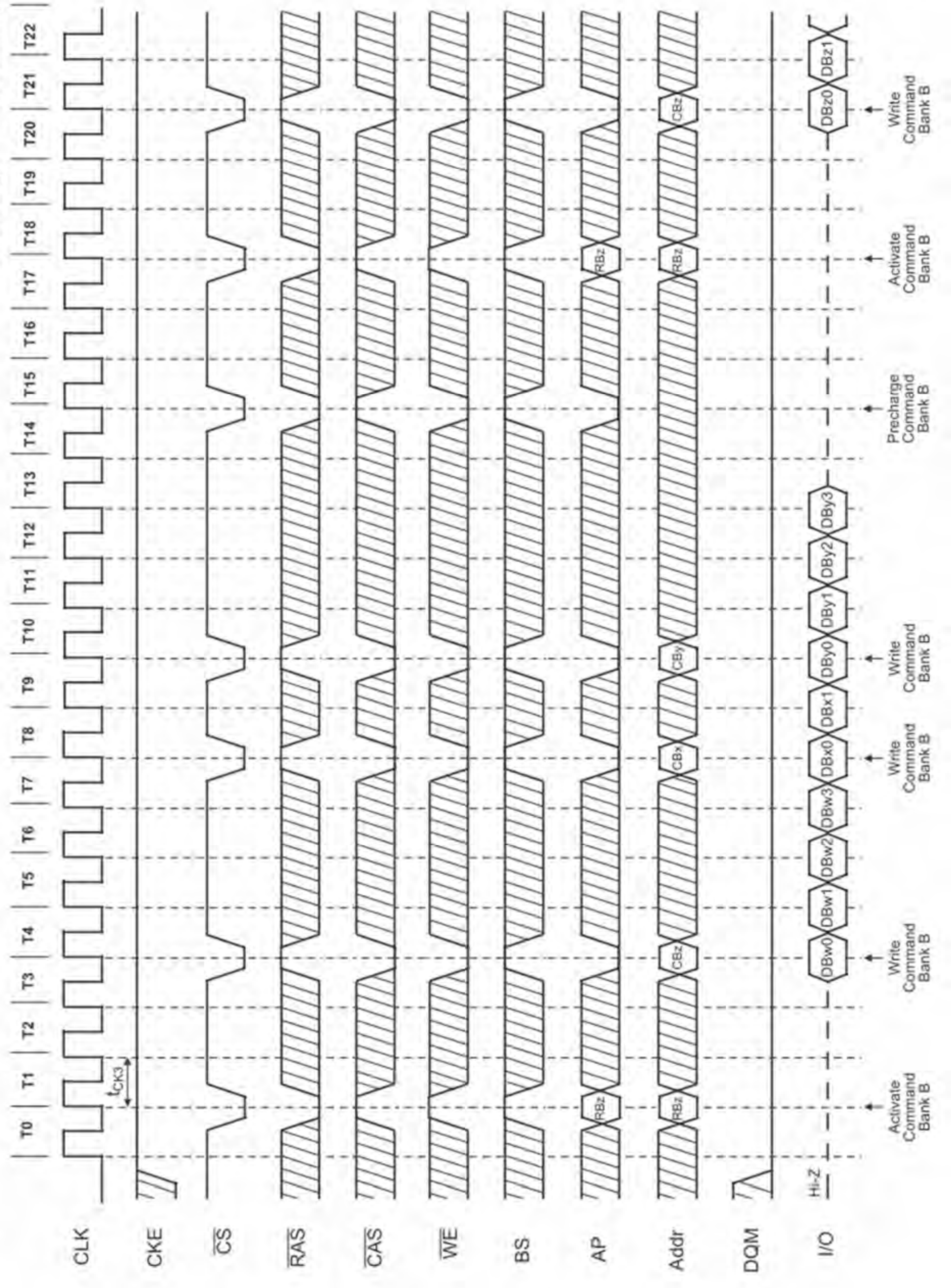
16.1 Random Column Write (Page within same Bank) (1 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 2



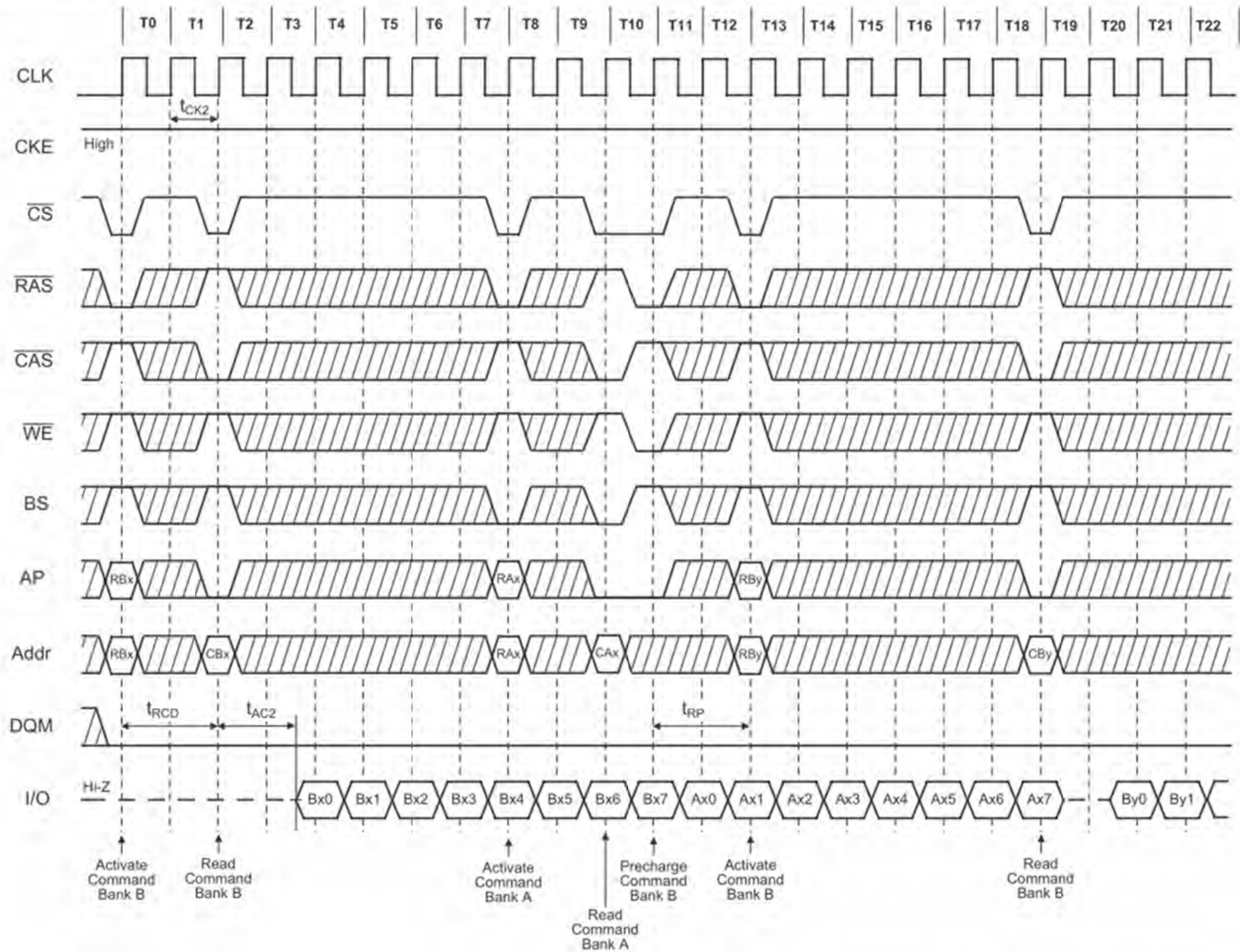
16.2 Random Column Write (Page within same Bank) (2 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 3



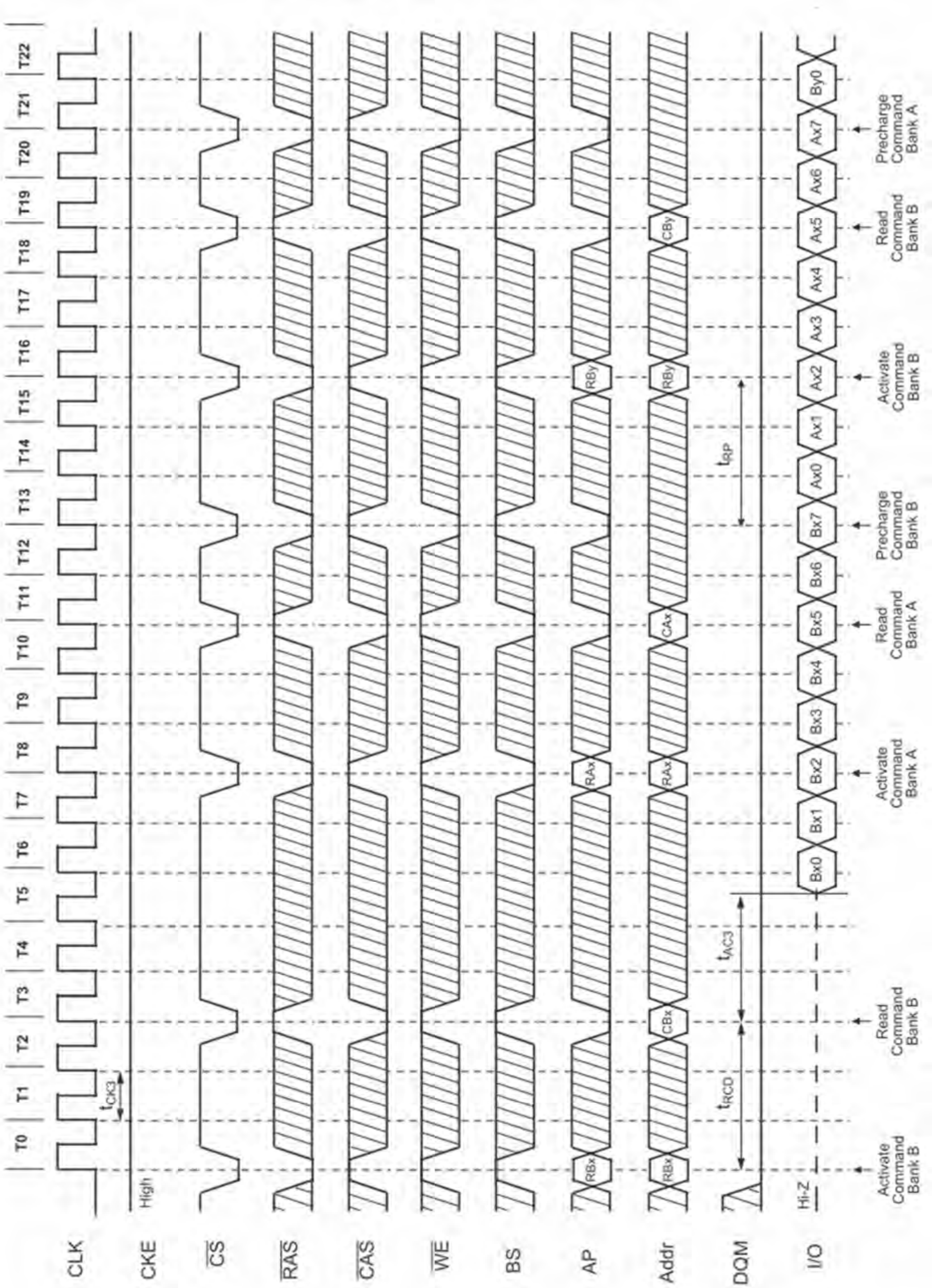
17.1 Random Row Read (Interleaving Banks) (1 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 2



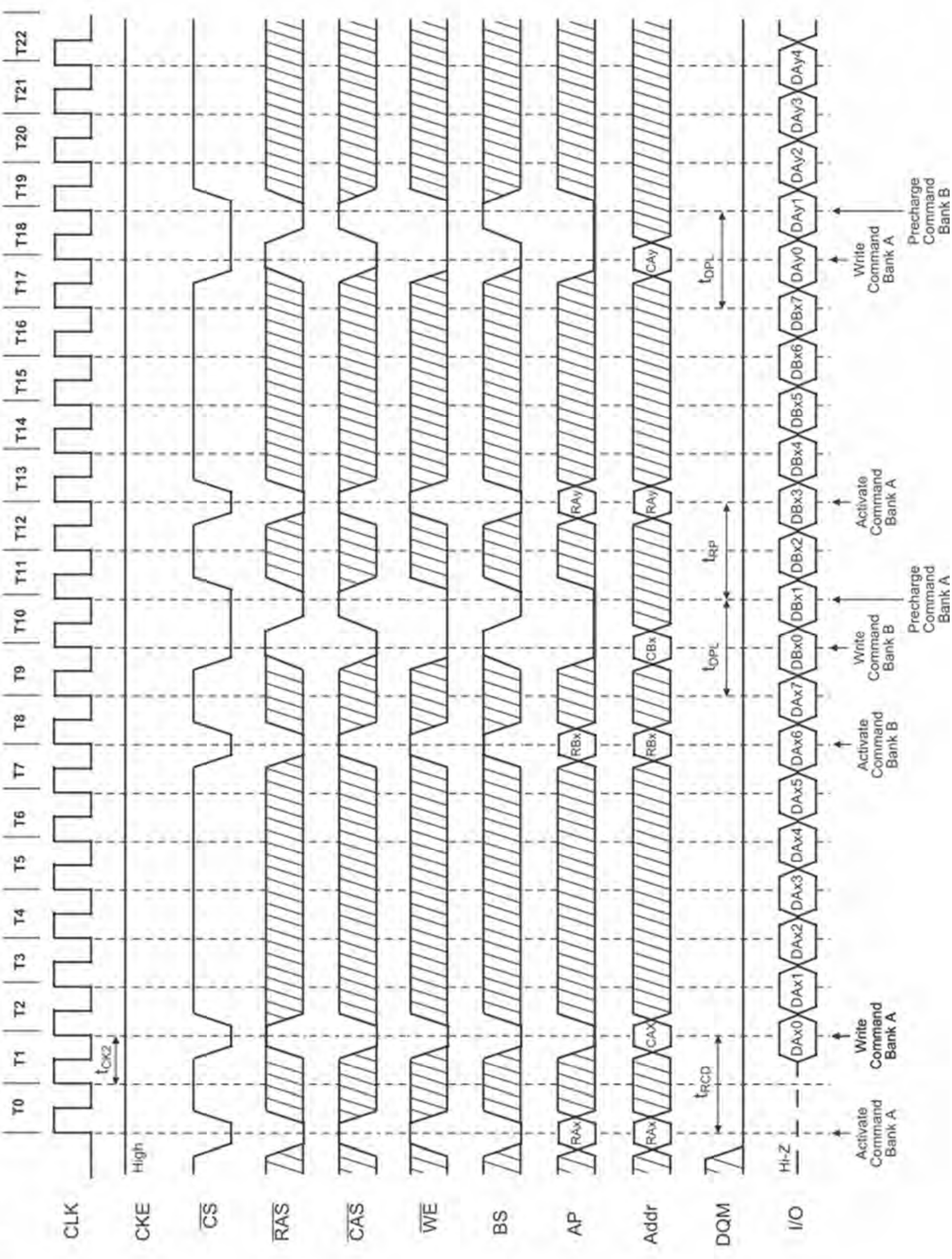
17.2 Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3



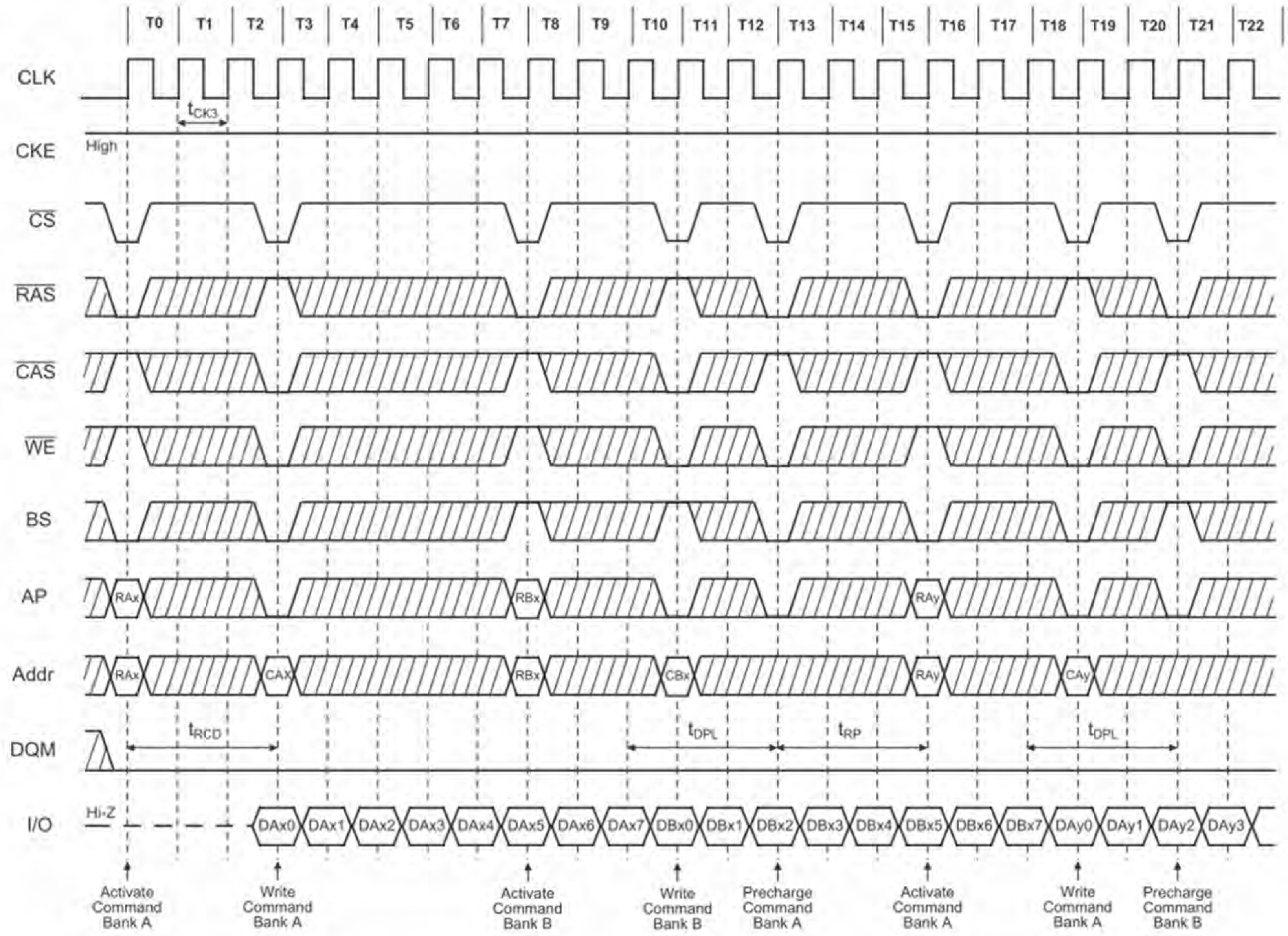
18.1 Random Row Write (Interleaving Banks) (1 of 2)

Burst Length = 8, CAS Latency = 2



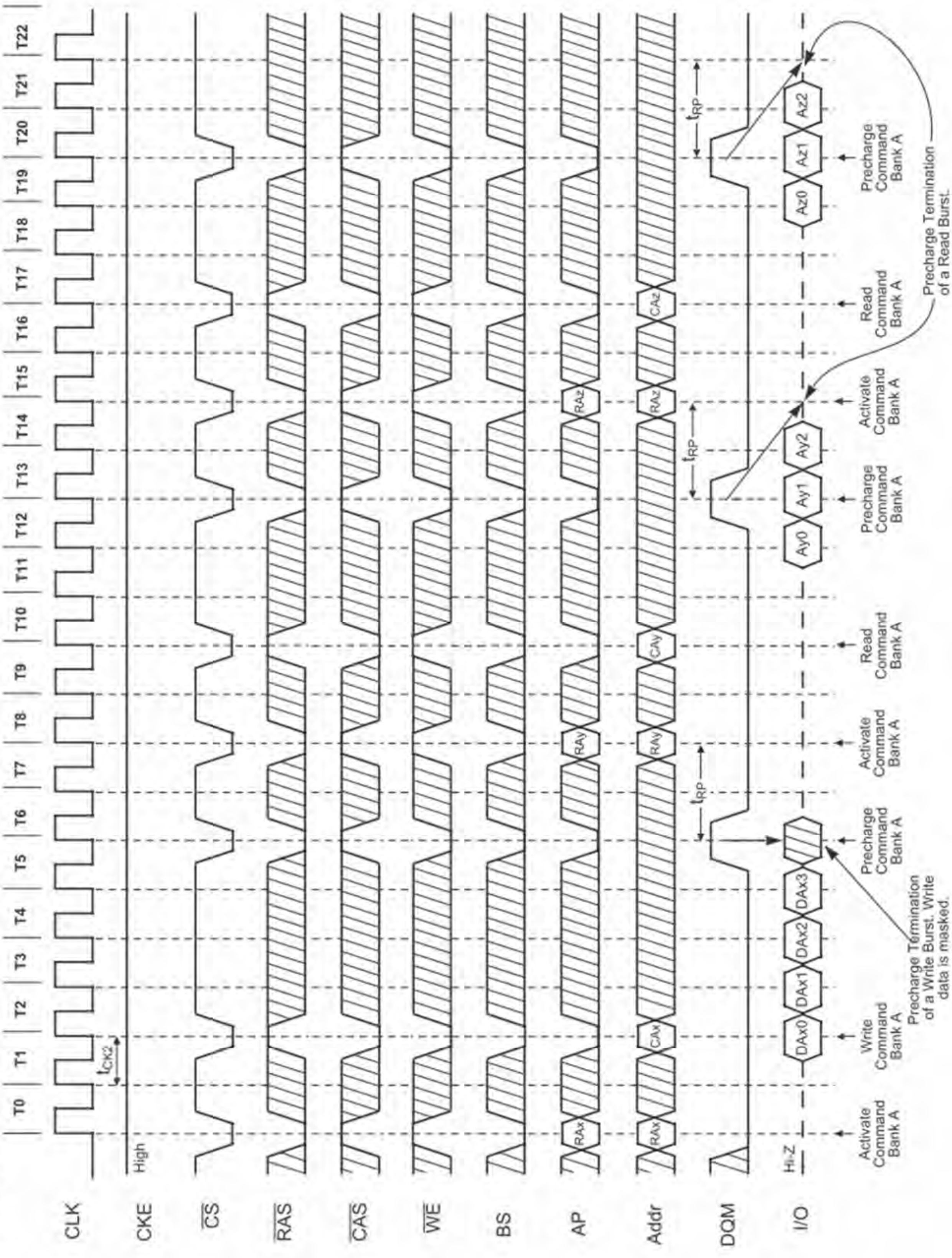
18.2 Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3



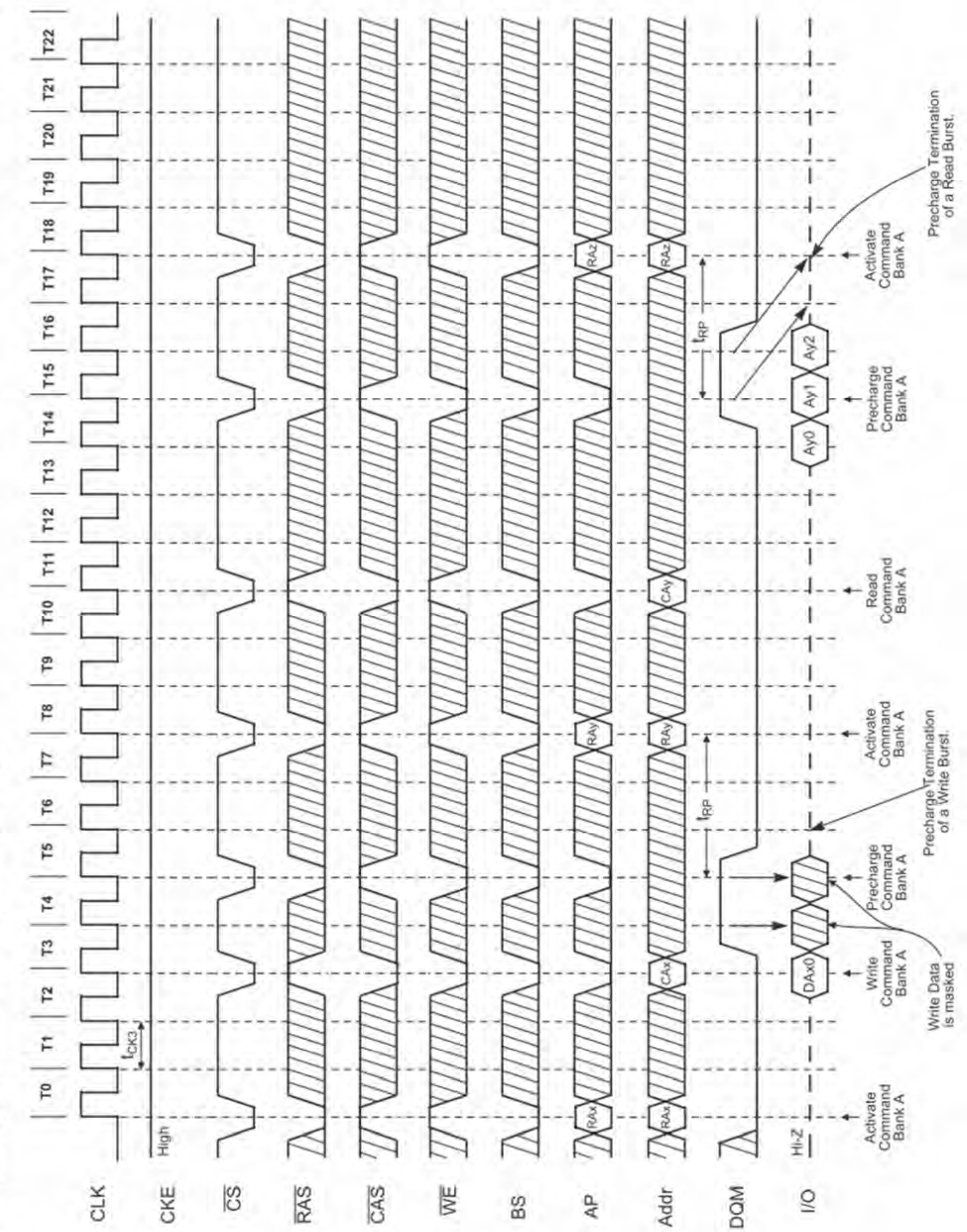
19.1 Precharge Termination of a Burst (1 of 2)

Burst Length = 8, CAS Latency = 2



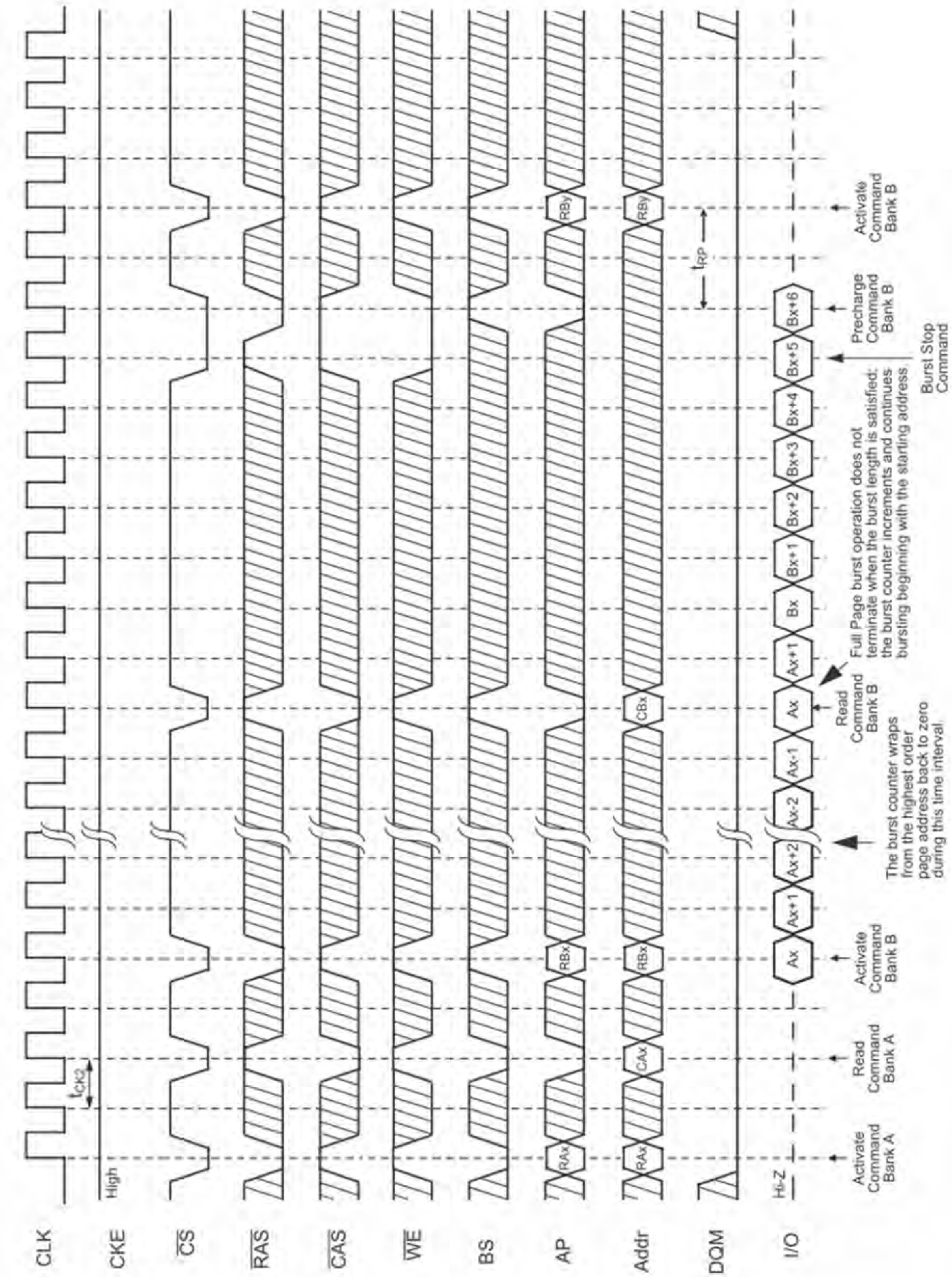
19.2 Precharge Termination of a Burst (2 of 2)

Burst Length = 4, 8, $\overline{CAS}$ Latency = 3



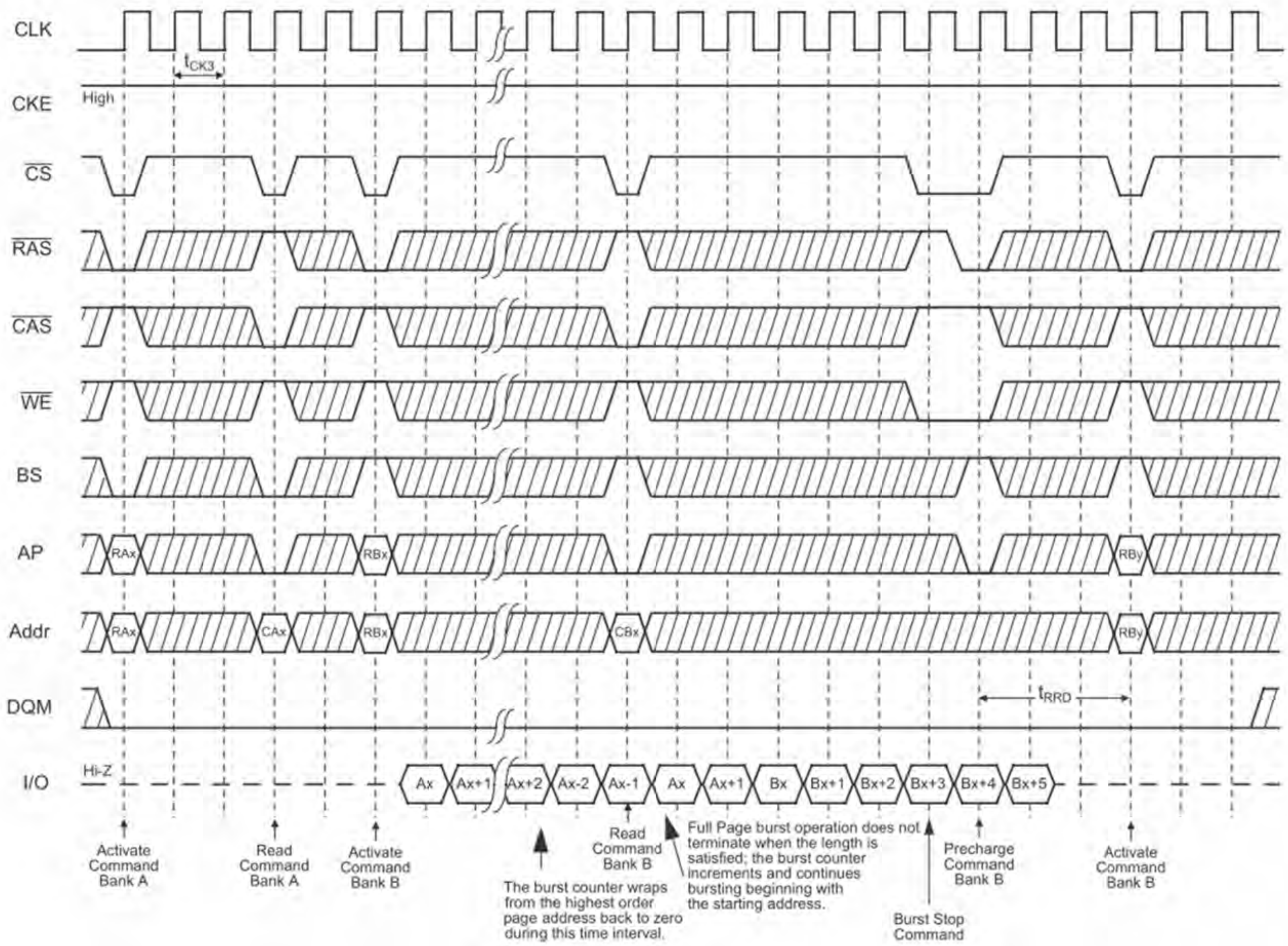
20.1 Full Page Read Cycle (1 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 2



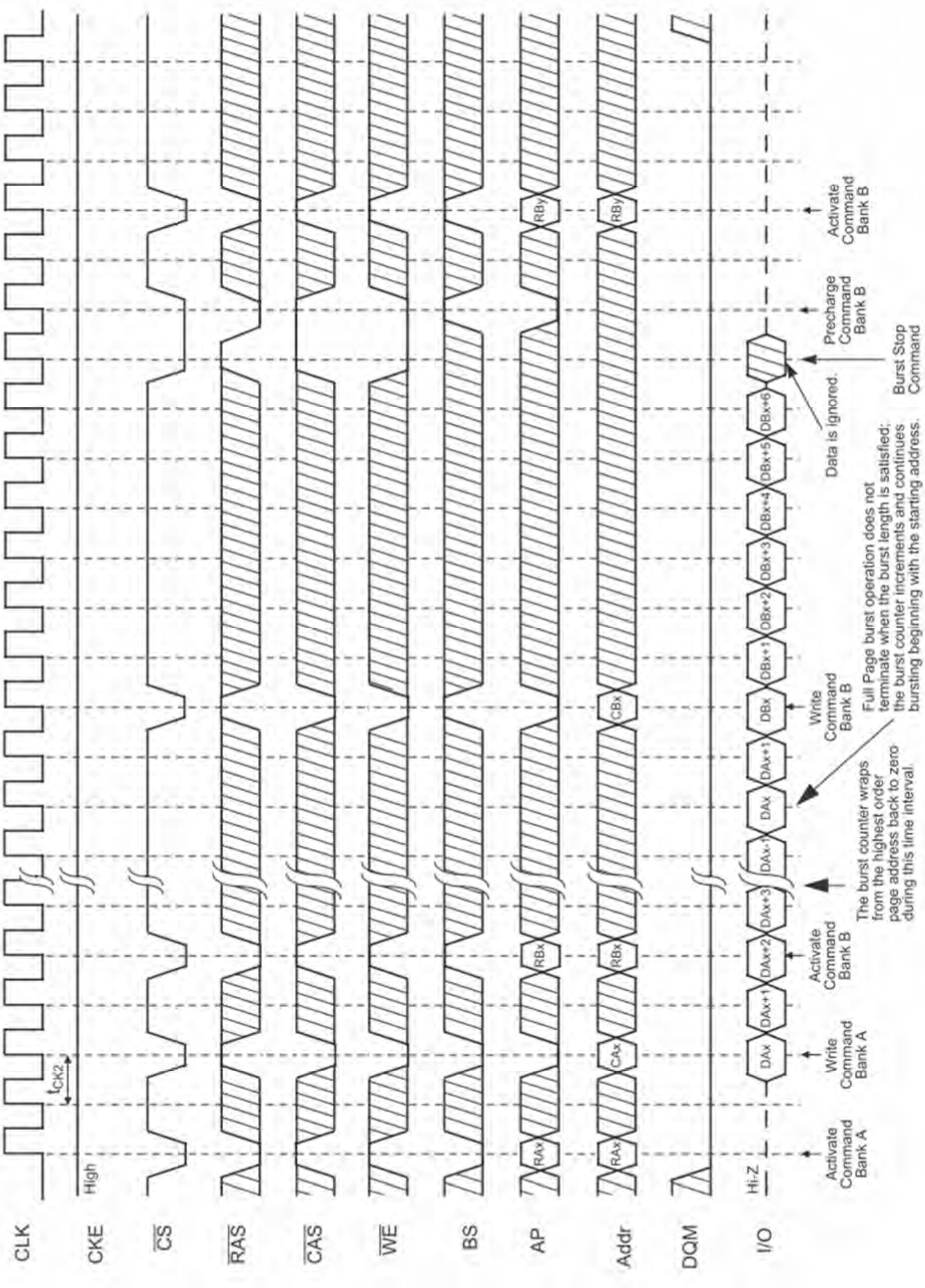
20.2 Full Page Read Cycle (2 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 3



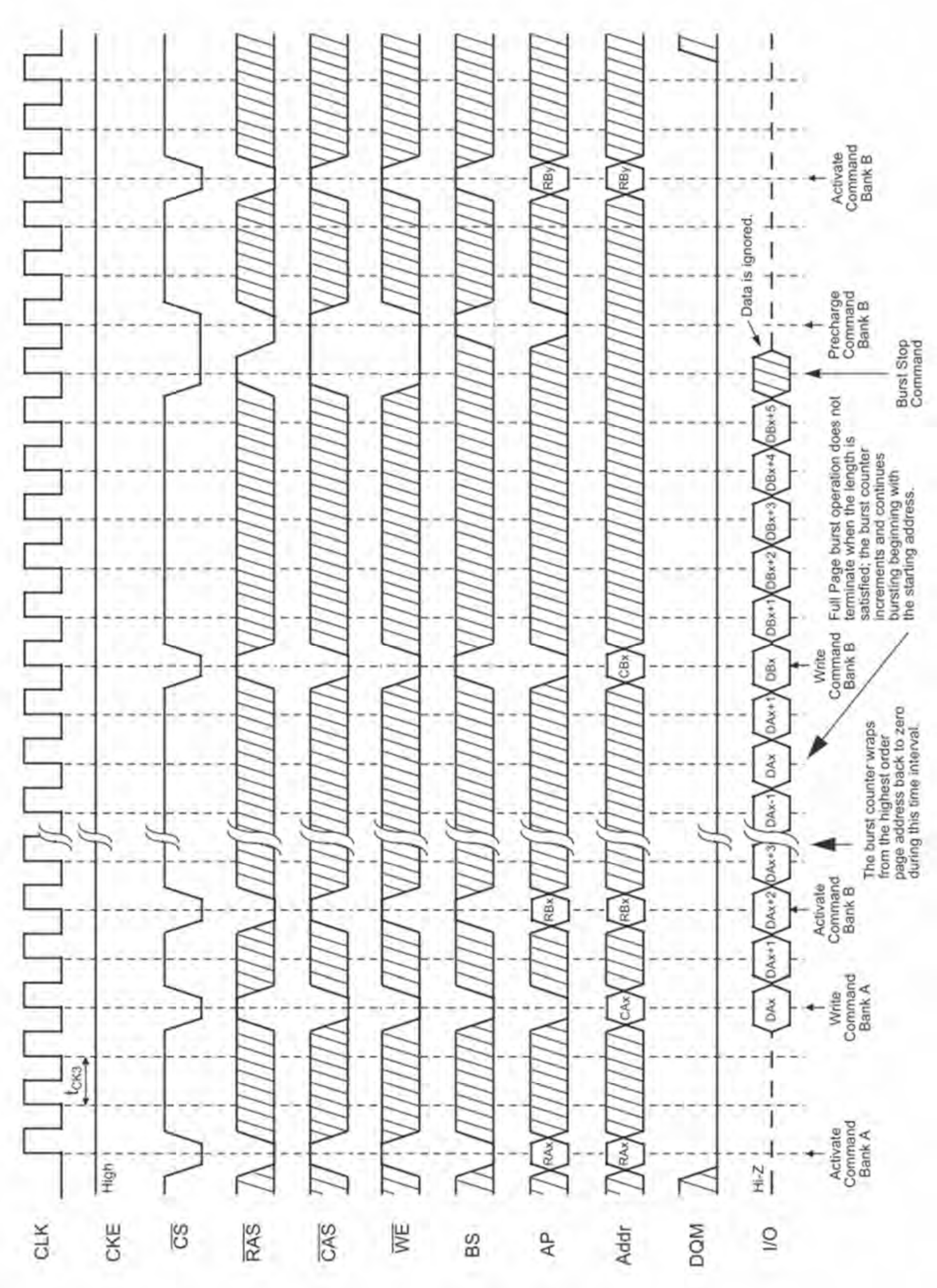
21.1 Full Page Write Cycle (1 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 2



21.2 Full Page Write Cycle (2 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 3



Complete List of Operation Commands

SDRAM Function Truth Table

CURRENT STATE[1]	CS	RAS	CAS	WE	BS	Addr	ACTION
Idle	H	X	X	X	X	X	NOP or Power Down
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	RA	Row (&Bank) Active; Latch Row Address
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh[5]
	L	L	L	L	Op-	Code	Mode reg. Access[5]
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BS	CA,AP	Begin Read; Latch CA; DetermineAP Begin Write; Latch CA;
	L	H	L	L	BS	CA,AP	DetermineAP
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, New Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	Term Burst, Start Write, DetermineAP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Term Burst, Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, Start Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	Term Burst, New Write, DetermineAP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Term Burst, Precharge[3]
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL

SDRAM Function Truth Table (continued)

CURRENT STATE[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS	Addr	ACTION
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Precharging	H	X	X	X	X	X	NOP;> Idle after tRP
	L	H	H	H	X	X	NOP;> Idle after Trp
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	X	X	X	ILLEGAL
Row Activating	H	X	X	X	X	X	NOP;> Row Active after tRCD
	L	H	H	H	X	X	NOP;> Row Active after tRCD
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Write Recovering	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	NOP;> Idle after tRC
	L	H	H	H	X	X	NOP;> Idle after tRC
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

Clock Enable (CKE) Truth Table

STATE(n)	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	ACTION
Self-Refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	H	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power-Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	H	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Low-Power Mode)
All Banks Idle[7]	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	H	X	X	X	X	Enter Power- Down
	H	L	L	H	H	H	X	Enter Power- Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP

Abbreviations:

RA = Row Address of Bank A
RB = Row Address of Bank B
RC = Row Address of Bank C
RD = Row Address of Bank D

CA = Column Address of Bank A
CB = Column Address of Bank B
CC = Column Address of Bank C
CD = Column Address of Bank D

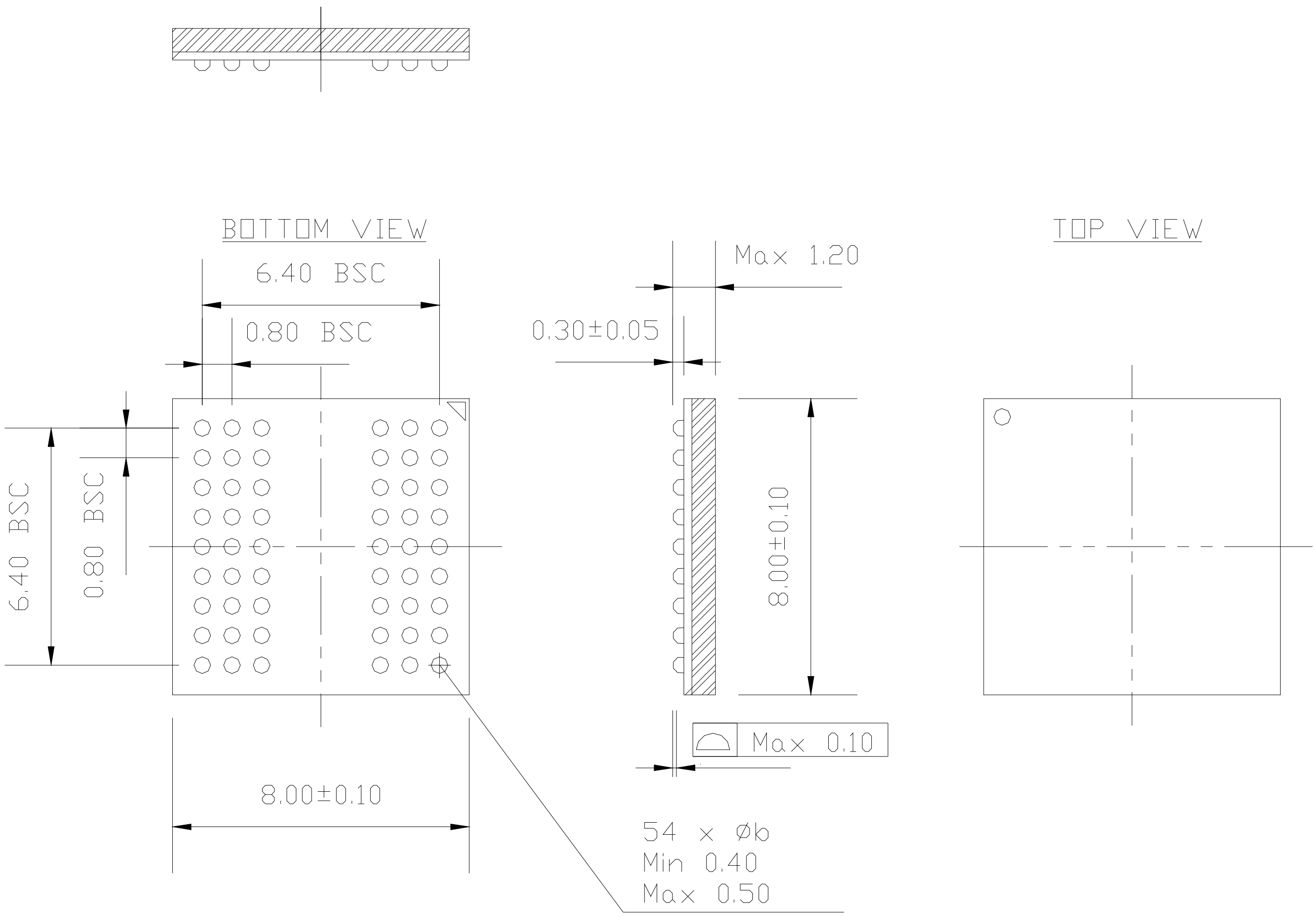
BS = Bank Address
AP = Auto Precharge

Notes for SDRAM function truth table:

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. May precharge bank(s) indicated by BS (and AP).
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.

Package Diagram (x16)

54-Ball Fine Pitch Ball Grid Array Outline



Revision History

Rev.	History	Release Date	Remarks
0.1	Initial release	Jan. 2020	
1.0	Formal release	Nov. 2020	
2.0	1. Revise Signal Pin Description 2. Remove TSOP SDRAM 3. Update Datasheet Format	Aug. 2022	