# *IM1232SDBA(B/T)*
# *128Mbit SDRAM*
# *4 Bank x 1Mbit x 32*

| | **6** |
|---|---|
| System Frequency ($f_{CK}$) | 166 MHz |
| Clock Cycle Time ($t_{CK3}$) | 6 ns |
| Clock Access Time ($t_{AC3}$) $\overline{CAS}$ Latency = 3 | 5.4 ns |
| Clock Access Time ($t_{AC2}$) $\overline{CAS}$ Latency = 2 | 6 ns |

## *Features*

- 4 banks x 1Mbit x 32 organization
- High speed data transfer rates up to 166 MHz
- Full Synchronous Dynamic RAM, with all signals referenced to clock rising edge
- Single Pulsed $\overline{RAS}$ Interface
- Data Mask for Read/Write Control
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8 and full page for Sequential Type
  1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Random Column Address every CLK (1-N Rule)
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 86 Pin TSOP II / 90 ball FBGA
- LVTTL Interface
- Single 3.3 V ± 0.3 V Power Supply

| ***Option*** | **Marking** |
|---|---|
| • Configuration | |
| -4Mx32 (4 Bank x 1Mbit x 32) | 1232 |
| • Package | |
| -86-pin TSOP | T |
| -90-ball FBGA (8mm x 13mm) | B |
| • Leaded/Lead-free | |
| Leaded | <blank> |
| Lead-free/RoHS | G |
| • Speed/Cycle Time | |
| 6ns @ CL3 (PC166) | -6 |
| • Temperature | |
| Commercial 0°C to 70°C Ta | <blank> |
| Industrial -40°C to 85°C Ta | I |
| • Automotive Grade | |
| Non-Automotive | <blank> |
| Automotive AEC-Q100 | A |

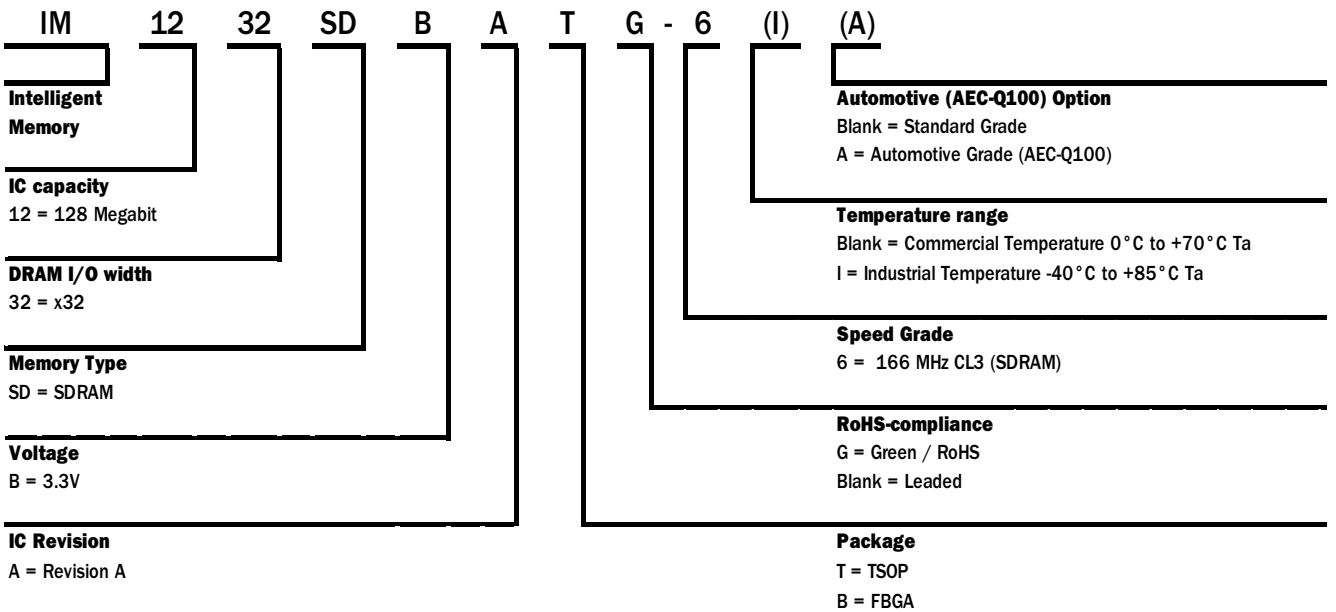
## *Description*

The IM1232SDBA(B/T) is a four bank Synchronous DRAM organized as 4 banks x 1Mbit x 32 . The IM1232SDBA(B/T) achieves high speed data transfer rates up to 166 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

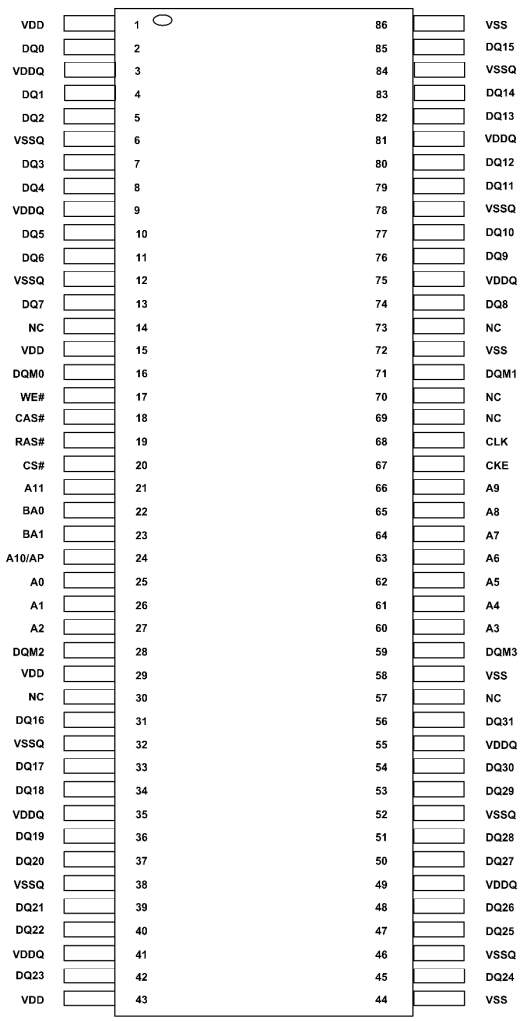
Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 166 MHz is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

## *Part Number Information*



| Description | Pkg. | Pin Count |
|---|---|---|
| TSOP-II | T | 86 |

### *86 Pin Plastic TSOP-II x32*
### *PIN CONFIGURATIO Top View*



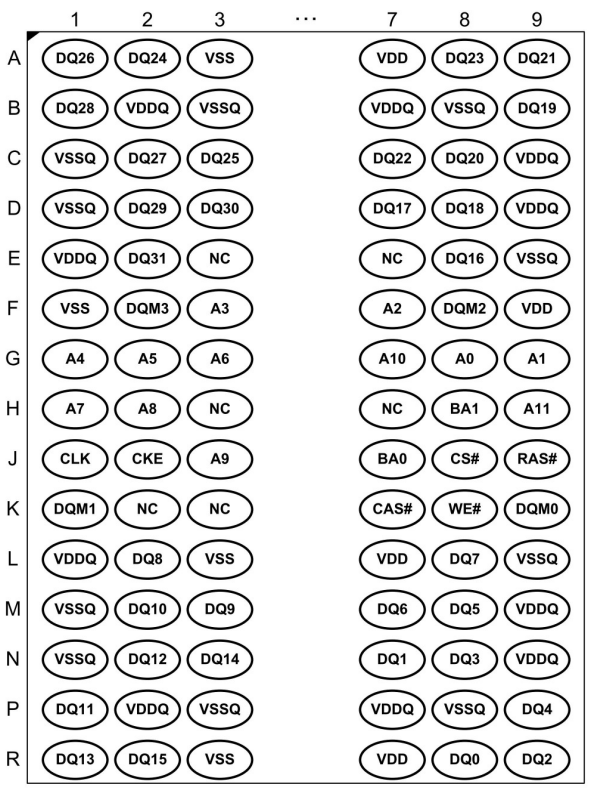

### *Pin Names*

| | |
|---|---|
| CLK | Clock Input |
| CKE | Clock Enable |
| CS | Chip Select |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| WE | Write Enable |
| $A_0$–$A_{11}$ | Address Inputs |
| BA0, BA1 | Bank Select |
| DQ0-DQ31 | Data Input/Output |
| DQM | Data Mask |
| VDD | Power (3.3V ± 0.3V) |
| VSS | Ground |
| VDDQ | Power for I/O's (3.3V ± 0.3V) |
| VSSQ | Ground for I/O's |
| NC | Not connected |

| Description | Pkg. | Pin Count |
|---|---|---|
| FBGA | B | 90 |

### *90 BALL FBGA x32PIN CONFIGURATION Top View*

for x 32 devices :




### *Pin Names*

| | |
|---|---|
| CLK | Clock Input |
| CKE | Clock Enable |
| CS | Chip Select |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| WE | Write Enable |
| A0-A11 | Address Inputs |
| BA0, BA1 | Bank Select |
| DQ0-DQ31 | Data Input/Output |
| DQM | Data Mask |
| VDD | Power (3.3V ± 0.3V) |
| VSS | Ground |
| VDDQ | Power for I/O's (3.3V ± 0.3V) |
| VSSQ | Ground for I/O's |
| NC | Not connected |

## *Capacitance**

(at Ta = 25 °C, VDD = VDDQ = 3.3 V ± 0.3 V)

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance: CLK | $C_{CLK}$ | 4.5 | 6 | pF |
| Input Capacitance: All other input pins and balls | $C_{IN}$ | 2.5 | 6 | pF |
| Input/output Capacitance: DQ | $C_{IO}$ | 4 | 6 | pF |

***Note:**Capacitance is sampled and not 100% tested.

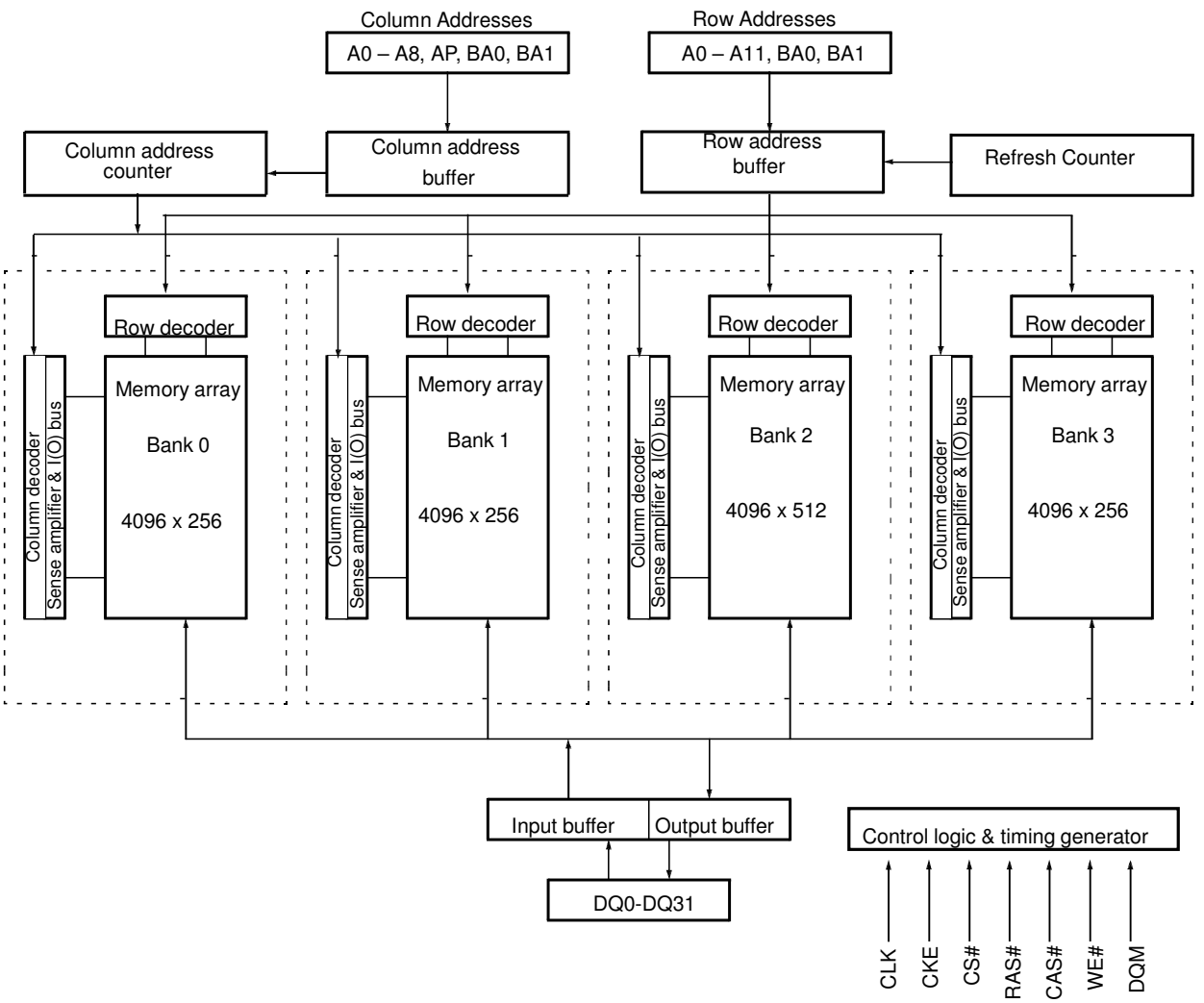
## *Absolute Maximum Ratings**

Operating temperature range .....0 to 70 °C for Commercial
-40 to 85 °C for Industrial
Storage temperature range .....-55 to 150 °C
Input/output voltage ..... -0.3 to (VDD±0.3) V
Power supply voltage ..... -0.3 to 4.6 V
Power dissipation ..... 1 W
Data out current (short circuit) ..... 50 mA

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## *Block Diagram*

**X32 Configuration**



## *Signal Pin Description*

| Pin | Type | Function |
|---|---|---|
| CLK | Input | **Clock:** CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers |
| CKE | Input | **Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CLK signal. If CKE goes low synchronously with clock(set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power. |
| BA0, BA1 | Input | **Bank Activate:** BA0 and BA1 defines to which bank the Bank Activate, Read, Write, or Bank Precharge command is being applied. The bank address BA0 and BA1 is used latched in mode register set. |
| A0 - A11 | Input | **Address Inputs:** A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 1M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the opcode during a Mode Register Set or Special Mode Register Set command. |
| $\overline{CS}$ | Input | **Chip Select:** $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code. |
| $\overline{RAS}$ | Input | **Row Address Strobe:** The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CLK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "LOW" and $\overline{CAS}$ is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the $\overline{WE}$ signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{WE}$ is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation. |
| $\overline{CAS}$ | Input | **Column Address Strobe:** The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CLK. When $\overline{RAS}$ is held "HIGH" and $\overline{CS}$ is asserted "LOW," the column access is started by asserting $\overline{CAS}$ "LOW." Then, the Read or Write command is selected by asserting $\overline{WE}$ "LOW" or "HIGH." |
| $\overline{WE}$ | Input | **Write Enable:** The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals and is latched at the positive edges of CLK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command. |
| DQM0-DQM3 | Input | **Data Input/Output Mask: Data Input Mask:** DQM0-DQM3 are byte specific. Input data is masked when DQM is sampled HIGH during a write cycle. DQM3 masks DQ31-DQ24, DQM2 masks DQ23-DQ16, DQM1 masks DQ15-DQ8, and DQM0 masks DQ7-DQ0. |
| DQ0-DQ31 | Input Output | **Data I/O:** The DQ0-31 input and output data are synchronized with the positive edges of CLK. The I/Os are byte-maskable during Reads and Writes. |
| NC | - | **No Connect:** These pins should be left unconnected. |
| VDDQ | Supply | **DQ Power:** Provide isolated power to DQs for improved noise immunity. |
| VSSQ | Supply | **DQ Ground:** Provide isolated ground to DQs for improved noise immunity. |

| Pin | Type | Function |
|---|---|---|
| VDD | Supply | **Power Supply:** 3.3V ± 0.3V. |
| VSS | Supply | **Ground** |

### *Operation Definition*

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 4 shows the truth table for the operation commands.

**Table 4. Truth Table (Note (1), (2))**

| Command | State | $CKE_{n-1}$ | $CKE_n$ | DQM(6) | BA0,1 | A10 | A11,9-0 | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank Activate | Idle(3) | H | X | X | V | Row address | | L | L | H | H |
| Bank Precharge | Any | H | X | X | V | L | X | L | L | H | L |
| Precharge All | Any | H | X | X | X | H | X | L | L | H | L |
| Write | Active(3) | H | X | V | V | L | Column address (A0 ~ A7) | L | H | L | L |
| Write and Auto Precharge | Active(3) | H | X | V | V | H | | L | H | L | L |
| Read | Active(3) | H | X | V | V | L | Column address (A0 ~ A7) | L | H | L | H |
| Read and Auto Precharge | Active(3) | H | X | V | V | H | | L | H | L | H |
| Mode Register Set | Idle | H | X | X | OP code | | | L | L | L | L |
| No-Operation | Any | H | X | X | X | X | X | L | H | H | H |
| Burst Stop | Active(4) | H | X | X | X | X | X | L | H | H | L |
| Device Deselect | Any | H | X | X | X | X | X | H | X | X | X |
| AutoRefresh | Idle | H | H | X | X | X | X | L | L | L | H |
| SelfRefresh Entry | Idle | H | L | X | X | X | X | L | L | L | H |
| SelfRefresh Exit | Idle (SelfRefresh) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | H |
| Clock Suspend Mode Entry | Active | H | L | X | X | X | X | H | X | X | X |
| | | | | | | | | L | V | V | V |
| Power Down Mode Entry | Any(5) | H | L | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | H |
| Clock Suspend Mode Exit | Active | L | H | X | X | X | X | X | X | X | X |
| Power Down Mode Exit | Any (PowerDown) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | H |
| Data Write/Output Enable | Active | H | X | L | X | X | X | X | X | X | X |
| Date Mask/Output Disable | Active | H | X | H | X | X | X | X | X | X | X |

**Notes:**

1. V = Valid, X = Don't Care, L = Logic Low, H = Logic High
2. CKEn signal is input level when commands are provided
   CKEn-1 signal is input level one clock before the commands are provided.
3. These are states of bank designated by BA signal.
4. Device state is 1, 2, 4, 8 and full page burst operation.
5. Power Down Mode cannot enter in the burst operation.
   When the command is asserted in the burst cycle, device state is clock suspend mode.
6. DQM0-3

### *Power On and Initialization*

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 us is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of two Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

### *Programming the Mode Register*

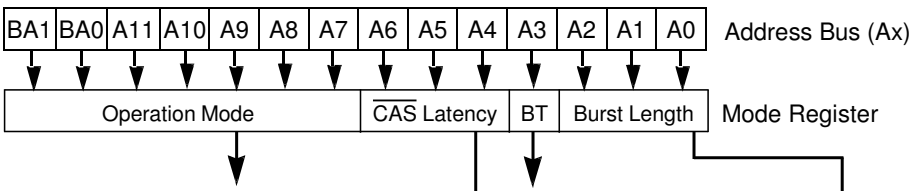
The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS Latency Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

### *Read and Write Operation*

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting RAS high and $\overline{CAS}$ low at a clock timing after a necessary delay, $t_{RCD}$, from the $\overline{RAS}$ timing. WE is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage. SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using sequential burst type. Full Page burst operation does not terminate once the burst length has been reached. (At the end of the page, it will wrap to the start address and continue.) In other words, unlike burst length of 2, 4, and 8, full page burst continues until it is terminated using another command.

### *Address Input for Mode Set (Mode Register Operation)*




**Operation Mode**

| BA1 | BA0 | A11 | A10 | A9 | A8 | A7 | Mode |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Burst Read/Burst Write |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | Burst Read/Single Write |

**Burst Type**

| A3 | Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

**CAS Latency**

| A6 | A5 | A4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserve |
| 0 | 0 | 1 | Reserve |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserve |
| 1 | 0 | 1 | Reserve |
| 1 | 1 | 0 | Reserve |
| 1 | 1 | 1 | Reserve |

**Burst Length**

| A2 | A1 | A0 | Length | |
|---|---|---|---|---|
| | | | Sequential | Interleave |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserve | Reserve |
| 1 | 0 | 1 | Reserve | Reserve |
| 1 | 1 | 0 | Reserve | Reserve |
| 1 | 1 | 1 | Full Page | Reserve |

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum $t_{RAS}$ or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

### *Burst Length and Sequence:*

| Burst Length | Starting Address (A2 A1 A0) | Sequential Burst Addressing (decimal) | Interleave Burst Addressing (decimal) |
|---|---|---|---|
| 2 | xx0 | 0, 1 | 0, 1 |
| | xx1 | 1, 0 | 1, 0 |
| 4 | x00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | x01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | x10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | x11 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 000 | 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 |
| | 001 | 1 2 3 4 5 6 7 0 | 1 0 3 2 5 4 7 6 |
| | 010 | 2 3 4 5 6 7 0 1 | 2 3 0 1 6 7 4 5 |
| | 011 | 3 4 5 6 7 0 1 2 | 3 2 1 0 7 6 5 4 |
| | 100 | 4 5 6 7 0 1 2 3 | 4 5 6 7 0 1 2 3 |
| | 101 | 5 6 7 0 1 2 3 4 | 5 4 7 6 1 0 3 2 |
| | 110 | 6 7 0 1 2 3 4 5 | 6 7 4 5 2 3 0 1 |
| | 111 | 7 0 1 2 3 4 5 6 | 7 6 5 4 3 2 1 0 |
| Full Page | nnn | Cn, Cn+1, Cn+2.... | not supported |

### *Refresh Mode*

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before- $\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one $t_{RC}$ delay is required prior to any access command.

### *DQM Function*

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency $t_{DQZ}$ ). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency $t_{DQW}$ = zero clocks).

### *Power Down*

In order to reduce standby power consumption, a power down mode is available. All banks must be pre-charged and the necessary Precharge delay ($t_{RP}$) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period ($t_{REF}$) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for mode entry and exit.

### *Auto Precharge*

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for $\overline{CAS}$ latencies 2, two clocks for $\overline{CAS}$ latencies 3 and three clocks for $\overline{CAS}$ latencies 4. If CA10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to $t_{WR}$ (Write recovery time) after the last data in. **Auto-Precharge** does not apply to full-page burst mode.

### *Precharge Command*

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2, two clocks before the last data out for $\overline{CAS}$ latency = 3. Writes require a time delay tWR from the last data out to apply the precharge command. A full-page burst may be truncated with a Precharge command to the same bank.

Bank Selection by Address Bits:

| A10 | BA0 | BA1 | |
|---|---|---|---|
| 0 | 0 | 0 | Bank 0 |
| 0 | 0 | 1 | Bank 1 |
| 0 | 1 | 0 | Bank 2 |
| 0 | 1 | 1 | Bank 3 |
| 1 | X | X | all Banks |

### *Burst Termination*

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory. The full-page burst is used in conjunction with Burst Terminate Command to generate arbitrary burst lengths.

## *Recommended Operation and Characteristics for LV-TTL*

$V_{SS}$ = 0 V; $V_{DD}$, $V_{DDQ}$ = 3.3 V ± 0.3 V

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high level voltage | $V_{IH}$ | 2.0 | - | $V_{DD}$ +0.3 | V | 1, 2 |
| Input low level voltage | $V_{IL}$ | - 0.3 | - | 0.8 | V | 1, 2 |
| Output high level voltage ($I_{OUT}$ = – 4.0 mA) | $V_{OH}$ | 2.4 | - | - | V | |
| Output low level voltage ($I_{OUT}$ = 4.0 mA) | $V_{OL}$ | - | - | 0.4 | V | |
| Input leakage current, any input ($0V < V_{IN} < V_{DD}$, All other pins not under test = 0V) | $I_{IL}$ | -10 | - | 10 | uA | |
| Output leakage current (Output Disable, $0V < V_{IN} < V_{DDQ}$) | $I_{OZ}$ | -10 | - | 10 | uA | |

**Note:**

1. All voltages are referenced to $V_{SS}$.
2. $V_{IH}$ may overshoot to $V_{DD}$ + 2.0 V for pulse width of < 4ns with 3.3V. $V_{IL}$ may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

## *Operating Currents*

$V_{DD}$ = 3.3 V ± 0.3 V (Recommended Operating Conditions unless otherwise noted)

| Symbol | Parameter & Test Condition | | Max. -6 | | Note |
|---|---|---|---|---|---|
| IDD1 | Operating Current $t_{RC} = t_{RCMIN.}$, $t_{RC} = t_{CKMIN}$ Active-precharge command cycling, without Burst Operation | 1 bank operation | 160 | mA | 1 |
| IDD2P | Precharge Standby Current in Power Down Mode $\overline{CS}$ =$V_{IH}$, CKE≤ $V_{IL(max)}$ | $t_{CK}$ = min. | 3 | mA | 1 |
| IDD2PS | | $t_{CK}$ = Infinity | 3 | mA | 1 |
| IDD2N | Precharge Standby Current in Non-Power Down Mode CS =$V_{IH}$, CKE≥ $V_{IL(max)}$ | $t_{CK}$ = min. | 50 | mA | |
| IDD2NS | | $t_{CK}$ = Infinity | 30 | mA | |
| IDD3NS | No Operating Current $t_{CK}$ = min, CS = $V_{IH(min)}$ bank ; active state ( 4 banks) | CKE ≥ $V_{IH(MIN.)}$ | 50 | mA | |
| IDD3N | | CKE ≤ $V_{IL(MAX.)}$ (Power down mode) | 60 | mA | |
| IDD4 | Burst Operating Current $t_{CK}$ = min Read/Write command cycling | | 200 | mA | 1,2 |
| IDD5 | Auto Refresh Current $t_{CK}$ = min Auto Refresh command cycling | | 260 | mA | 1 |
| IDD6 | Self Refresh Current Self Refresh Mode, CKE≤ 0.2V | | 3 | mA | |

**Notes:**

1. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of $t_{CK}$ and $t_{RC}$. Input signals are changed one time during $t_{CK}$.
2. These parameter depend on output loading. Specified values are obtained with output open.

## *AC Characteristics* [1,2,3]

$V_{SS}$ = 0 V; $V_{DD}$ = 3.3 V ± 0.3 V

| # | Symbol | Parameter | Limit Values | | Unit | Note |
|---|---|---|---|---|---|---|
| | | | -6 | | | |
| | | | Min. | Max. | | |
| 1 | $t_{CK}$ | Clock Cycle Time<br>$\overline{CAS}$ Latency = 3<br>$\overline{CAS}$ Latency = 2 | <br>6<br>10 | <br>–<br>– | ns | |
| 2 | $t_{CK}$ | Clock Frequency<br>$\overline{CAS}$ Latency = 3<br>$\overline{CAS}$ Latency = 2 | <br>–<br>– | <br>166<br>100 | MHz | |
| 3 | $t_{AC}$ | Access Time from Clock<br>$\overline{CAS}$ Latency = 3<br>$\overline{CAS}$ Latency = 2 | <br>–<br>– | <br>5.4<br>6 | ns | 2, 3 |
| 4 | $t_{CH}$ | Clock High Time | 2.5 | – | ns | |
| 5 | $t_{CL}$ | Clock Low Time | 2.5 | – | ns | |
| 6 | $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay<br>(same bank) | 18 | – | ns | 5 |
| 7 | $t_{RP}$ | Precharge to refresh / Row activate Command<br>(same bank) | 18 | – | ns | 5 |
| 8 | $t_{RAS}$ | Row activate to Percharge Time<br>(same bank) | 42 | 100K | ns | 5 |
| 9 | $t_{RC}$ | Row Cycle Time<br>(same bank) | 60 | – | ns | 5 |
| 10 | $t_{RRD}$ | Row activate to Row active Delay<br>(different banks) | 12 | – | ns | 5 |
| 11 | $t_{CCD}$ | $\overline{CAS}$ to $\overline{CAS}$ Delay time | 1 | – | $t_{CK}$ | |
| 12 | $t_{OH}$ | Data Output Hold Time | 2.5 | – | ns | 2 |
| 13 | $t_{LZ}$ | Data Out to Low Impedance | 1 | – | ns | |
| 14 | $t_{HZ}$ | Data Out to High Impedance | – | 5.4 | ns | 6 |
| 15 | $t_{WR}$ | Write Recovery Time | 2 | – | $t_{CK}$ | |
| 16 | $t_{IS}$ | Data/Address/Control Input set-up Time | 1.5 | – | ns | |
| 17 | $t_{IH}$ | Data/Address/Control Input set-up Time | 0.8 | – | ns | |
| 18 | $t_{PDE}$ | Power Down Exit set-up time | $t_{IS} + t_{CK}$ | – | ns | |
| 19 | $t_{REFI}$ | Refresh Interval Time | – | 15.6 | us | |
| 20 | $t_{XSR}$ | Exit Self Refresh to any Command | $t_{IS} + t_{RC}$ | – | ns | |
| 21 | $t_{MRD}$ | Mode Register Set Command Cycle Time | 2 | – | $t_{CK}$ | |

### *Notes for AC Parameters:*

1. For proper power-up see the operation section of this data sheet.

2. AC timing tests have $V_{IL}$ = 0.4V and $V_{IH}$ = 2.4V with the timing referenced to the 1.4 V crossover point. The transition time is measured between $V_{IH}$ and $V_{IL}$. All AC measurements assume $t_T$ = 1ns with the AC output load circuit shown in Figure 1.

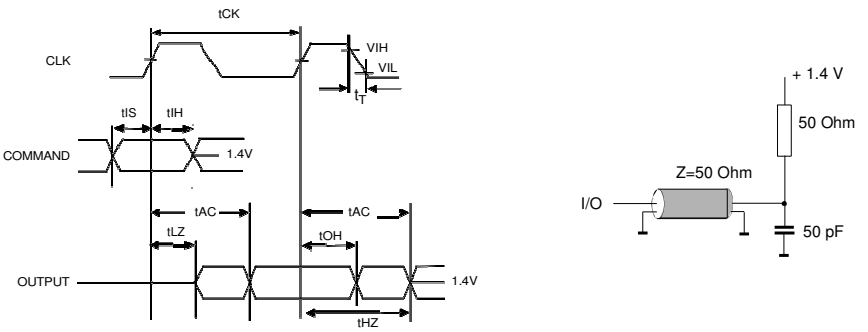



**Figure 1.**

3. If clock rising time is longer than 1 ns, a time ($t_T$/2 – 0.5)ns has to be added to this parameter.

4. If $t_T$ is longer than 1 ns, a time ($t_T$ – 1) ns has to be added to this parameter.

5. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

*the number of clock cycle = specified value of timing period (counted in fractions as a whole number)*

Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.

6. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

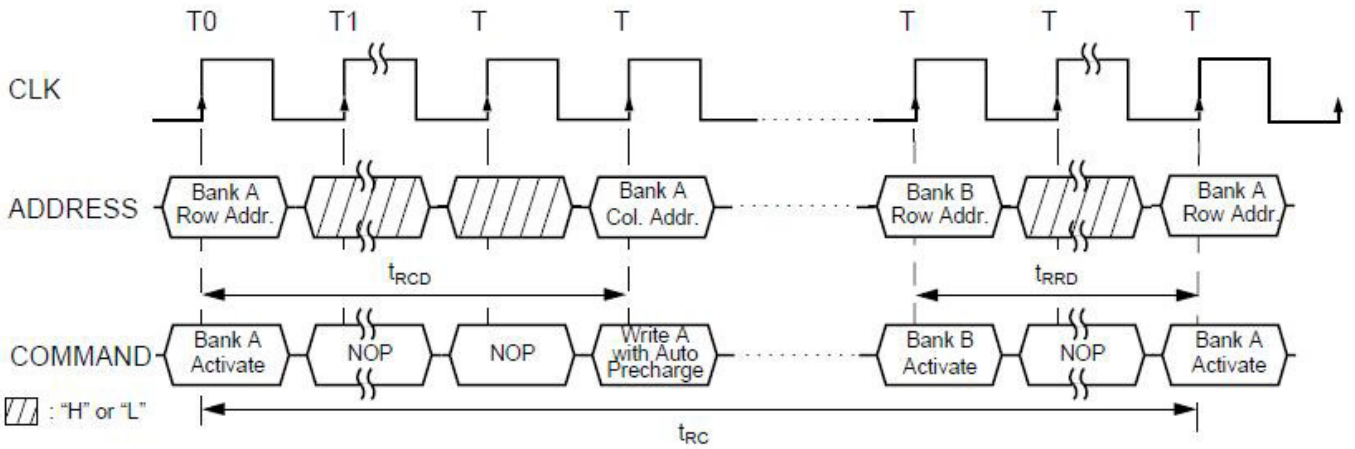
***Timing Diagrams***

***Timing Diagrams*** (Cont'd)

19. Precharge Termination of a Burst
    - 19.1 $\overline{\text{CAS}}$ Latency = 2
    - 19.2 $\overline{\text{CAS}}$ Latency = 3
20. Full Page Burst Operation
    - 20.1 Full Page Burst Read, $\overline{\text{CAS}}$ Latency = 2
    - 20.2 Full Page Burst Read, $\overline{\text{CAS}}$ Latency = 3
21. Full Page Burst Operation
    - 21.1 Full Page Burst Write, $\overline{\text{CAS}}$ Latency = 2
    - 21.2 Full Page Burst Write, $\overline{\text{CAS}}$ Latency = 3

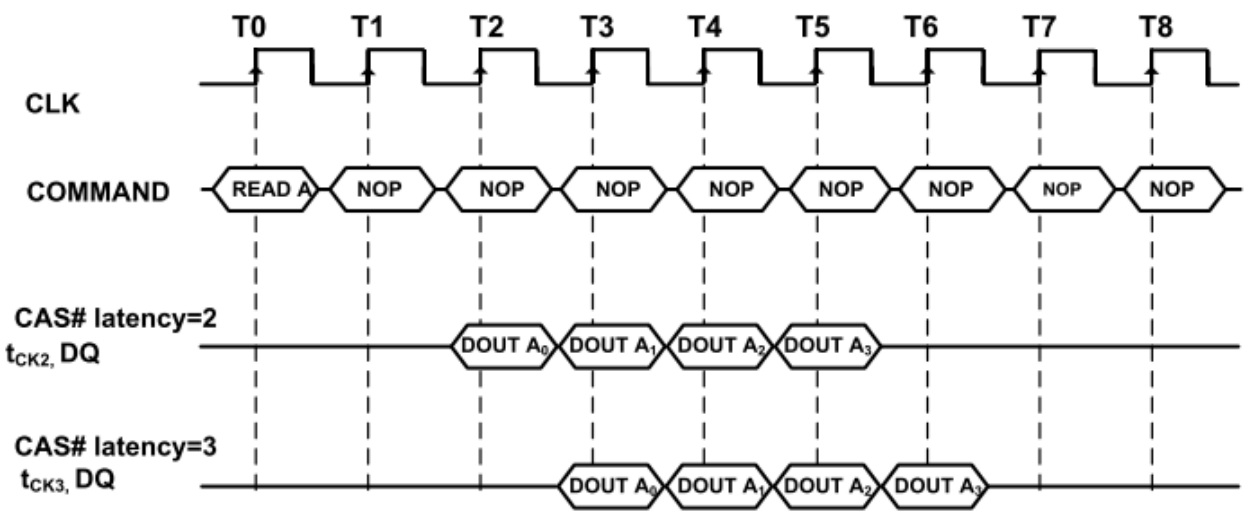
***1. Bank Activate Command Cycle***

***(CAS latency = 3)***



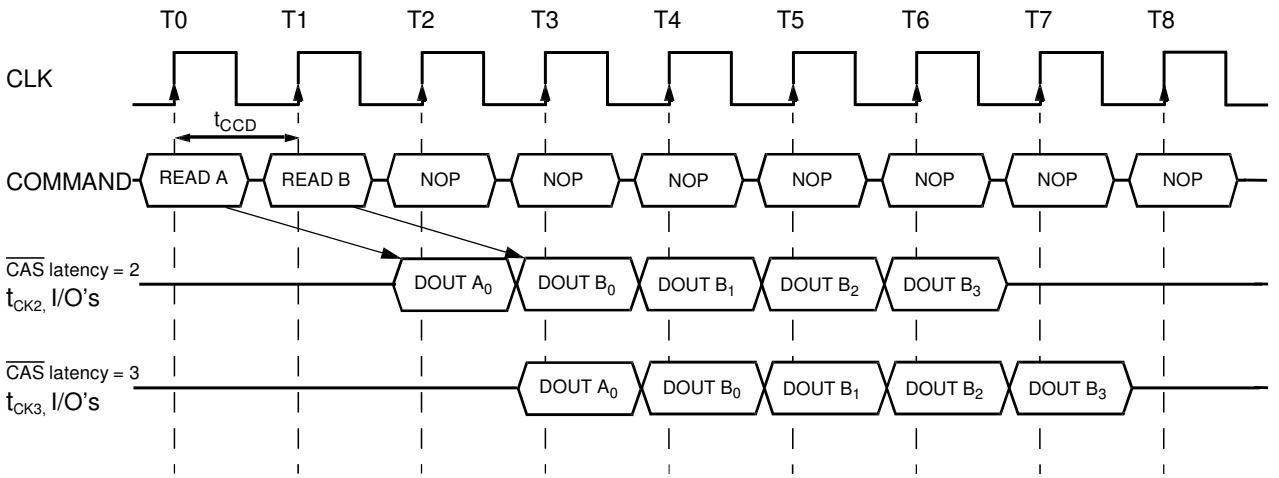

***2. Burst Read Operation***

***(Burst Length = 4, CAS latency = 2, 3)***



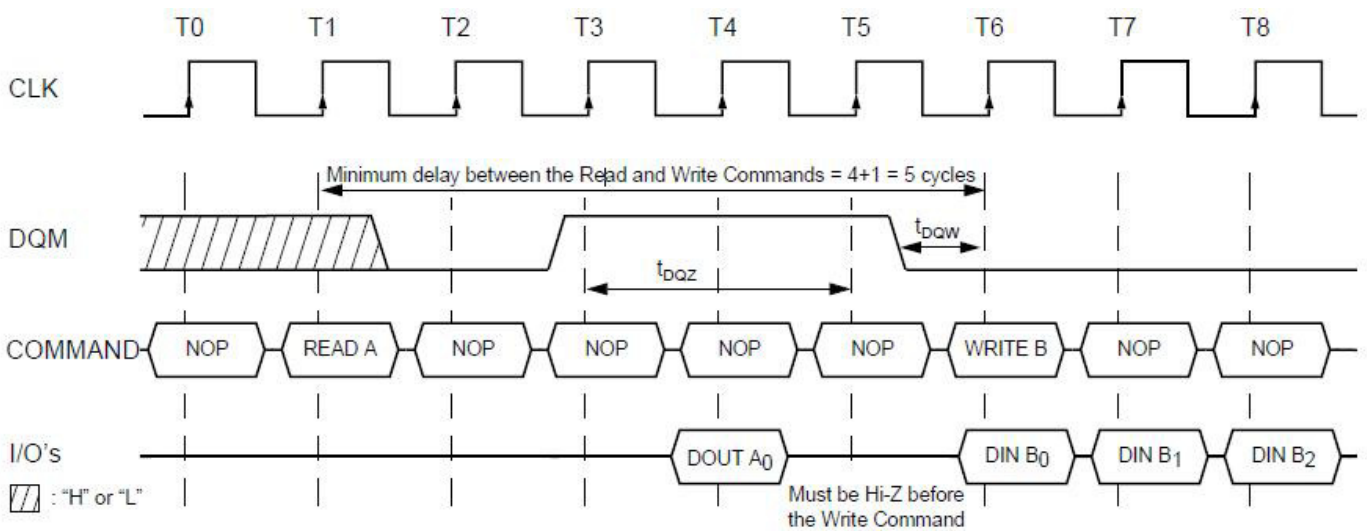
### *3. Read Interrupted by a Read*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



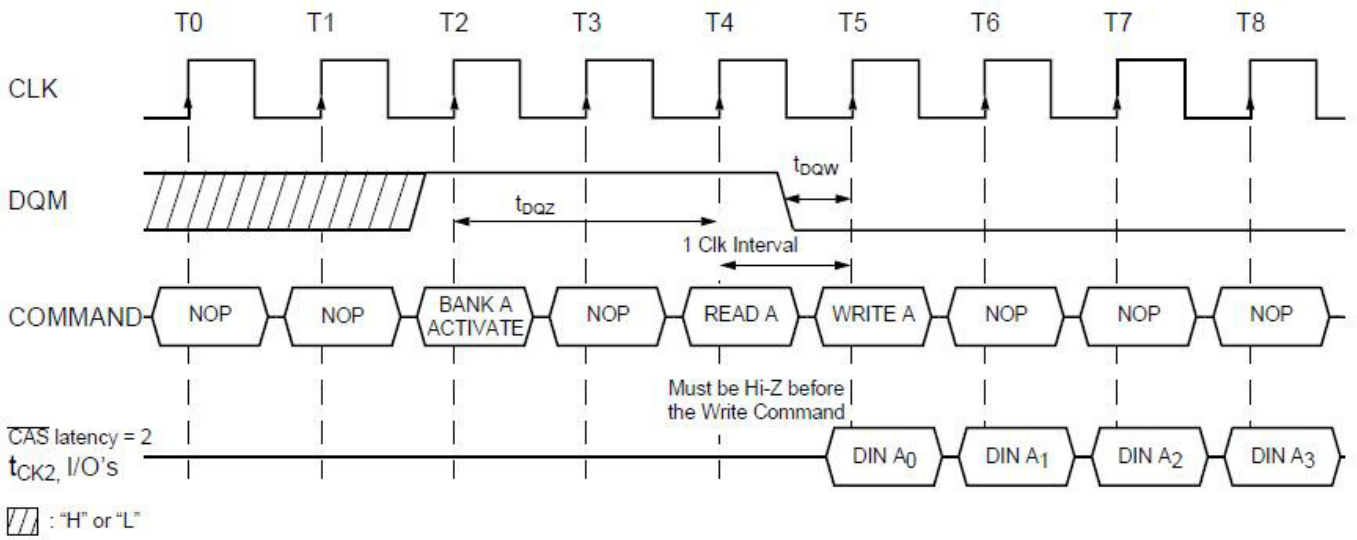

### *4.1 Read to Write Interval*

### *(Burst Length = 4, $\overline{CAS}$ latency = 3)*



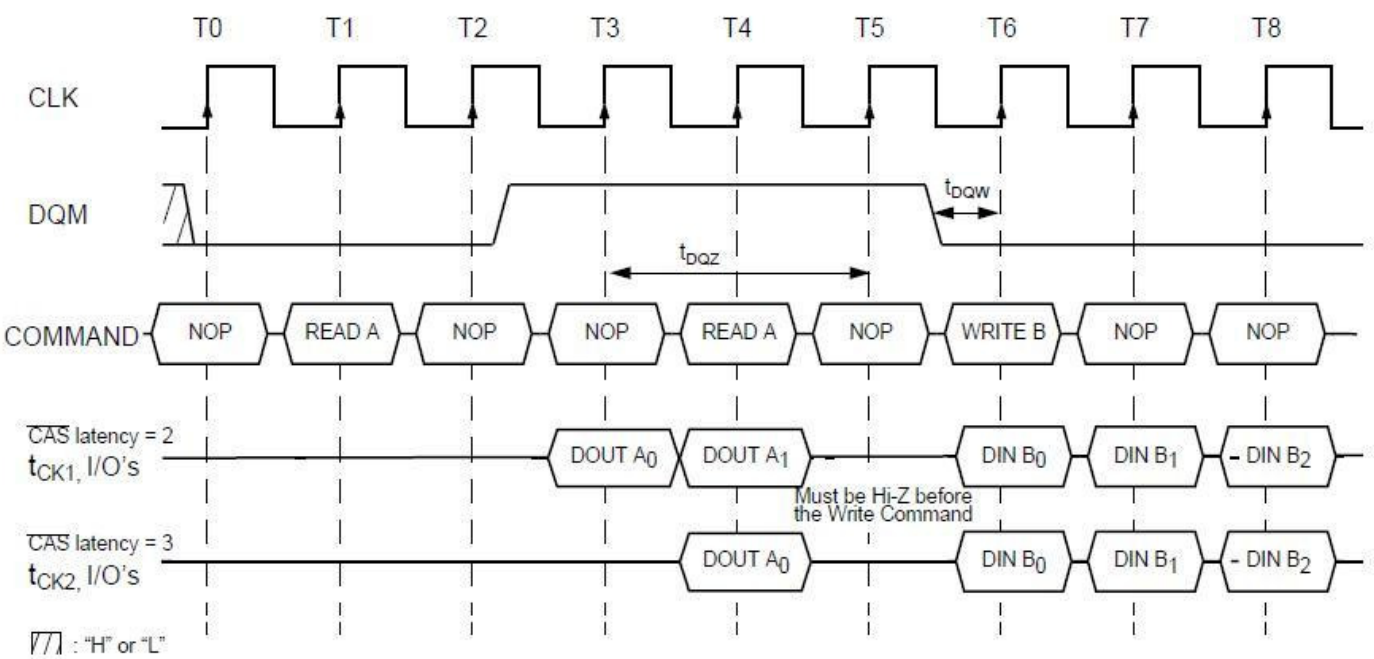
### *4.2 Minimum Read to Write Interval*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2)*



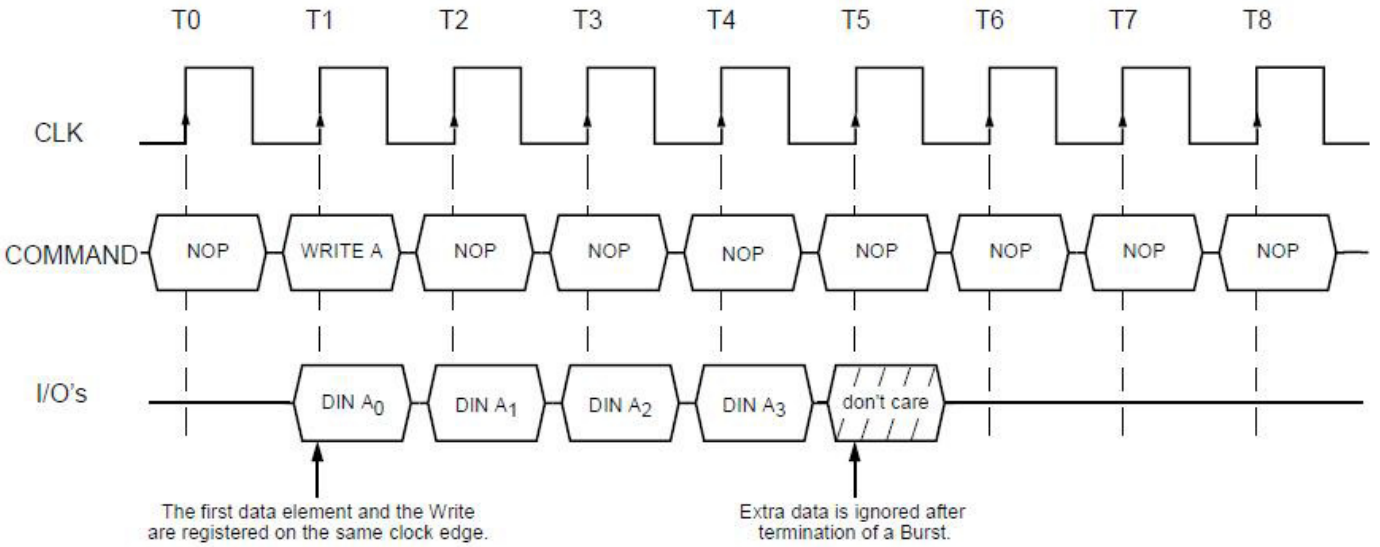

### *4.3 Non-Minimum Read to Write Interval*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



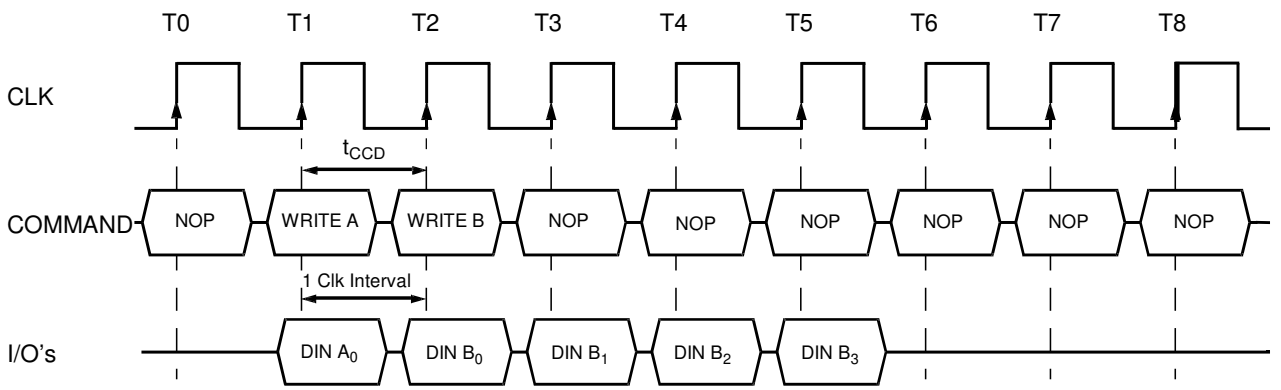
### *5. Burst Write Operation*

### *(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)*



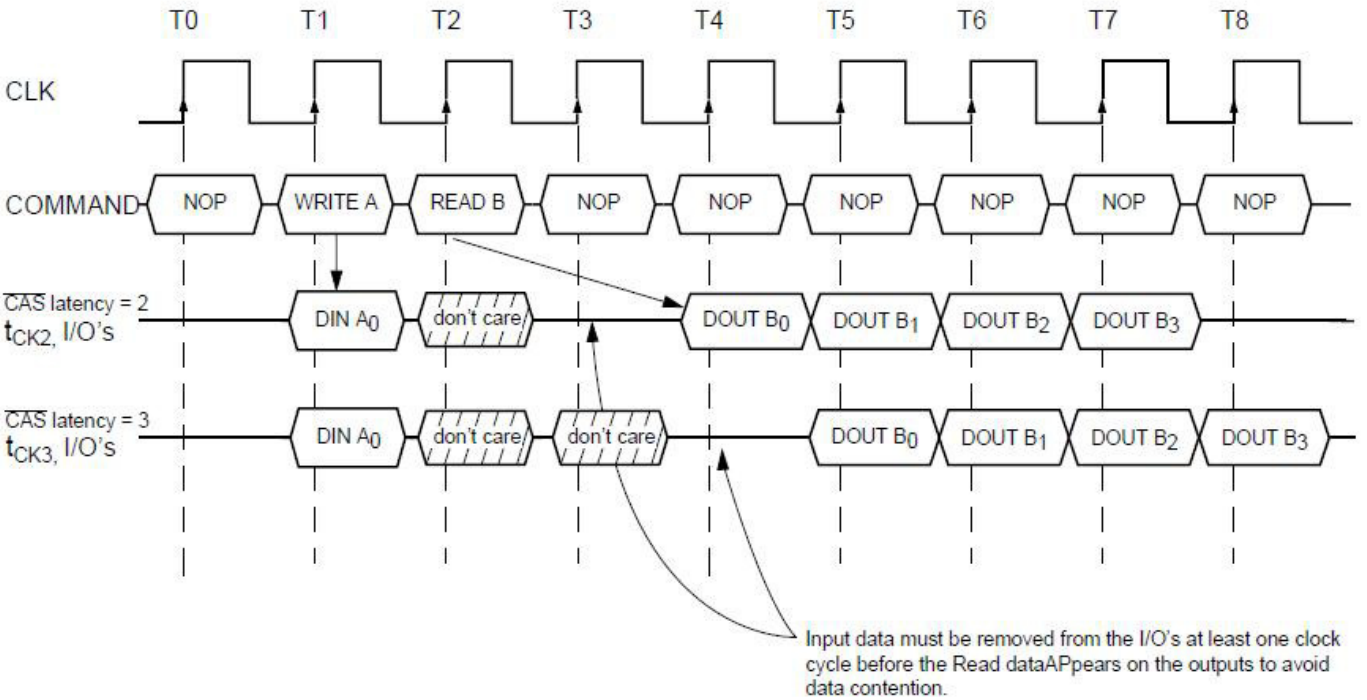

### *6.1 Write Interrupted by a Write*

### *(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)*



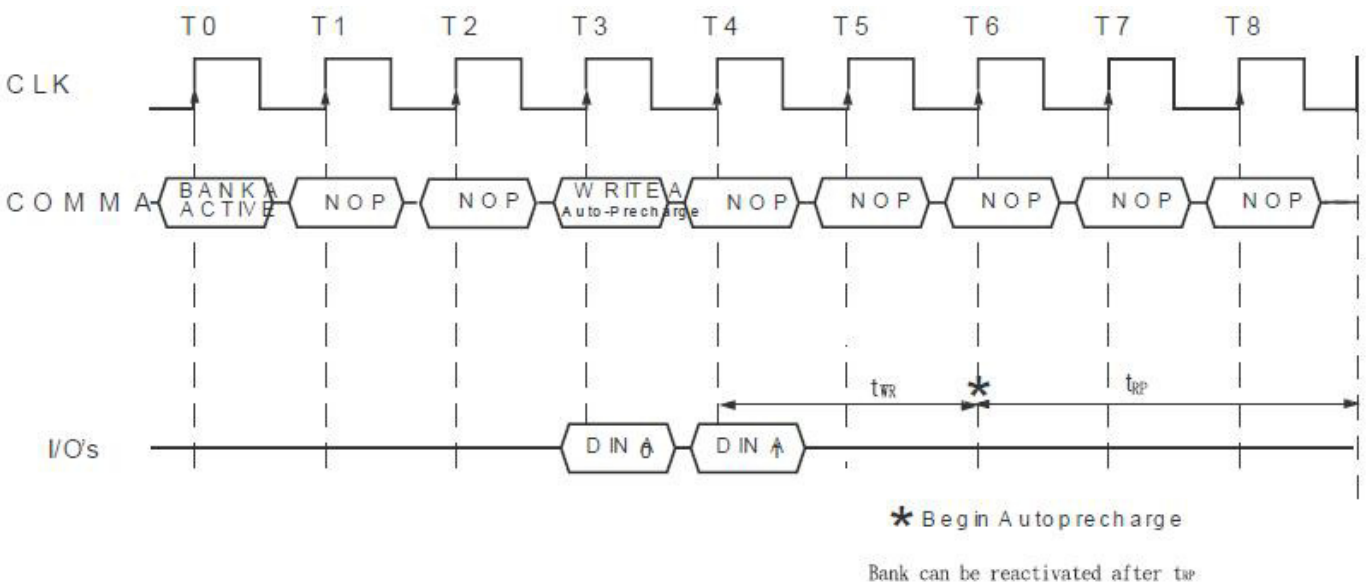
### *6.2 Write Interrupted by a Read*

### *(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)*



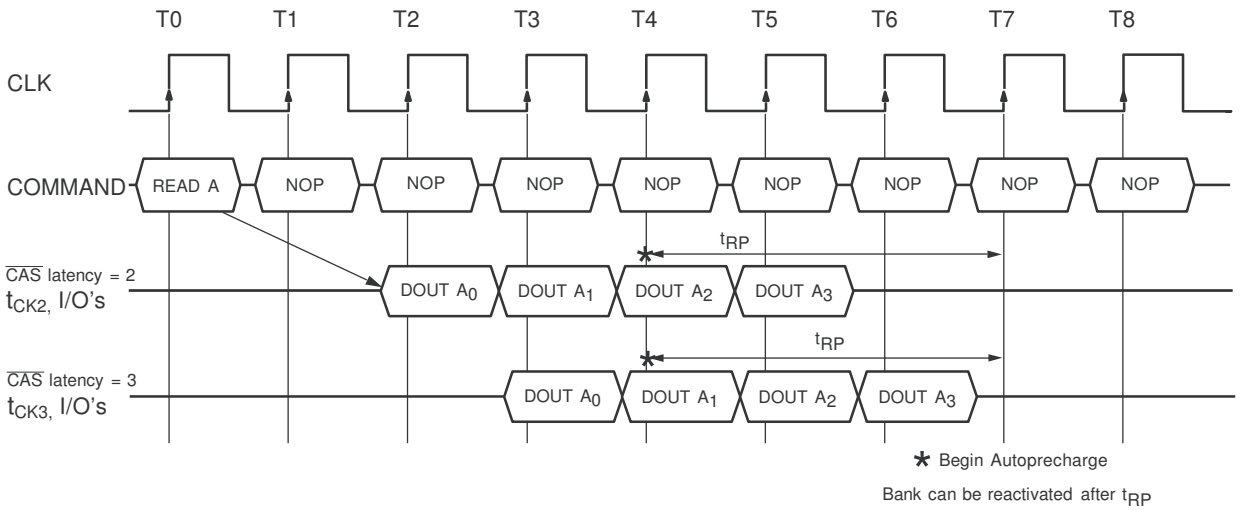

### *7.1 Burst Write with Auto-Precharge*

### *Burst Length = 2, $\overline{\text{CAS}}$ latency = 2, 3)*

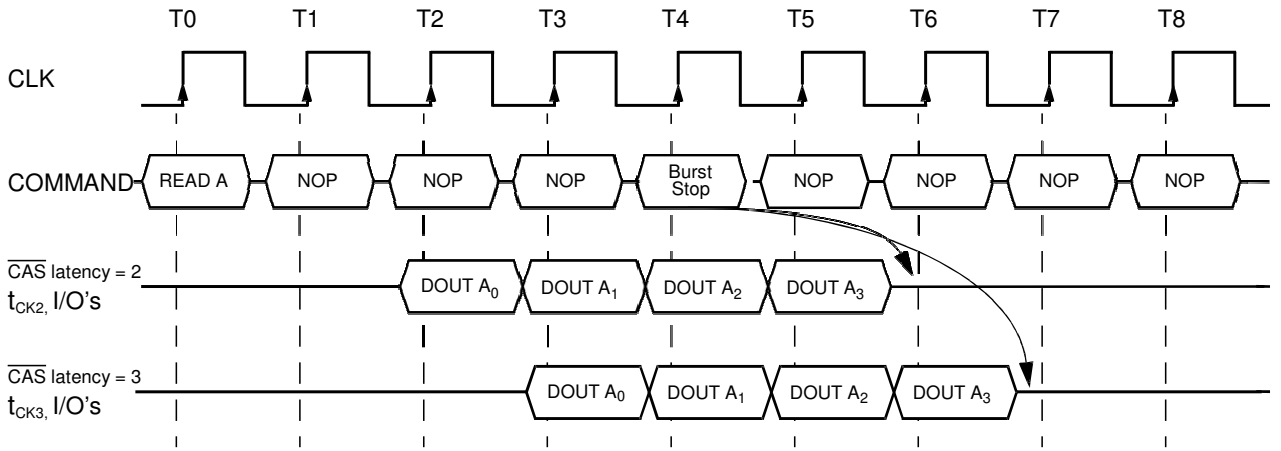


### *7.2 Burst Read with Auto-Precharge*

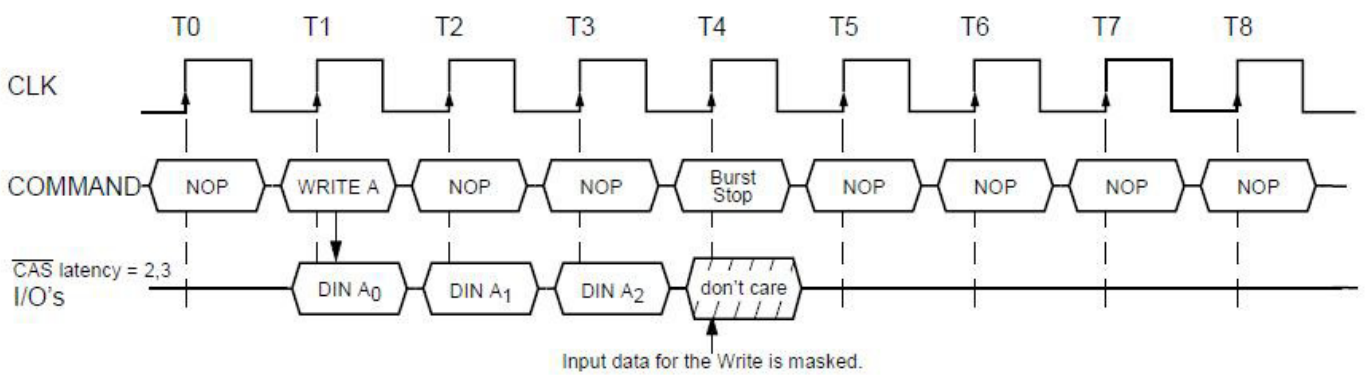
### *Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



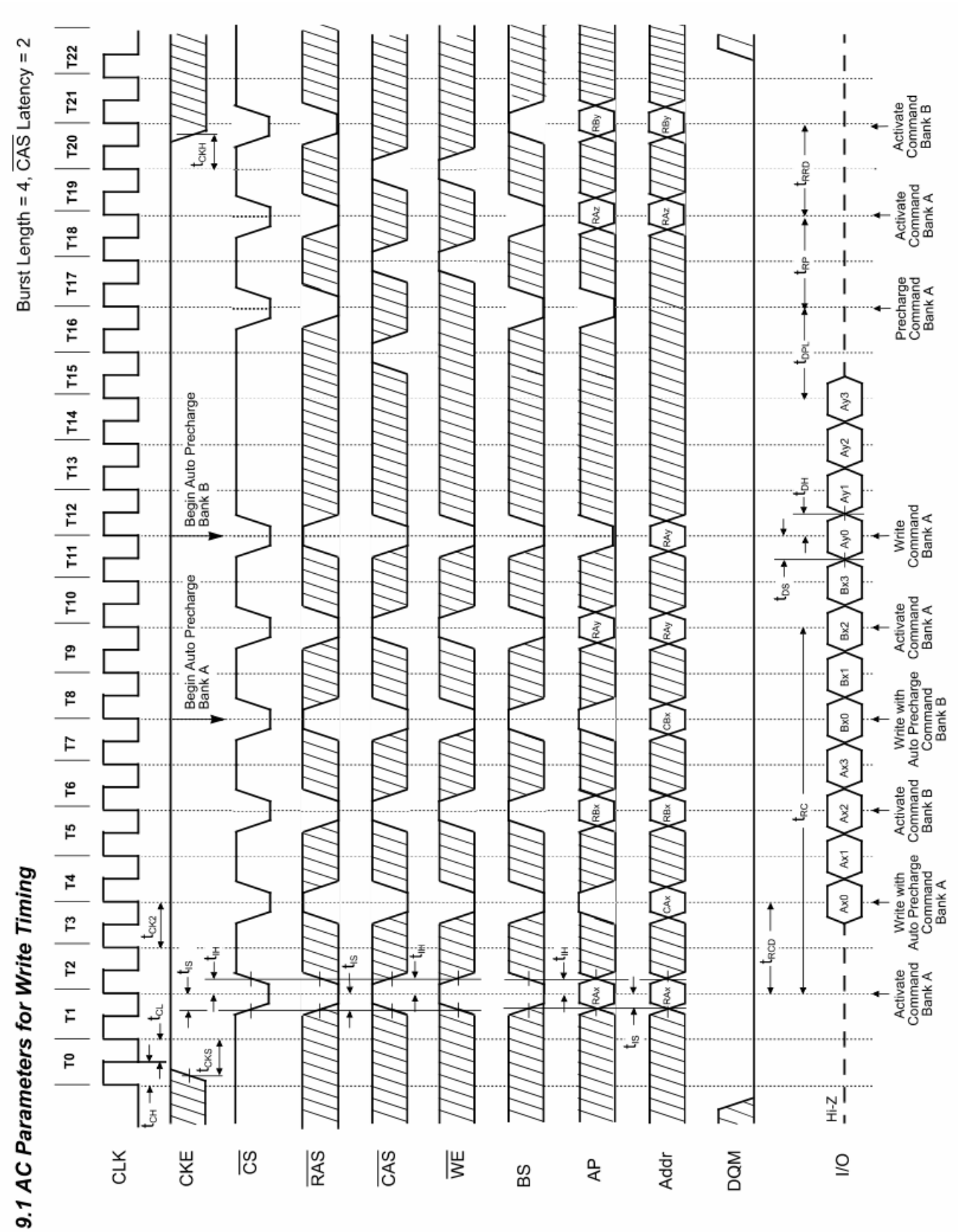
### *8.1 Termination of a Burst Read Operation*
### *(CAS latency = 2, 3)*



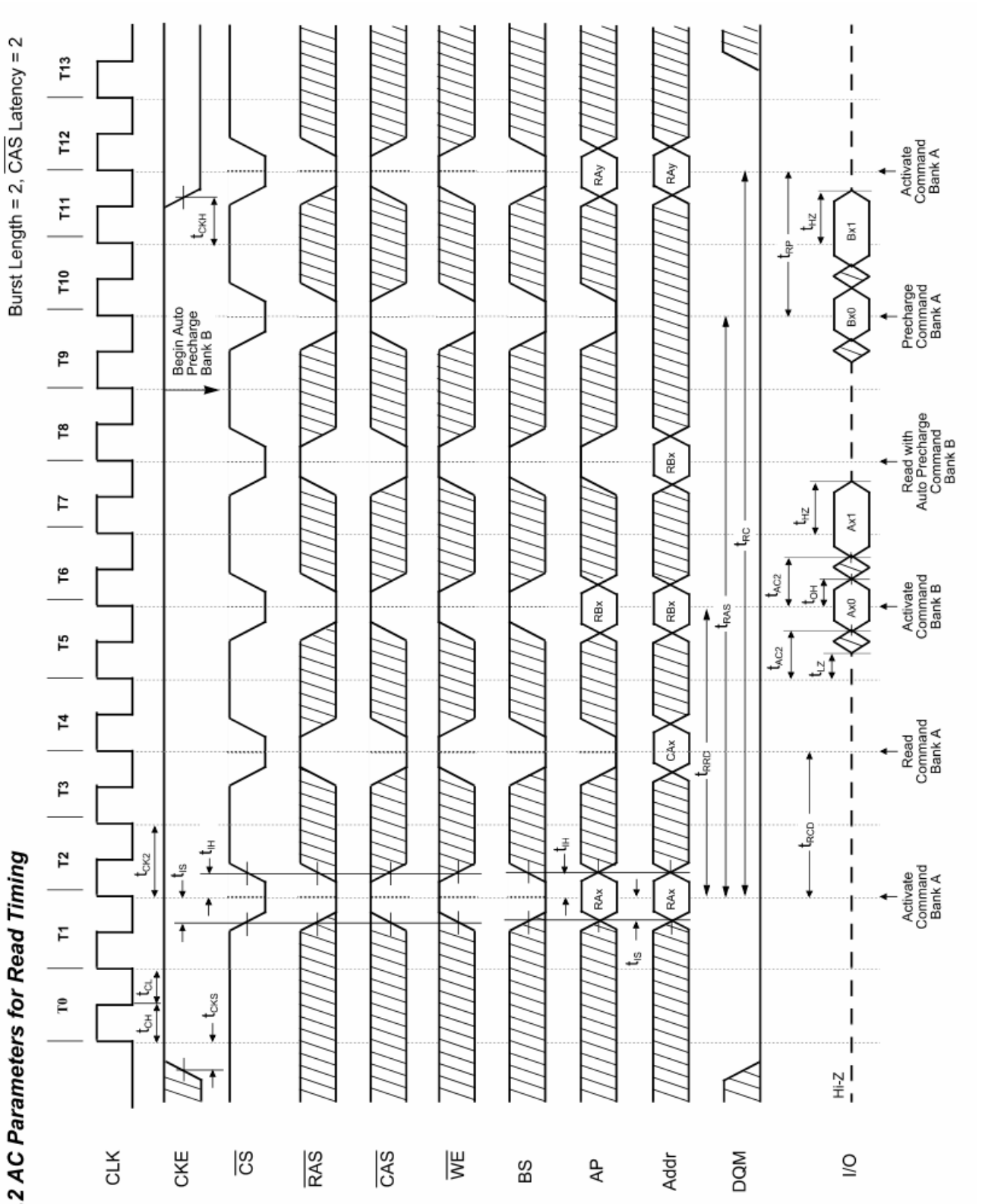

### *8.2 Termination of a Burst Write Operation*
### *(CAS latency = 2, 3)*



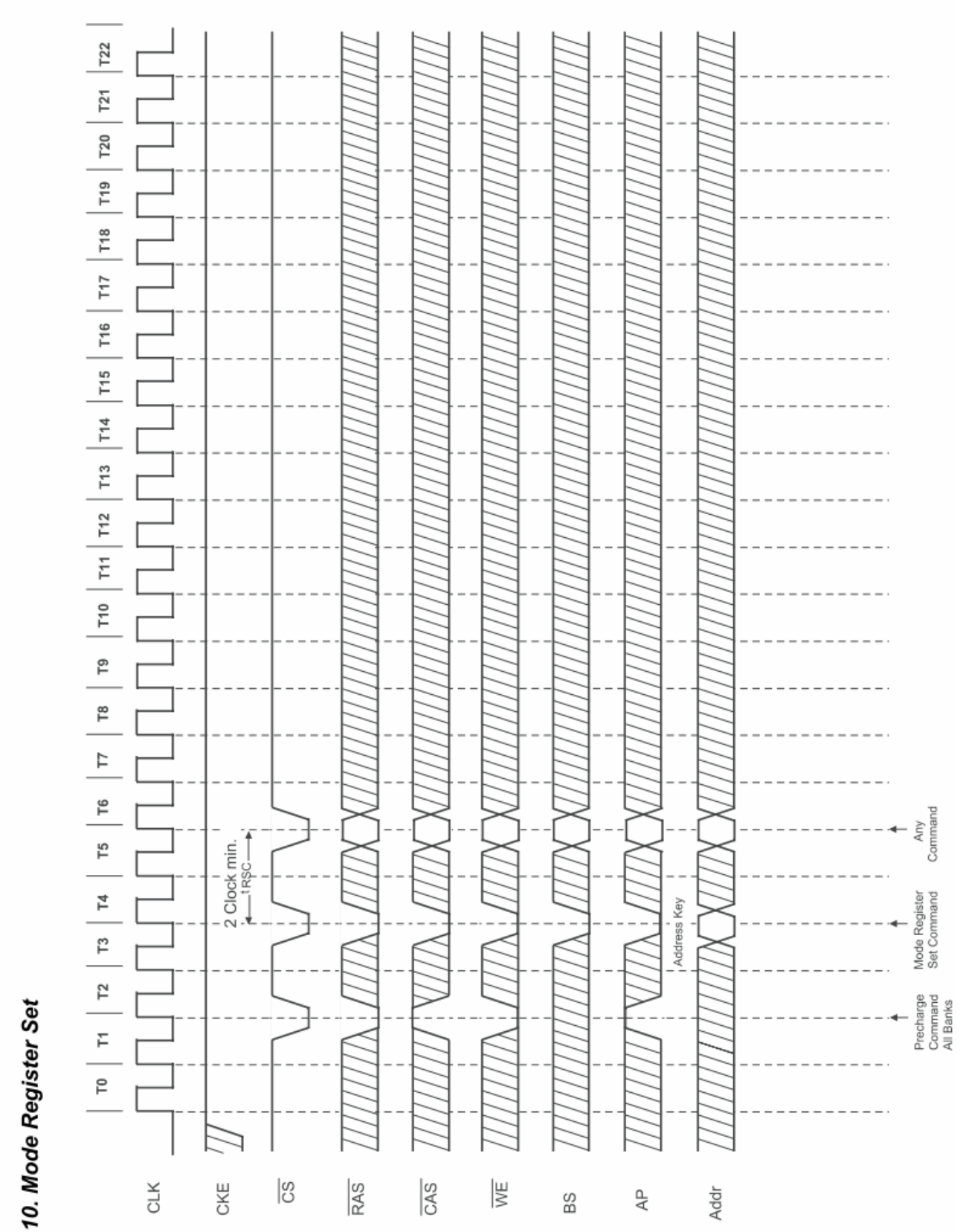
## 9.1 AC Parameters for Write Timing



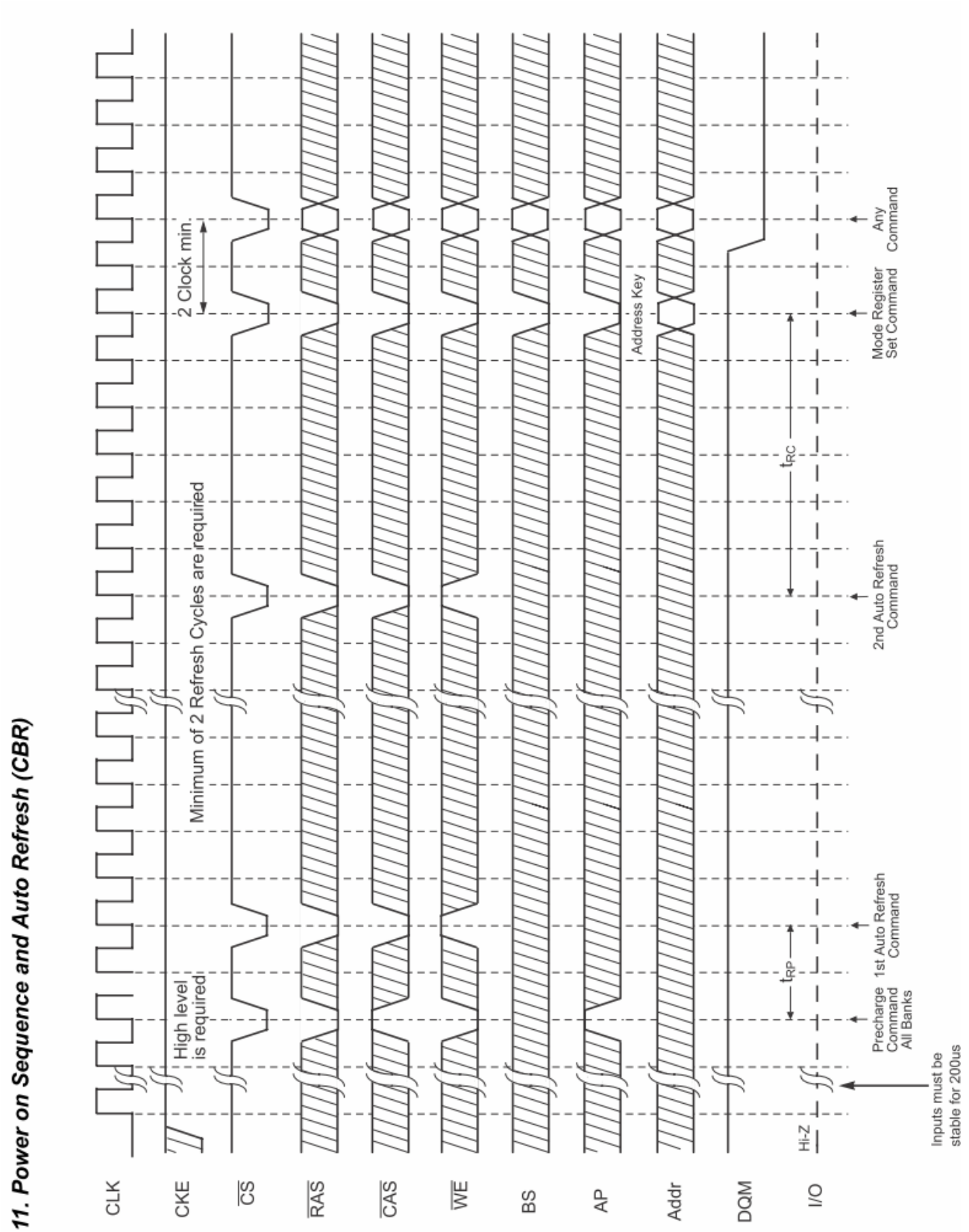
## 9.2 AC Parameters for Read Timing



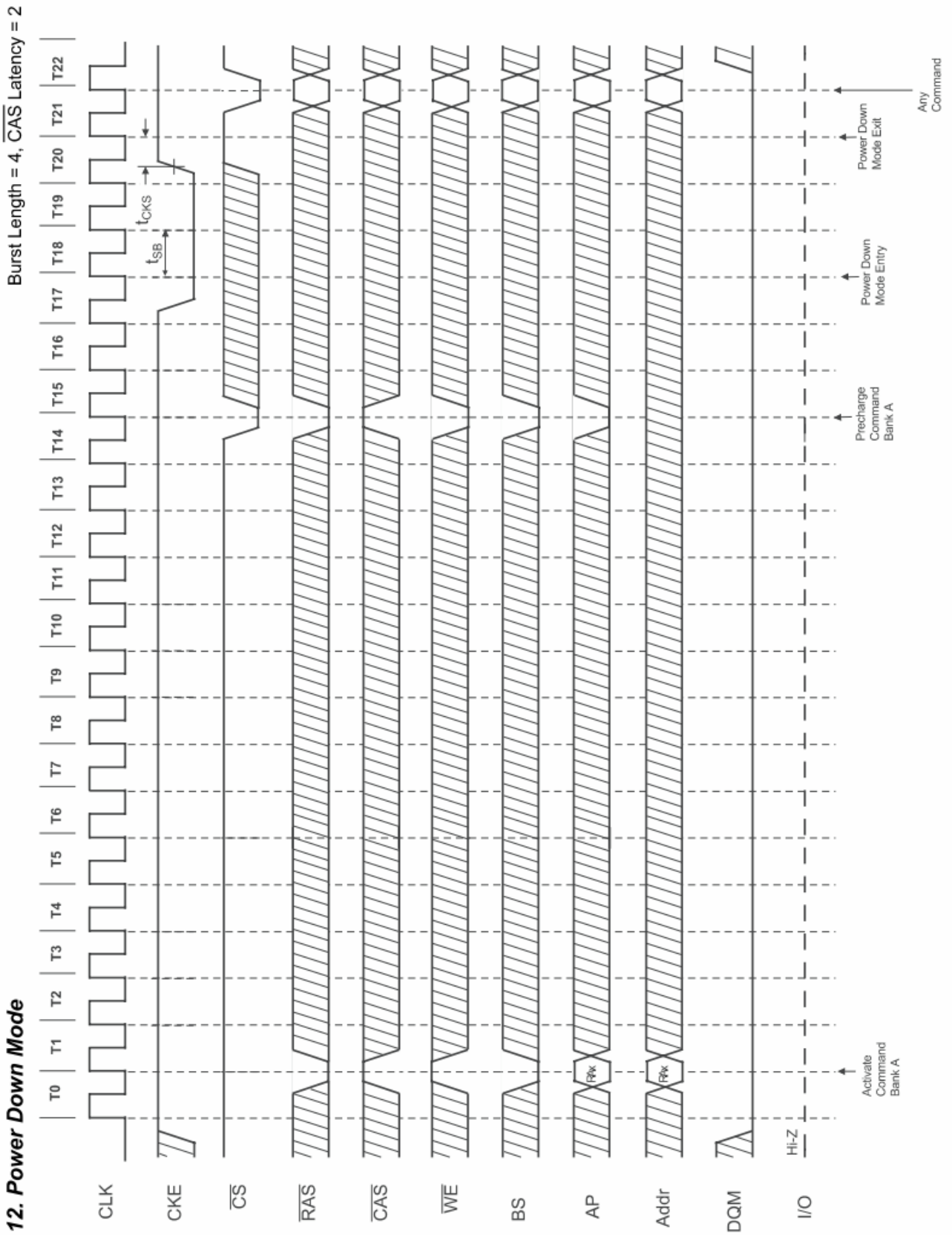
## 10. Mode Register Set



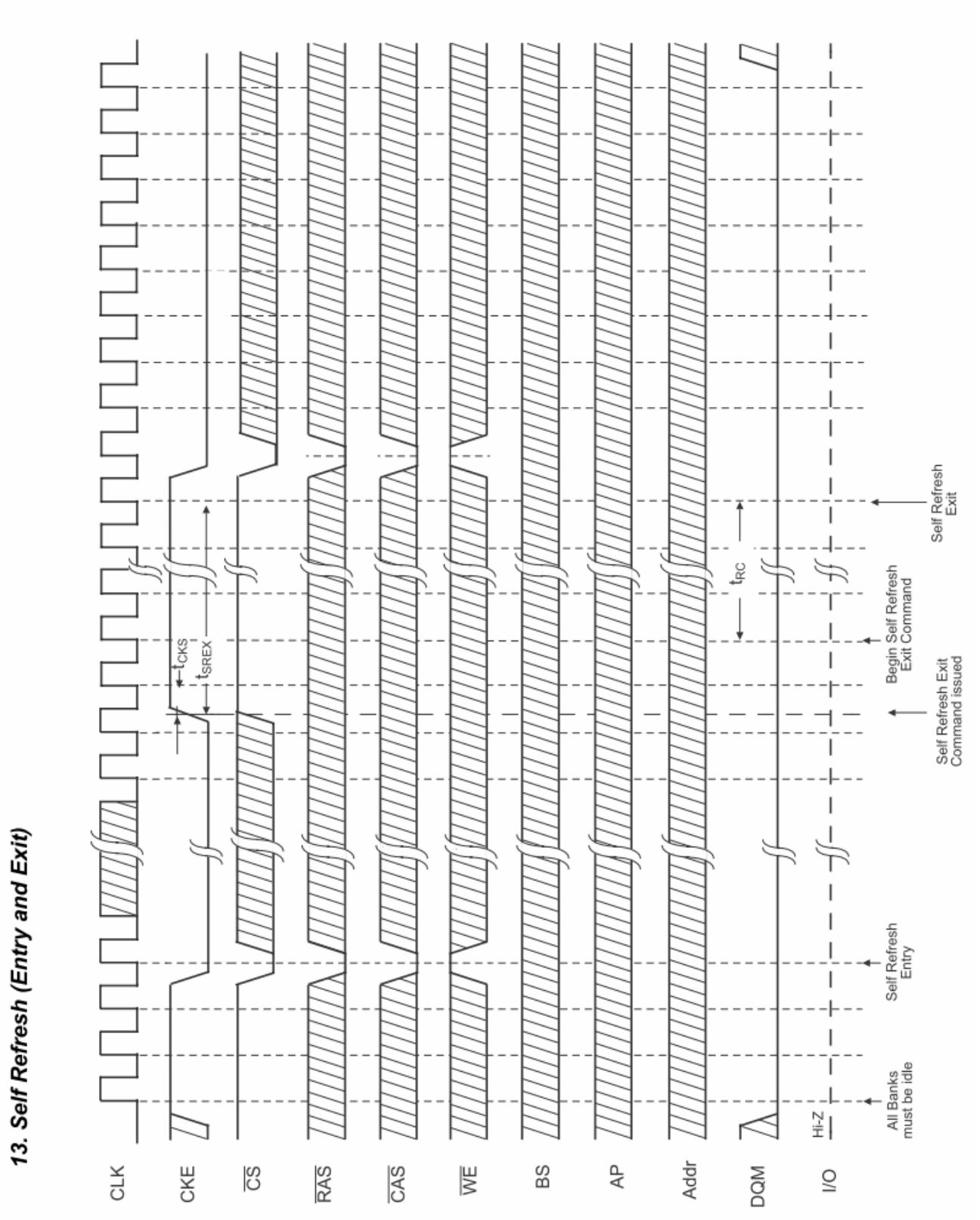
### 11. Power on Sequence and Auto Refresh (CBR)



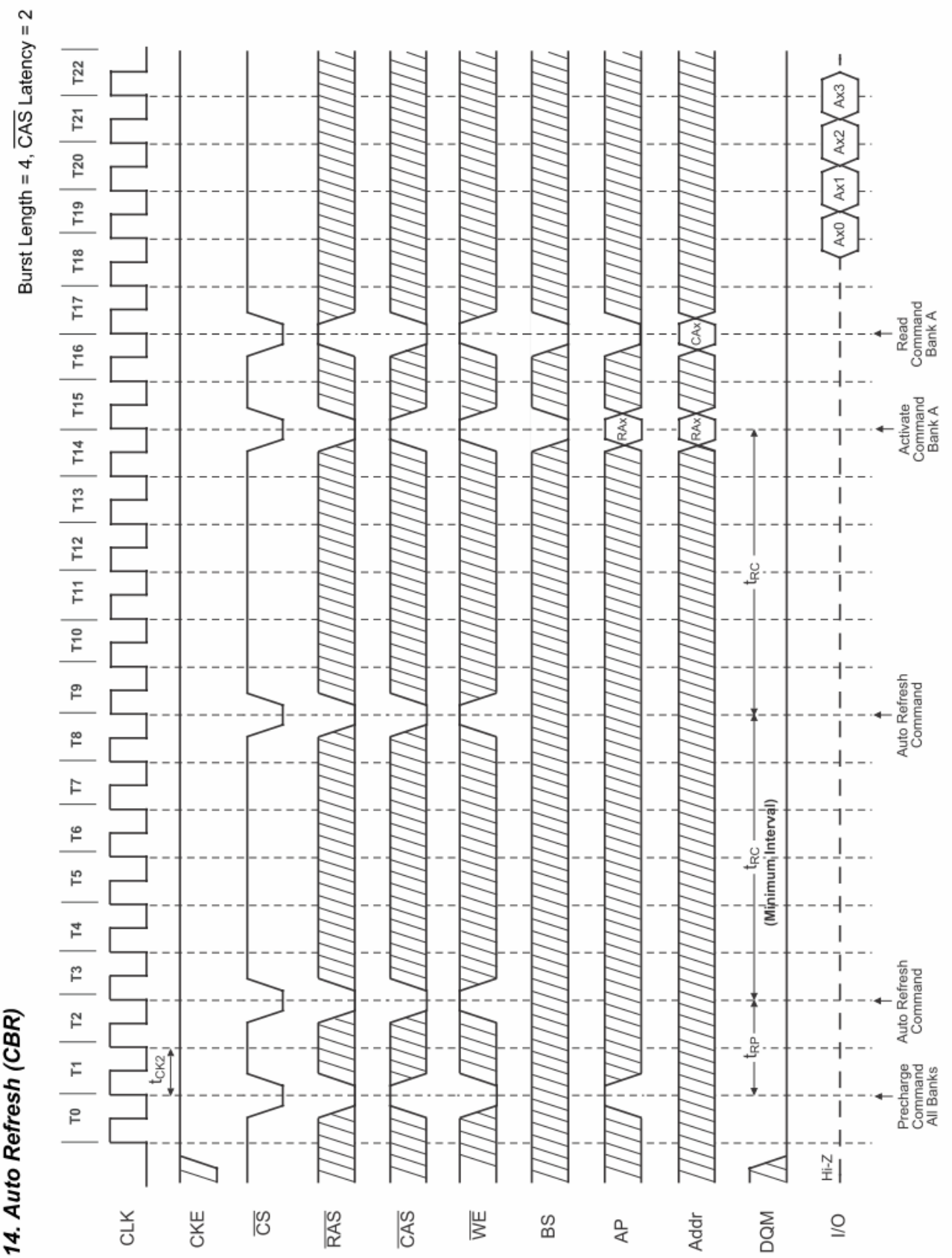
## 12. Power Down Mode



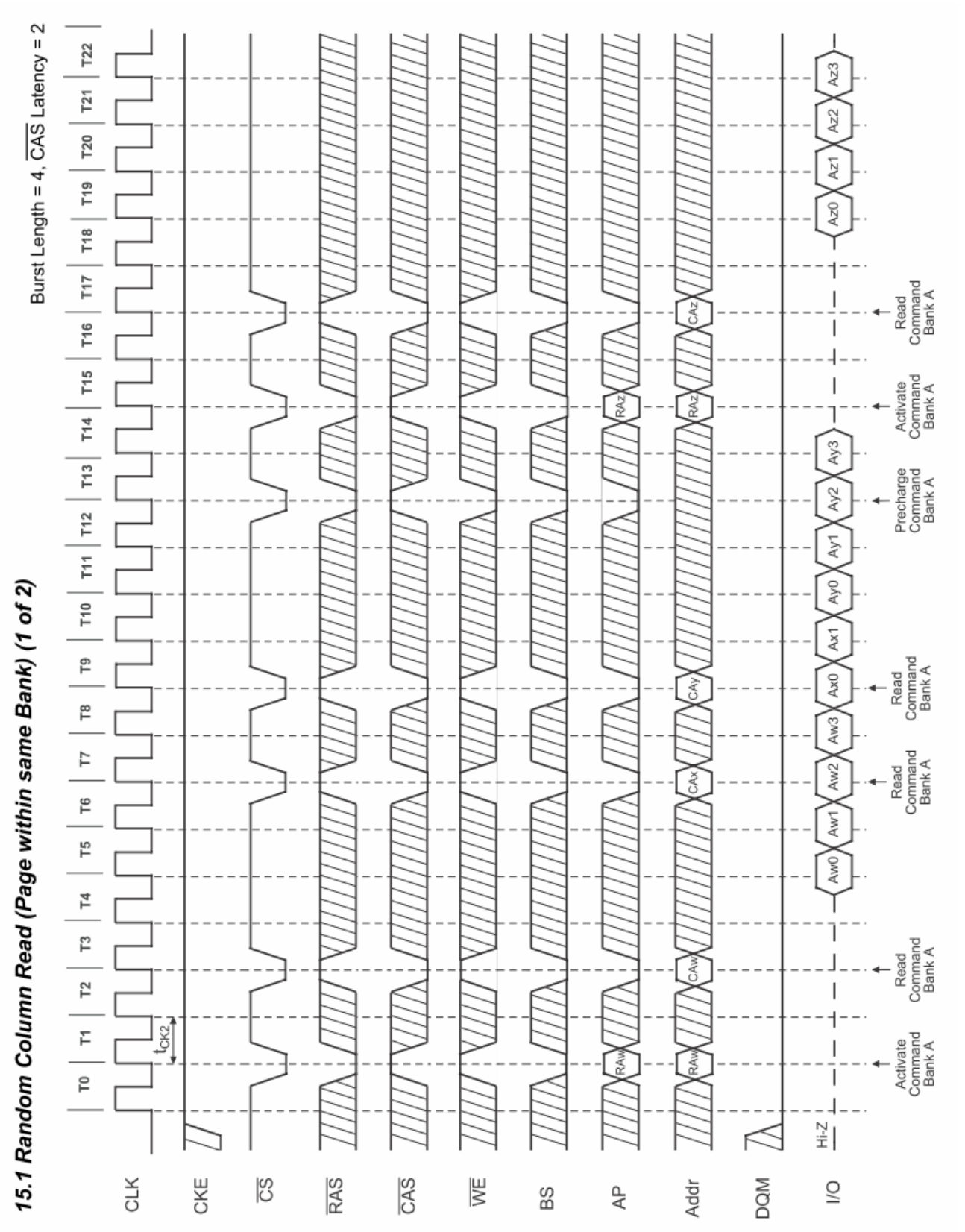
### 13. Self Refresh (Entry and Exit)



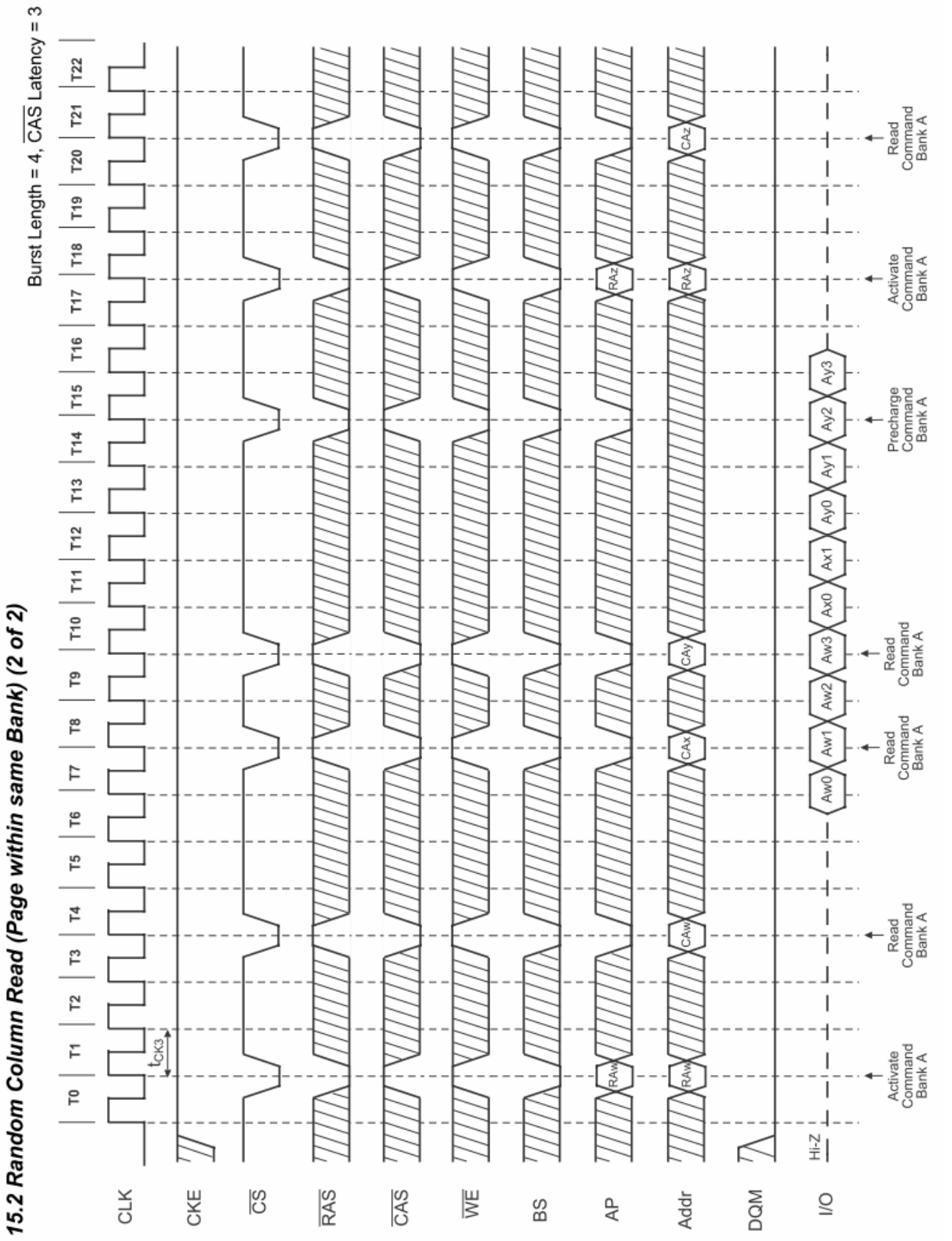
## 14. Auto Refresh (CBR)



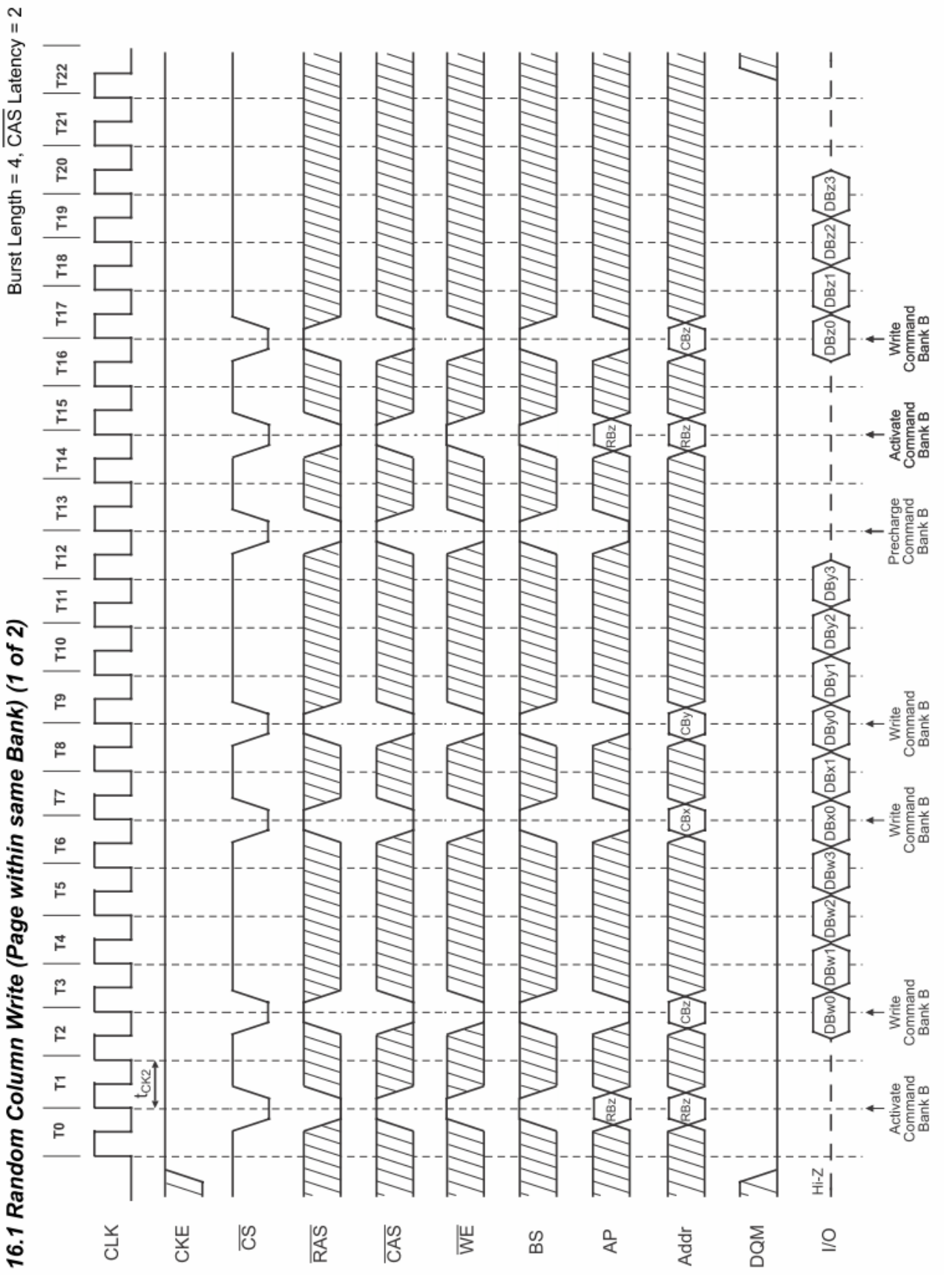
### 15.1 Random Column Read (Page within same Bank) (1 of 2)



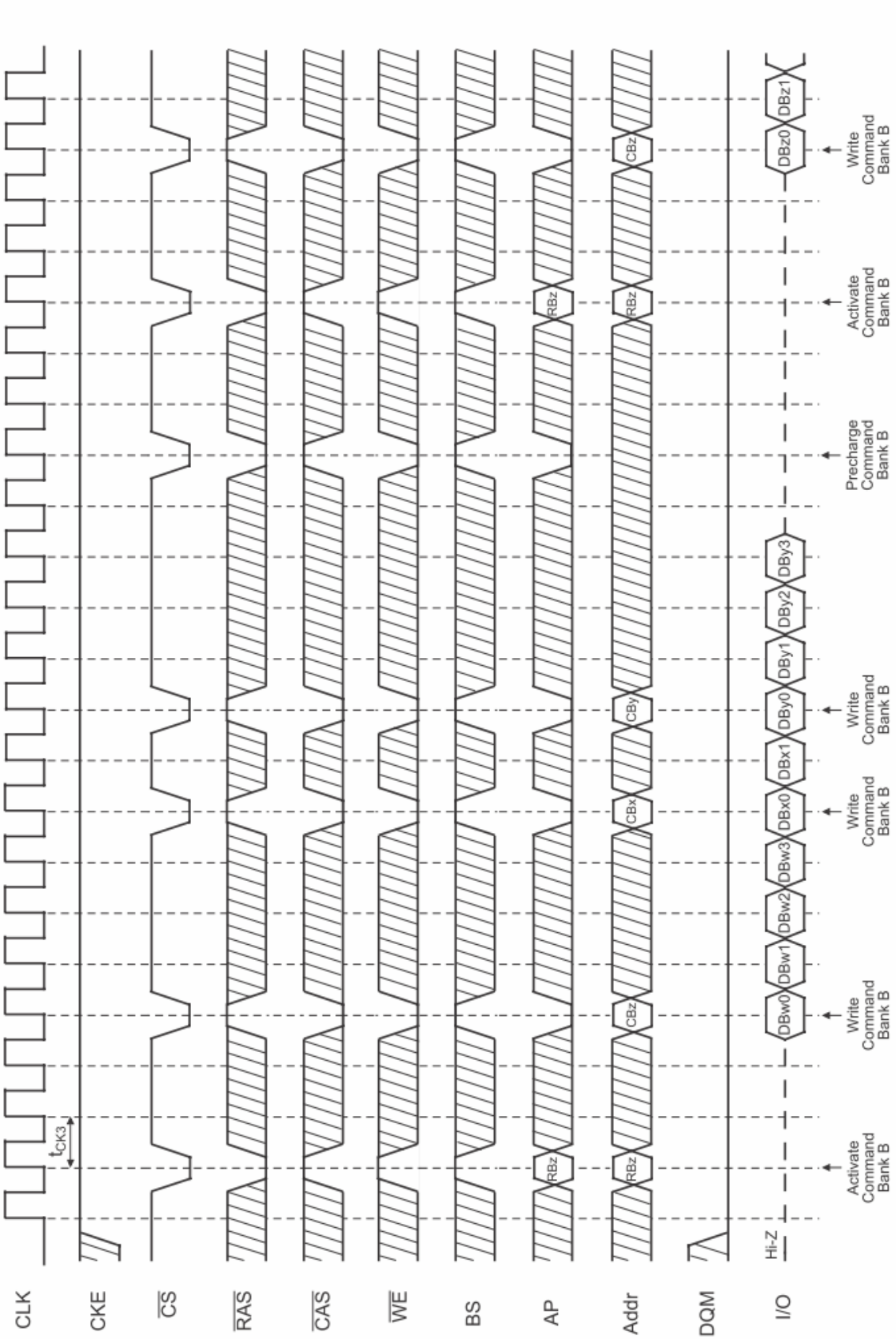
## 15.2 Random Column Read (Page within same Bank) (2 of 2)



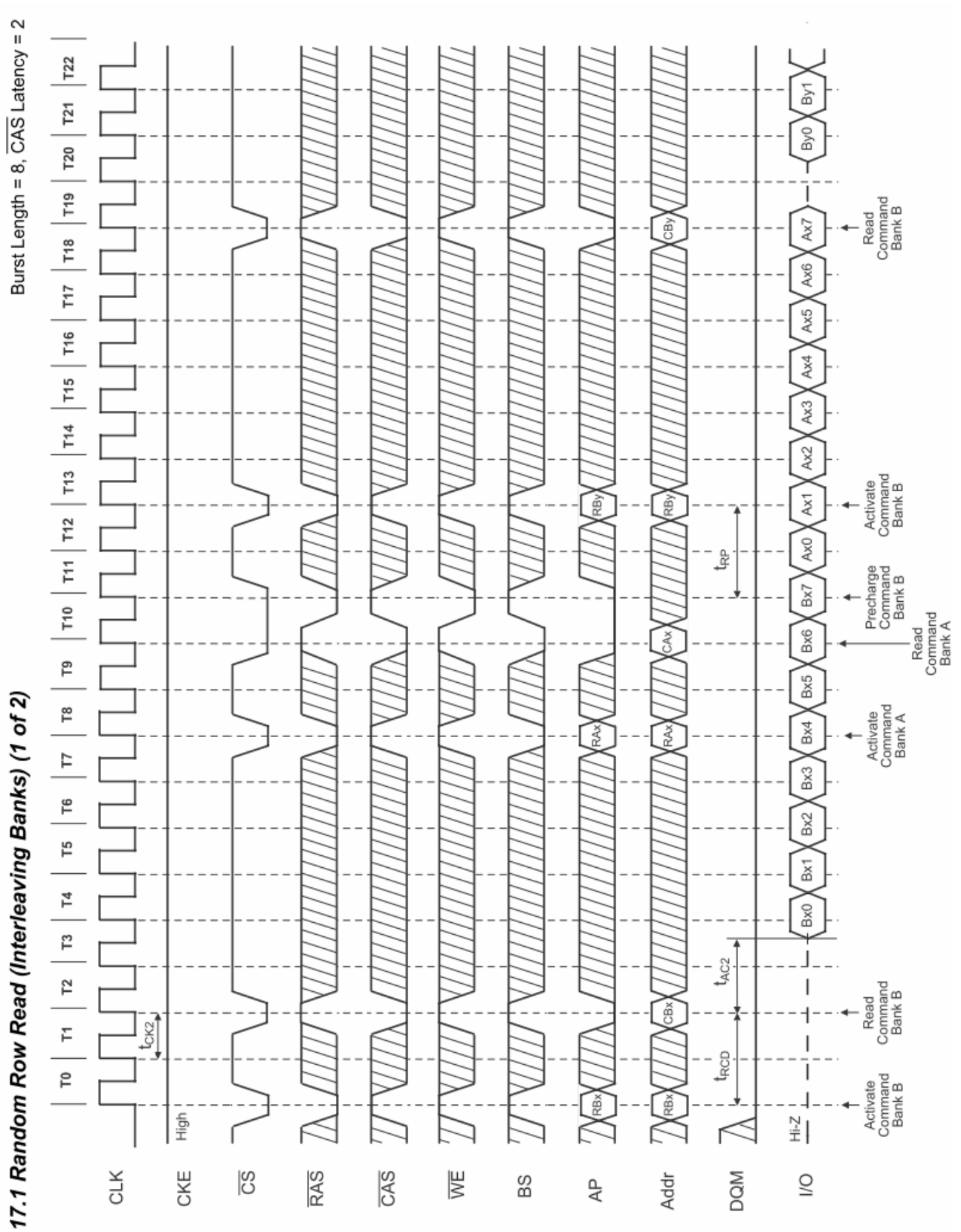
### 16.1 Random Column Write (Page within same Bank) (1 of 2)



### 16.2 Random Column Write (Page within same Bank) (2 of 2)

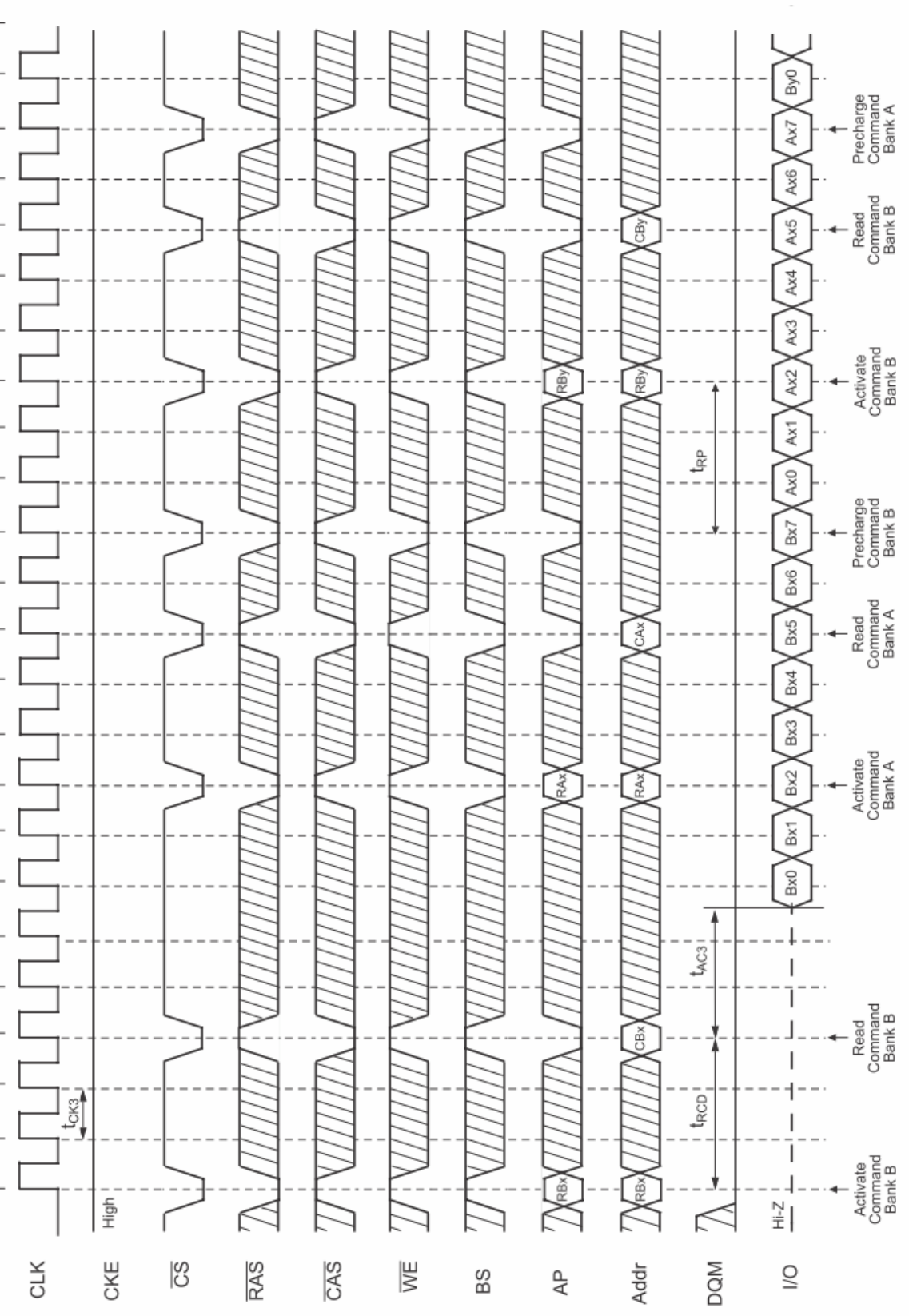


### 17.1 Random Row Read (Interleaving Banks) (1 of 2)

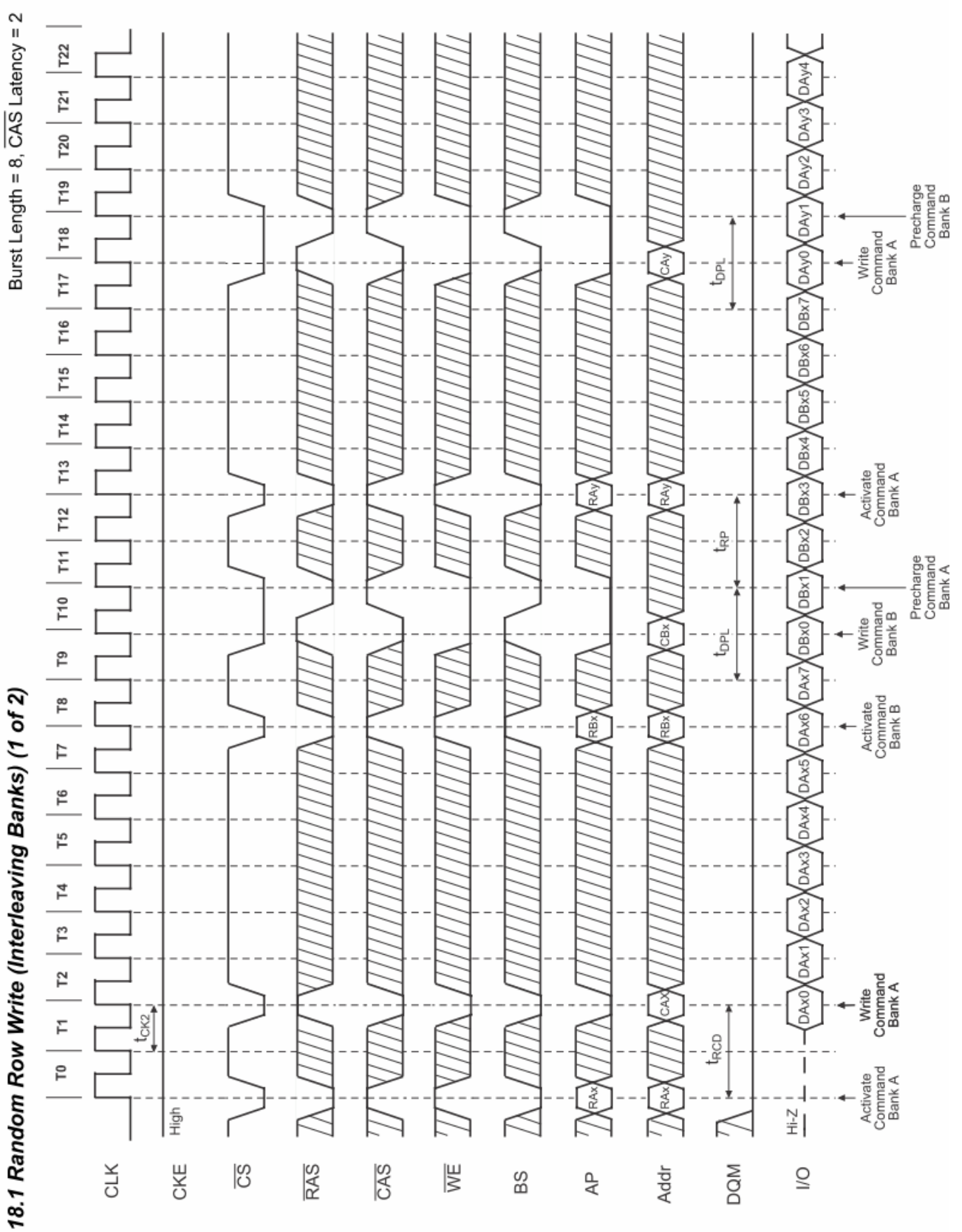


## 17.2 Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3

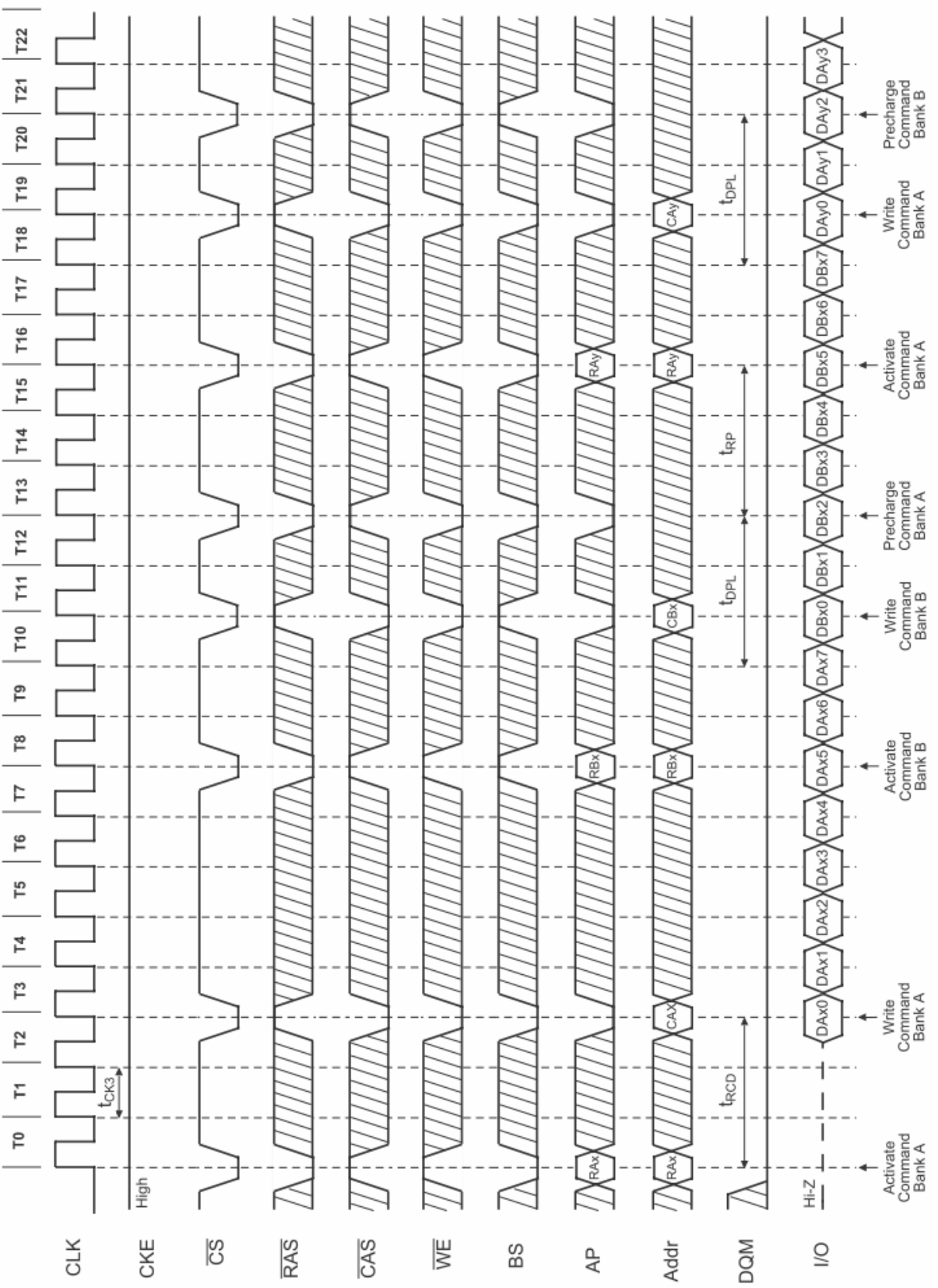


### 18.1 Random Row Write (Interleaving Banks) (1 of 2)

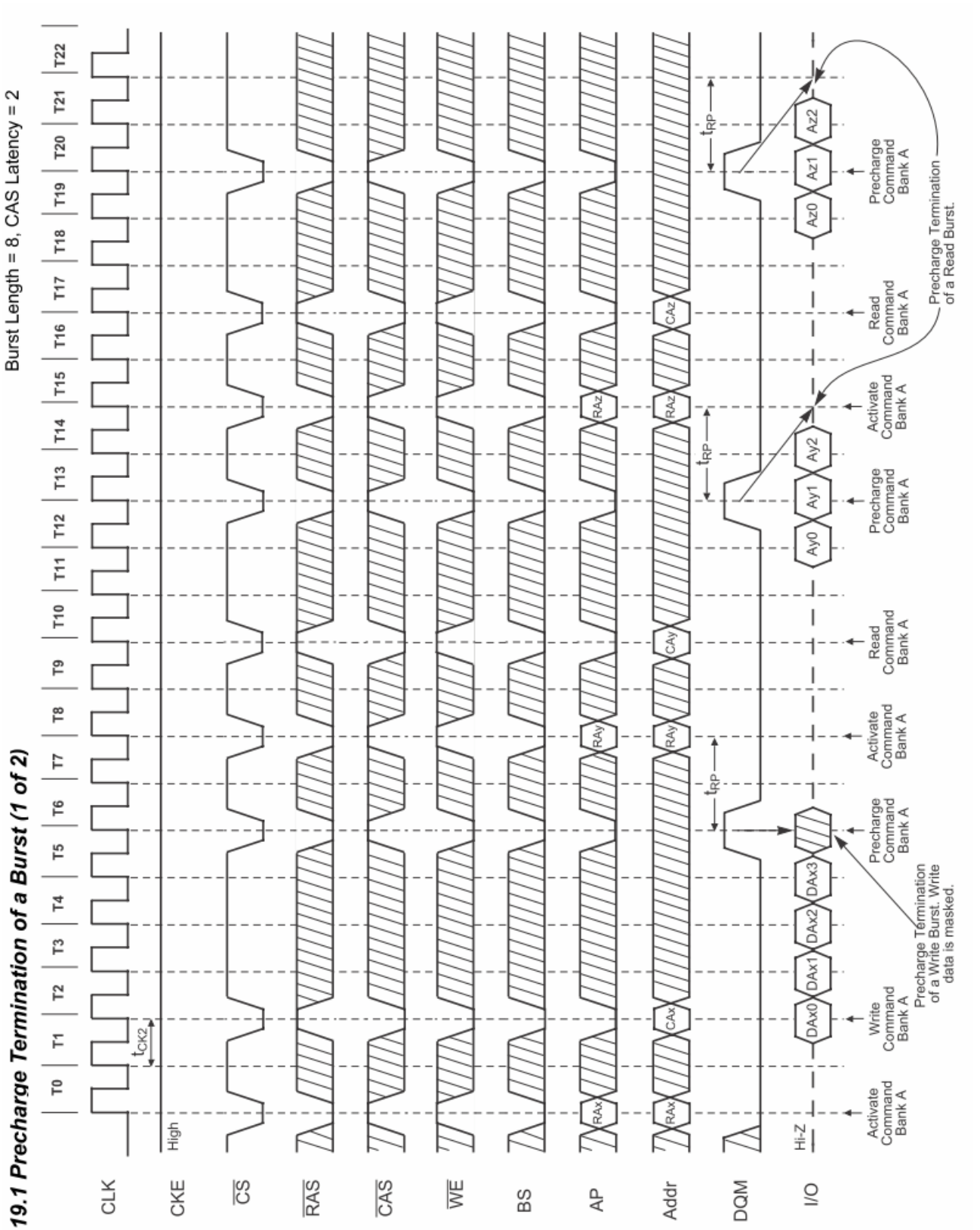


## 18.2 Random Row Write (Interleaving Banks) (2 of 2)

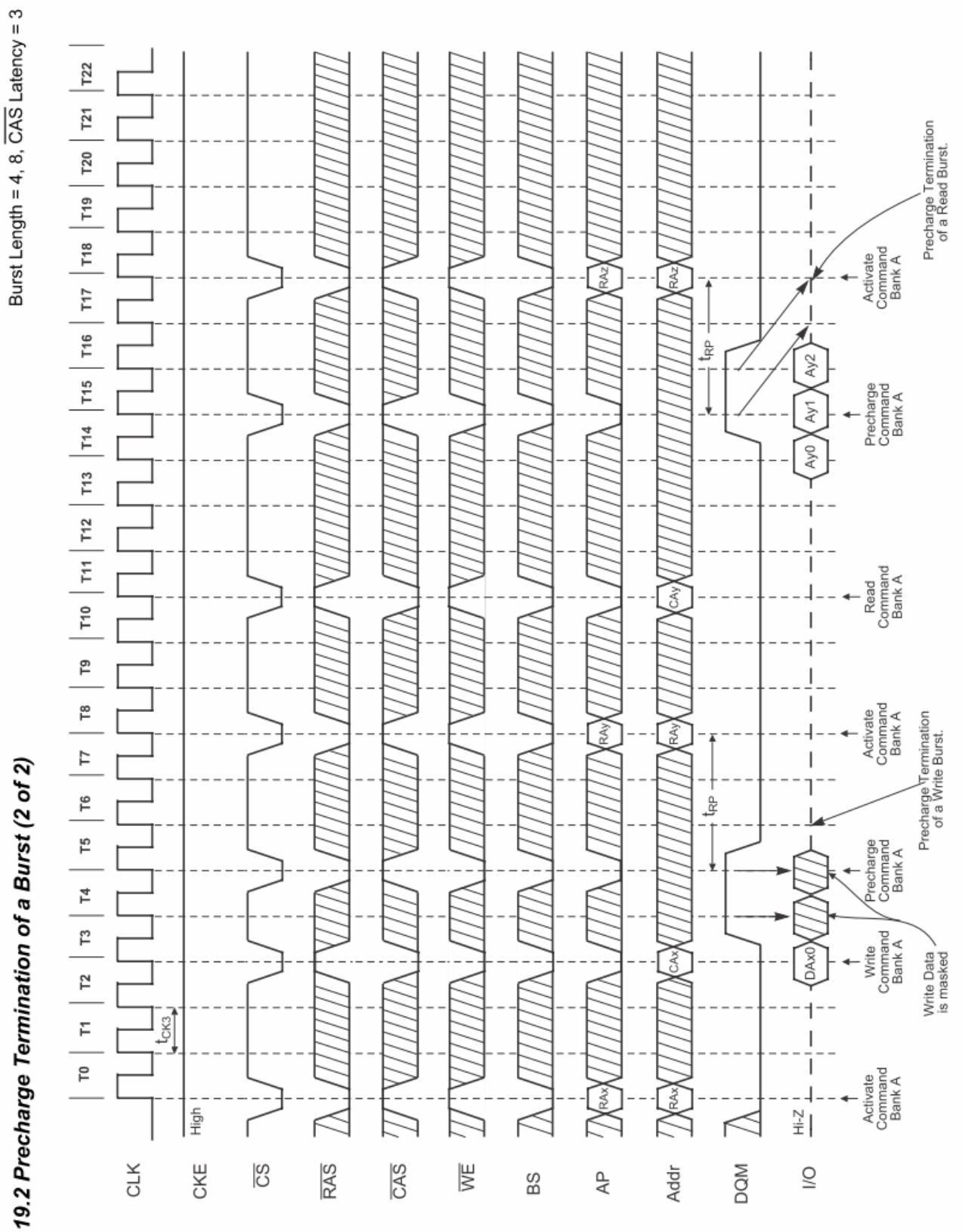
Burst Length = 8, $\overline{CAS}$ Latency = 3



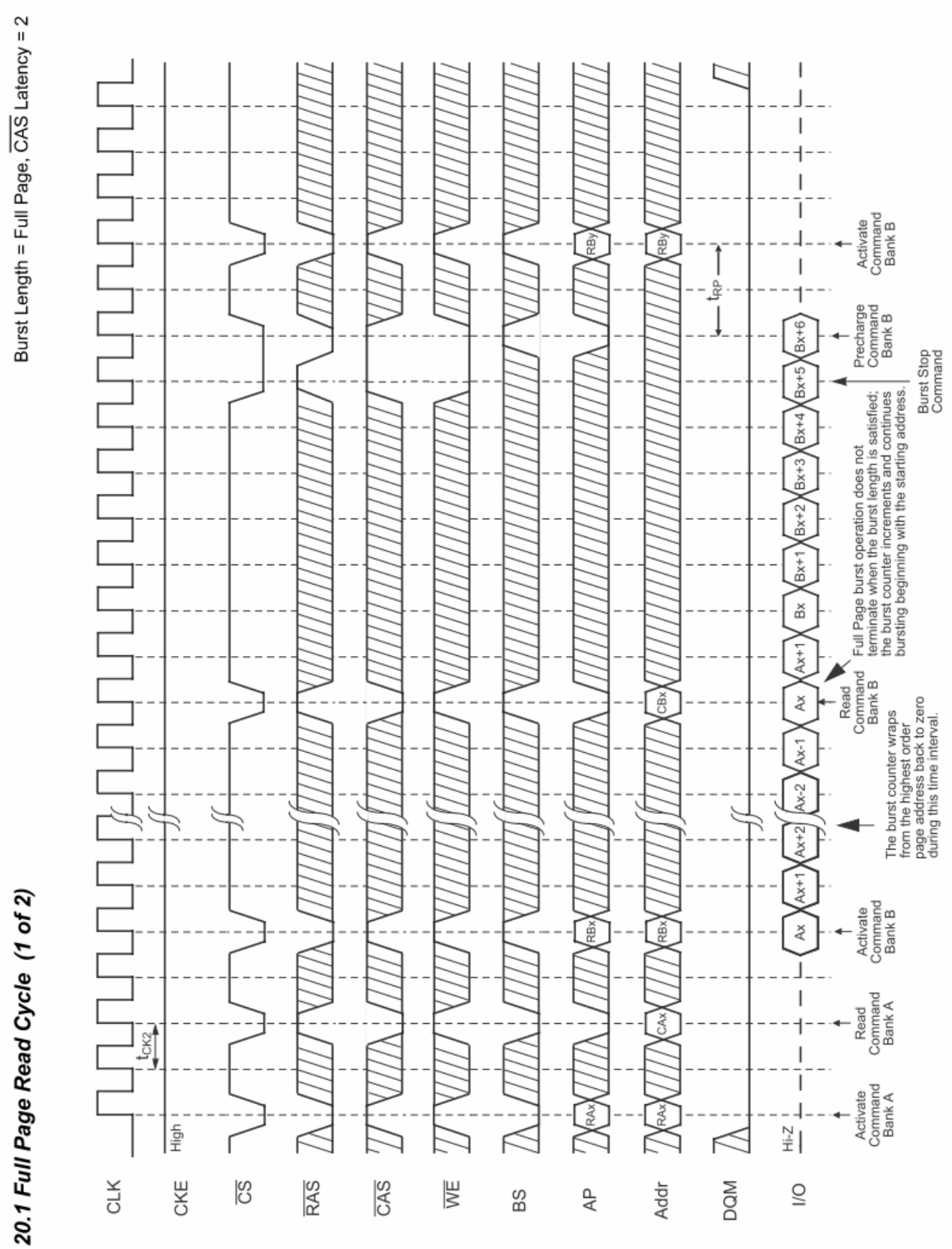
## 19.1 Precharge Termination of a Burst (1 of 2)



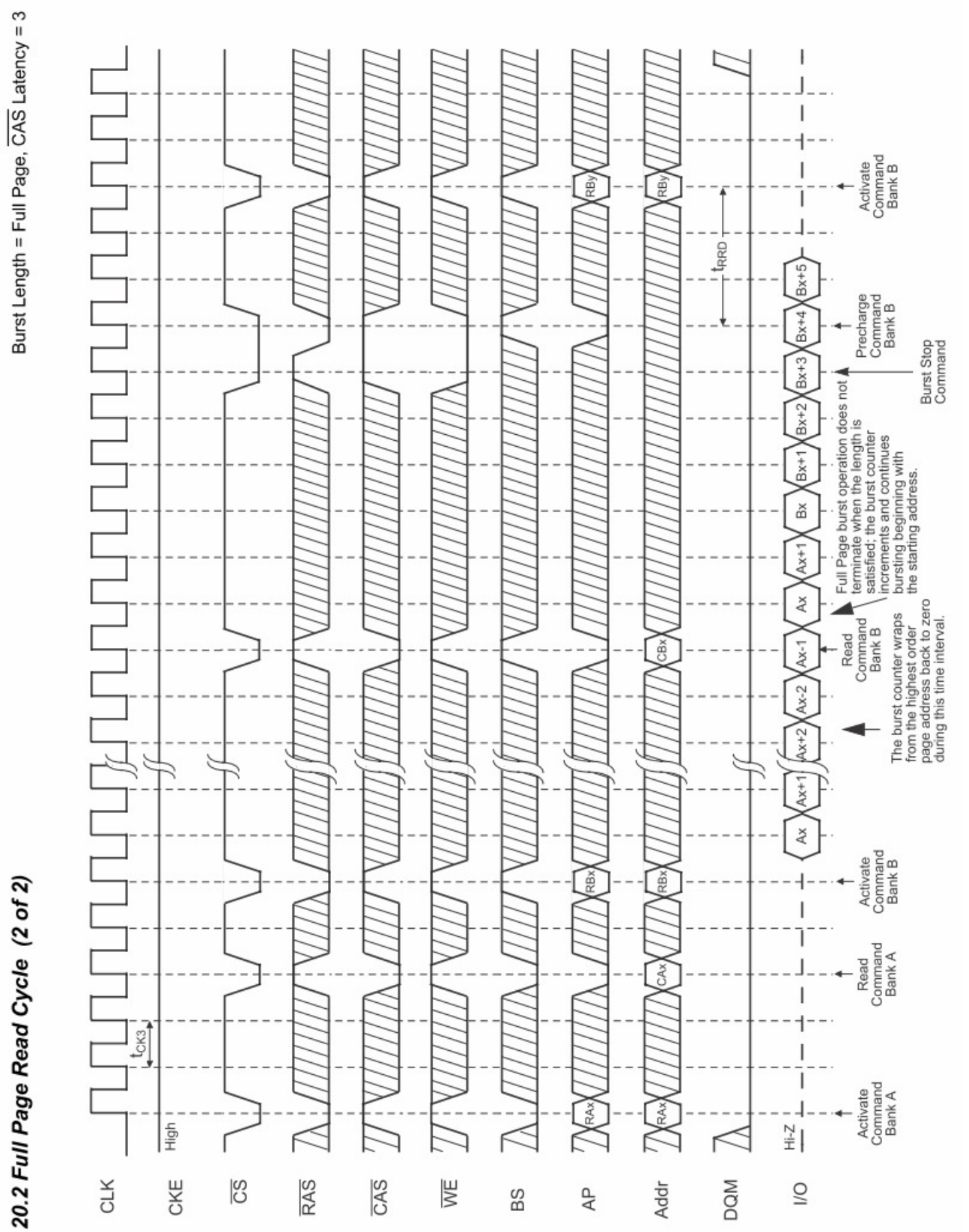
### 19.2 Precharge Termination of a Burst (2 of 2)



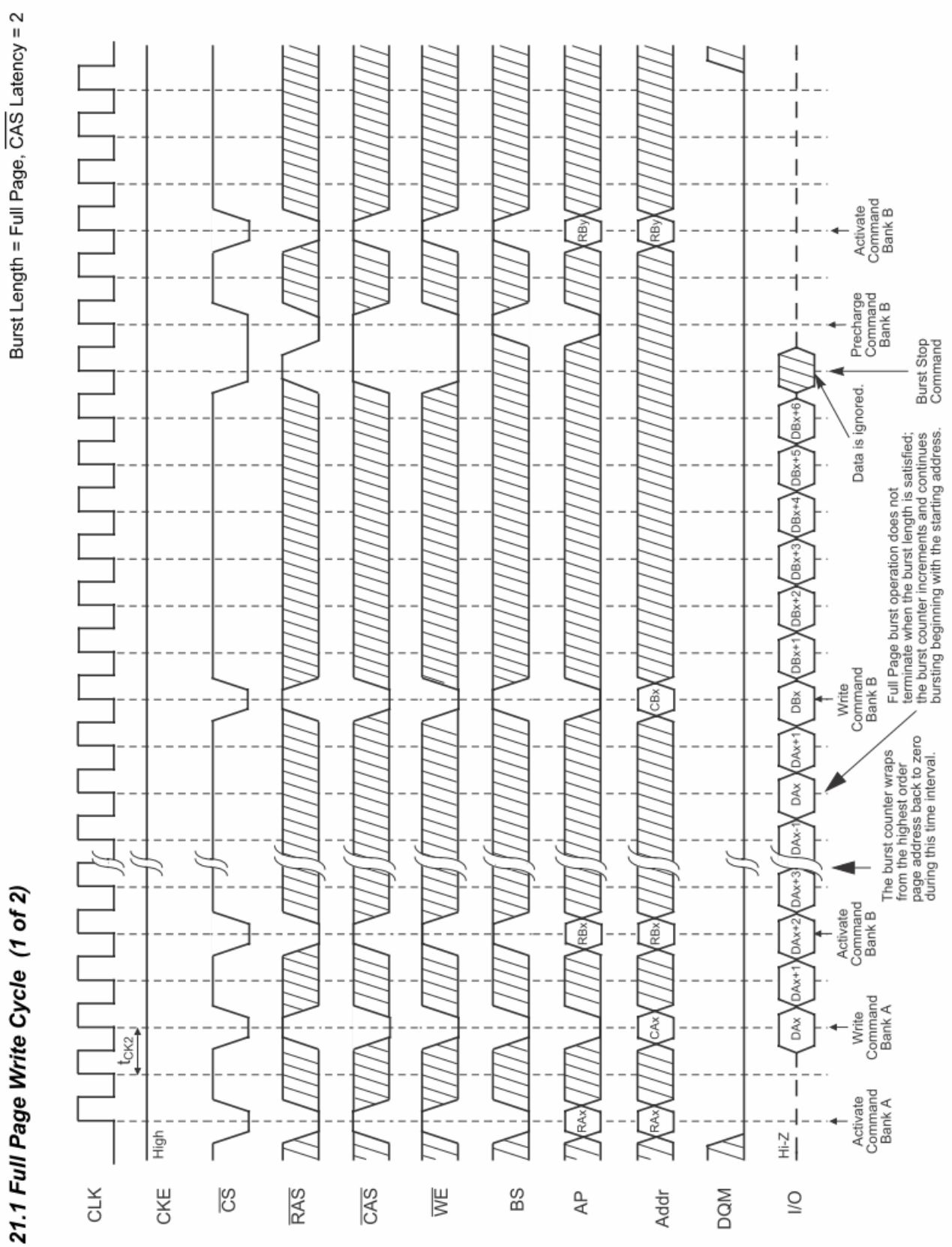
## 20.1 Full Page Read Cycle (1 of 2)



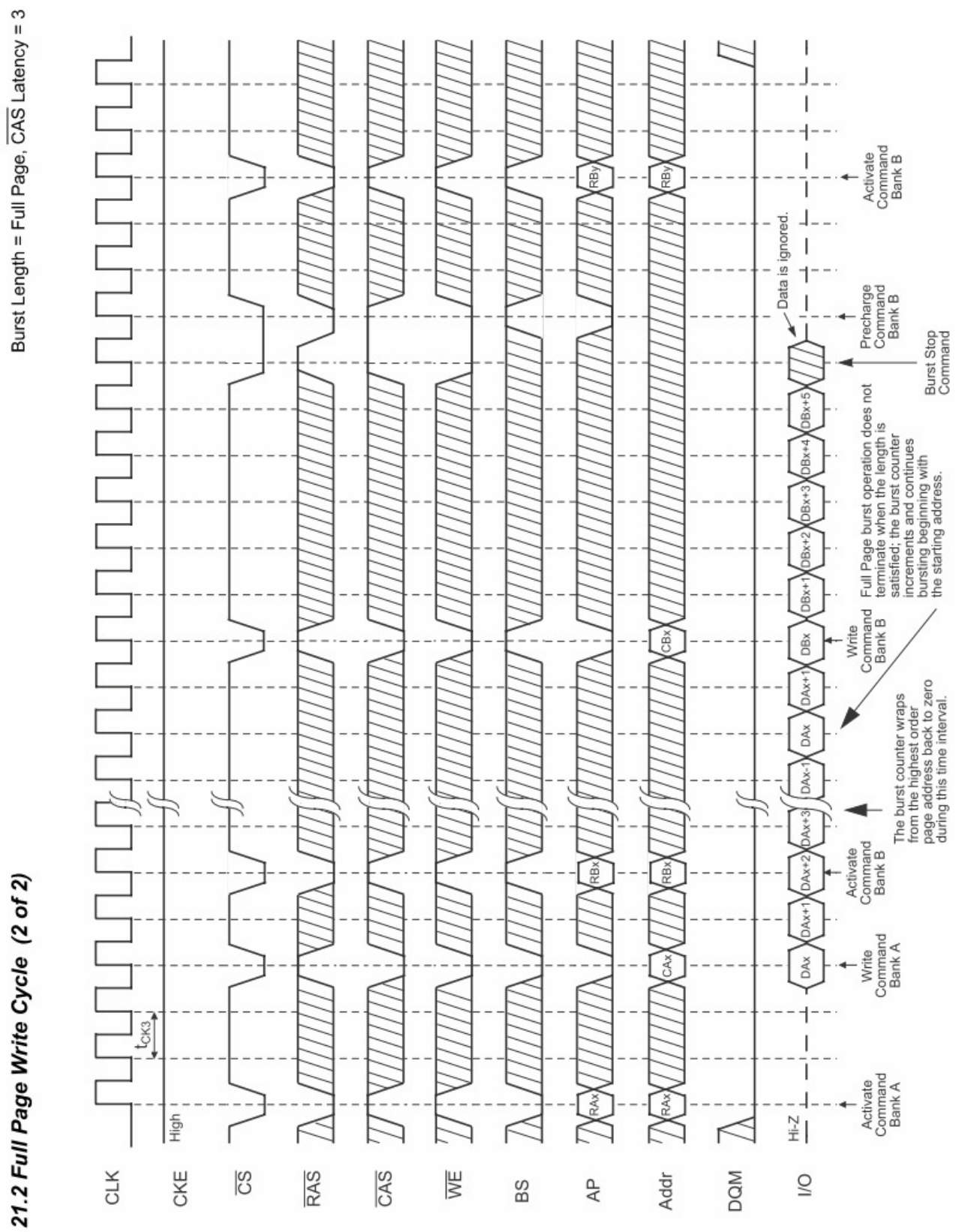
## 20.2 Full Page Read Cycle (2 of 2)



## 21.1 Full Page Write Cycle (1 of 2)



## 21.2 Full Page Write Cycle (2 of 2)



## *Complete List of Operation Commands*

### *SDRAM Function Truth Table*

| CURRENT STATE[1] | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BS | Addr | ACTION |
|---|---|---|---|---|---|---|---|
| Idle | H | X | X | X | X X | X | NOP or Power Down |
| | L | H | H | H | BS | X | NOP |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | RA | Row (&Bank) Active; Latch Row Address |
| | L | L | H | L | X | AP | NOP[4] |
| | L | L | L | H | Op- | X | Auto-Refresh or Self-Refresh[5] |
| | L | L | L | L | | Code | Mode reg. Access[5] |
| Row Active | H | X | X | X | X X | X X | NOP |
| | L | H | H | X | BS | CA,AP | NOP |
| | L | H | L | H | BS | CA,AP | Begin Read; Latch CA; DetermineAP |
| | L | H | L | L | BS | X | Begin Write; Latch CA; DetermineAP |
| | L | L | H | H | BS | AP | ILLEGAL[2] |
| | L | L | H | L | X | X | Precharge |
| | L | L | L | X | | | ILLEGAL |
| Read | H | X | X | X | X X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | H | BS | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | L | BS | X | Burst Stop Command > Row Active |
| | L | H | L | H | BS | CA,AP | Term Burst, New Read, DetermineAP[3] |
| | L | H | L | L | BS | CA,AP | Term Burst, Start Write, DetermineAP[3] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | X | AP | Term Burst, Precharge |
| | L | L | L | X | | X | ILLEGAL |
| Write | H | X | X | X | X X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | H | BS | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | L | BS | X | Burst Stop Command > Row Active |
| | L | H | L | H | BS | CA,AP | Term Burst, Start Read, DetermineAP[3] |
| | L | H | L | L | BS | CA,AP | Term Burst, New Write, DetermineAP[3] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | X | AP | Term Burst, Precharge[3] |
| | L | L | L | X | | X | ILLEGAL |
| Read with Auto Precharge | H | X | X | X | X X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | H | BS | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | H | X | X | ILLEGAL[2] |
| | L | H | L | L | BS | X | ILLEGAL |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | X | AP | ILLEGAL[2] |
| | L | L | L | X | | X | ILLEGAL |

### *SDRAM Function Truth Table (continued)*

| CURRENT STATE[1] | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BS | Addr | ACTION |
|---|---|---|---|---|---|---|---|
| Write | H | X | X | X | X X | X | NOP (Continue Burst to End;> Precharge) |
| with | L | H | H | H | BS | X | NOP (Continue Burst to End;> Precharge) |
| Auto | L | H | H | L | BS | X | ILLEGAL[2] |
| Precharge | L | H | L | H | X | X | ILLEGAL[2] |
| | L | H | L | L | BS | X | ILLEGAL |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | X | AP | ILLEGAL[2] |
| | L | L | L | X | | X | ILLEGAL |
| Precharging | H | X | X | X | X X | X | NOP;> Idle after tRP |
| | L | H | H | H | BS | X | NOP;> Idle after tRP |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | X | AP | NOP[4] |
| | L | L | L | X | | X | ILLEGAL |
| Row | H | X | X | X | X X | X | NOP;> Row Active after tRCD |
| Activating | L | H | H | H | BS | X | NOP;> Row Active after tRCD |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | X | AP | ILLEGAL[2] |
| | L | L | L | X | | X | ILLEGAL |
| Write | H | X | X | X | X X | X | NOP NOP |
| Recovering | L | H | H | H | BS | X | ILLEGAL[2] |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | X | AP | ILLEGAL |
| | L | L | L | X | | X | |
| Refreshing | H | X | X | X | X | X | NOP;> Idle after tRC |
| | L | H | H | H | X | X | NOP;> Idle after tRC |
| | L | H | H | L | X | X | ILLEGAL |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | H | X | X | X | ILLEGAL |
| | L | L | L | X | X | X | ILLEGAL |
| Mode | H | X | X | X | X | X | NOP |
| Register | L | H | H | H | X | X | NOP |
| | L | H | H | L | X | X | ILLEGAL |
| Accessing | L | H | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | ILLEGAL |

## *Clock Enable (CKE) Truth Table:*

| STATE(n) | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | ACTION |
|---|---|---|---|---|---|---|---|---|
| Self-Refresh[6] | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | EXIT Self-Refresh, Idle after tRC |
| | L | H | L | H | H | H | X | EXIT Self-Refresh, Idle after tRC |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP (Maintain Self-Refresh) |
| Power-Down | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | EXIT Power-Down, > Idle. |
| | L | H | L | H | H | H | X | EXIT Power-Down, > Idle. |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP (Maintain Low-Power Mode) |
| All. Banks Idle[7] | H | H | X | X | X | X | X | Refer to the function truth table |
| | H | L | H | X | X | X | X | Enter Power- Down |
| | H | L | L | H | H | H | X | Enter Power- Down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | H | X | X | ILLEGAL |
| | H | L | L | L | L | H | X | Enter Self-Refresh |
| | H | L | L | L | L | L | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP |

Abbreviations:

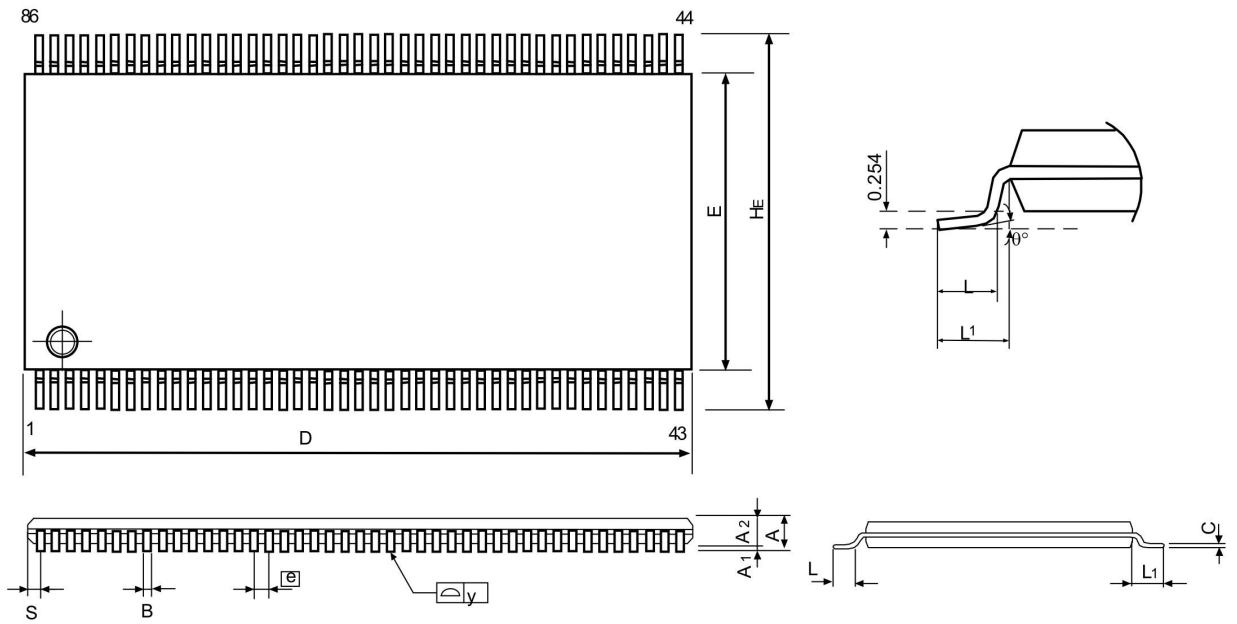
RA = Row Address of Bank A
CA = Column Address of Bank A
BS = Bank Address
RB = Row Address of Bank B
CB = Column Address of Bank B
AP = Auto Precharge
RC = Row Address of Bank C
CC = Column Address of Bank C
RD = Row Address of Bank D
CD = Column Address of Bank D

**Notes for SDRAM function truth table:**

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. May precharge bank(s) indicated by BS (andAP).
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.

## *Package Diagram*

### 86-Pin TSOP II Package Outline Drawing Information



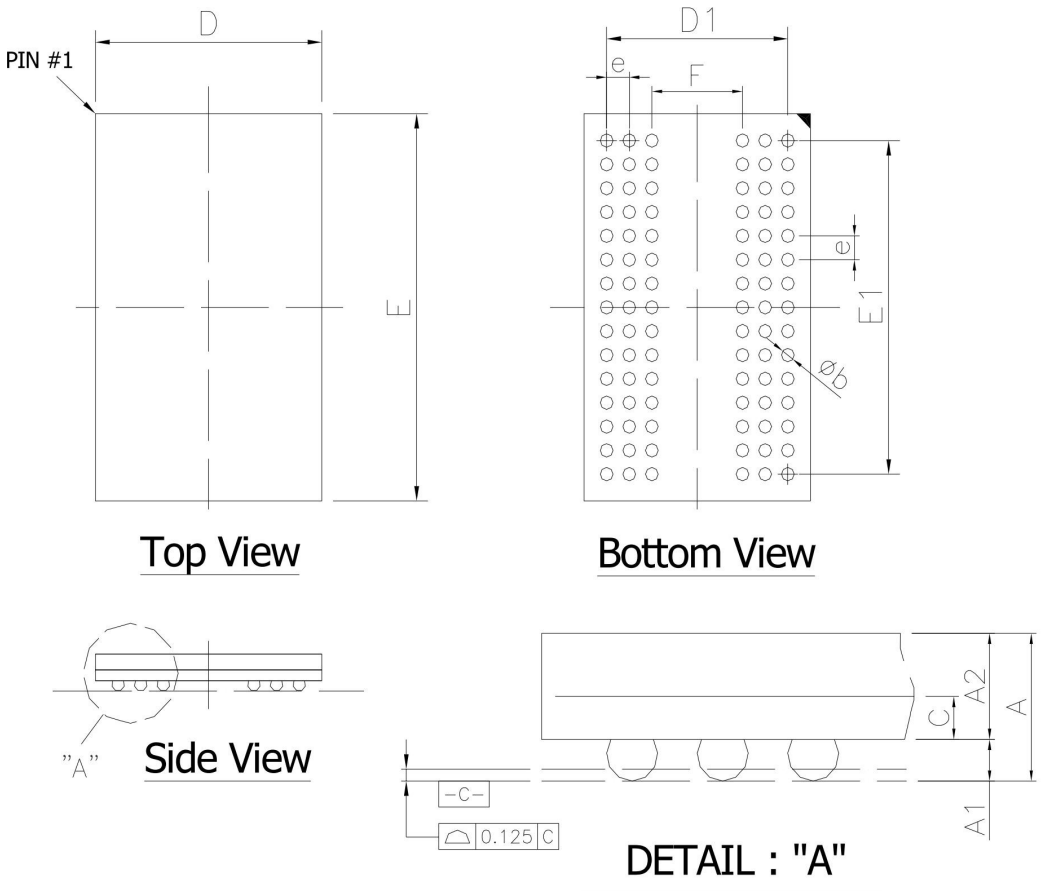

| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Normal | Max | Min | Normal | Max |
| A | — | — | 0.047 | — | — | 1.20 |
| A1 | 0.002 | 0.004 | 0.008 | 0.05 | 0.10 | 0.2 |
| A2 | 0.035 | 0.039 | 0.043 | 0.9 | 1 | 1.1 |
| B | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| C | — | 0.005 | — | — | 0.127 | — |
| D | 0.87 | 0.875 | 0.88 | 22.09 | 22.22 | 22.35 |
| E | 0.395 | 0.400 | 0.405 | 10.03 | 10.16 | 10.29 |
| e | — | 0.0197 | — | — | 0.50 | — |
| HE | 0.455 | 0.463 | 0.471 | 11.56 | 11.76 | 11.96 |
| L | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 | 0.60 |
| L1 | — | 0.0315 | — | — | 0.80 | — |
| S | — | 0.024 | — | — | 0.61 | — |
| y | — | — | 0.004 | — | — | 0.10 |
| θ | 0° | — | 8° | 0° | — | 8° |

**Notes:**

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.
4. Controlling dimension: mm

## *Package Diagram*

### 90 Ball FBGA 8x13x.2mm (Max.) Outline Drawing Information




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | -- | -- | 0.047 | -- | -- | 1.20 |
| A1 | 0.012 | 0.014 | 0.016 | 0.30 | 0.35 | 0.40 |
| A2 | 0.027 | 0.029 | 0.031 | 0.69 | 0.74 | 0.79 |
| C | 0.007 | 0.008 | 0.010 | 0.17 | 0.21 | 0.25 |
| D | 0.311 | 0.315 | 0.319 | 7.90 | 8.00 | 8.10 |
| E | 0.508 | 0.512 | 0.516 | 12.90 | 13.00 | 13.10 |
| D1 | -- | 0.252 | -- | -- | 6.40 | -- |
| E1 | -- | 0.441 | -- | -- | 11.2 | -- |
| e | -- | 0.031 | -- | -- | 0.80 | -- |
| b | 0.016 | 0.018 | 0.020 | 0.40 | 0.45 | 0.50 |
| F | -- | 0.126 | -- | -- | 3.2 | -- |

## *Revision History*

| Rev. | History | Draft Date | Remark |
|---|---|---|---|
| 1.0 | Initial release | Aug. 2015 | |
| 2.0 | 1. Amend the VDD and VDDQ voltage information on Pin Name table (P3 and P4)<br>2. Change the Pin names of VCC and VCCQ to VDD and VDDQ respectively | Oct. 2018 | |