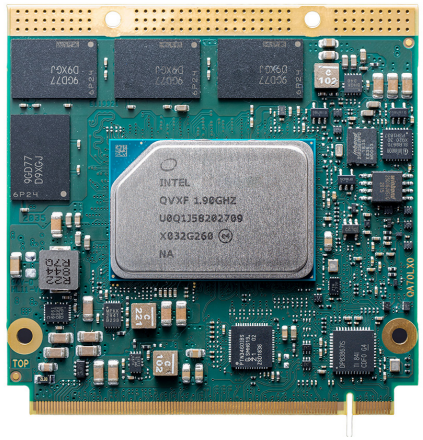

Qseven® conga-QA7

Qseven 2.1 module based on Intel® Atom®, Pentium® and Celeron® Elkhart Lake SoC

User's Guide

Revision 0.3 (Preliminary)

congatec

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2021.05.28	BEU	• Preliminary release
0.2	2021.06.08	BEU	• Added software license information to preface section • Changed connector name to TMDS in table 23
0.3	2021.06.16	BEU	• Updated feature descriptions in table 3 and section 3 "Block Diagram"

Preface

This user's guide provides information about the components, features, connectors, and BIOS available on the conga-QA7. It is one of three documents that should be referred to when designing a Qseven® application.

The other reference documents that should be used include the following:

Qseven® Design Guide 2.0
Qseven® Specification 2.1

The links to the Qseven® documents can be found on the SGET e.V. website at www.sget.org

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Caution

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Note

Notes call attention to important information that should be observed.

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Contents

List of Tables

Terminology

Term	Description
PCIe	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8, or x16 link.
eMMC	Embedded MultiMediaCard
SD card	Secure Digital card is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
DDI	Digital Display Interface
DP	DisplayPort is a VESA open digital communications interface.
LPC	Low Pin-Count is a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SMBus	System Management Bus is a popular derivative of the I²C-bus.
SPI	Serial Peripheral Interface is a synchronous serial data link standard that operates in full duplex mode.
GbE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C	Not connected
N.A	Not available
TBD	To be determined

1 Introduction

1.1 Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Computer-On-Module that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The conga-QEVAL/Qseven 2.0 evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose those suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

1.2 conga-QA7 Options Information

The conga-QA7 is available in eight variants (five commercial and three industrial). The tables below show the different configurations available.

Table 1 conga-QA7 (Commercial Variants)

PN	015800	015801	015802	015820	015821
Processor	Intel® Atom® x6425E	Intel® Atom® x6413E	Intel® Atom® x6211E	Intel® Pentium® J6426	Intel® Celeron® J6413
- Cores	4	4	2	4	4
- Base Frequency	2.0 GHz	1.5 GHz	1.3 GHz	2.0 GHz	1.8 GHz
- Burst Frequency	3.0 GHz	3.0 GHz	3.0 GHz	3.0 GHz	3.0 GHz
- TDP	12 W	9 W	6 W	10 W	10 W
Graphics	Intel® UHD Graphics	Intel® UHD Graphics	Intel® UHD Graphics	Intel® UHD Graphics	Intel® UHD Graphics
- Execution Units	32	16	16	32	16
- Base Frequency	500 MHz	500 MHz	350 MHz	400 MHz	400 MHz
- Burst Frequency	750 MHz	750 MHz	750 MHz	850 MHz	800 MHz
Memory	16 GB	8 GB	4 GB	16 GB	8 GB
- Type	LPDDR4x	LPDDR4x	LPDDR4x	LPDDR4x	LPDDR4x
- Speed	3200 MT/s	3200 MT/s	3200 MT/s	3200 MT/s	3733 MT/s
- ECC	In-band	In-band	In-band	N.A	N.A
eMMC	64 GB	32 GB	32 GB	64 GB	32 GB
- Version	eMMC 5.1	eMMC 5.1	eMMC 5.1	eMMC 5.1	eMMC 5.1

Table 2 conga-QA7 (Industrial Variants)

PN	015810	015811	015812
Processor	Intel® Atom® x6425RE	Intel® Atom® x6414RE	Intel® Atom® x6212RE
- Cores	4	4	2
- Base Frequency	1.9 GHz	1.5 GHz	1.2 GHz
- Burst Frequency	N.A	N.A	N.A
- TDP	12 W	9 W	6 W
Graphics	Intel® UHD Graphics	Intel® UHD Graphics	Intel® UHD Graphics
- Execution Units	32	16	16
- Base Frequency	400 MHz	400 MHz	350 MHz
- Burst Frequency	N.A	N.A	N.A
Memory	8 GB	4 GB	4 GB
- Type	LPDDR4x	LPDDR4x	LPDDR4x
- Speed	4267 MT/s	3200 MT/s	3200 MT/s
- ECC	In-band	In-band	In-band
eMMC	32 GB	32 GB	32 GB
- Version	eMMC 5.1	eMMC 5.1	eMMC 5.1

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Qseven Form Factor; Qseven Spec. Rev. 2.1 compliant; 70 x 70 mm	
CPU	Intel® Atom®, Pentium® and Celeron® Elkhart Lake	
DRAM	Max. 16 GB onboard LPDDR4x; up to 4267 MT/s	
Ethernet	Intel® GbE with TSN support and Out-Of-Band Management; Real-time trigger	
I/O Interfaces	Up to 2x USB 3.1 Gen 2 Up to 1x USB3.1 Dual Role Up to 8x USB 2.0 2x SATA III SDIO 4x PCIe Gen3	I²C Bus SMBus SPI (option) UART CAN LPC
Mass Storage	eMMC 5.1 onboard flash up to 64 Gbyte (optional up to 256 Gbyte)	
Audio	Intel® HD Audio	
Graphics	Intel® UHD Graphics (Gen11 LP)	
LVDS	18/24-bit Single/Dual Channel LVDS Interface, resolutions up to 1920X1200@60Hz, VESA standard or JEIDA data mapping, Automatic Panel Detection via EDID/EP; shared with eDP 1.3 supporting up to 4096x2160@60Hz (option) or MIPI-DSI 1.2 supporting up to 3200x2000@60Hz	
Digital Display Interface	Dual Mode DisplayPort 1.4 4096x2160@60Hz	
congatec Board Controller	Multistage watchdog; non-volatile user data storage; manufacturing and board Information; board statistics; fast mode and multi-master I²C bus; power loss control	
Embedded BIOS Feature	AMI Aptio® UEFI firmware; 32 Mbyte serial SPI with congatec Embedded BIOS features; OEM Logo; OEM CMOS Defaults; LCD Control; Display Auto Detection; Backlight Control; Flash Update	
Power Management	ACPI 5 .0 compliant; Smart Battery Management	
Operating Systems	Microsoft® Windows 10; Microsoft® Windows 10 IoT Enterprise; Linux (Yocto Project); Android; RTS Hypervisor	
Temperature Range	Commercial: Operating Temperature: 0 to +60°C Industrial: Operating Temperature: -40 to +85°C	Storage Temperature: -20 to +80°C Storage Temperature: -40 to +85°C
Humidity	Operating: 10 to 90% r. H. non cond. Storage: 5 to 95% r. H. non cond.	
Size	70 x 70 mm (approx. 2.75” x 2.75”)	

2.2 Supported Operating Systems

The conga-QA7 supports the following operating systems:

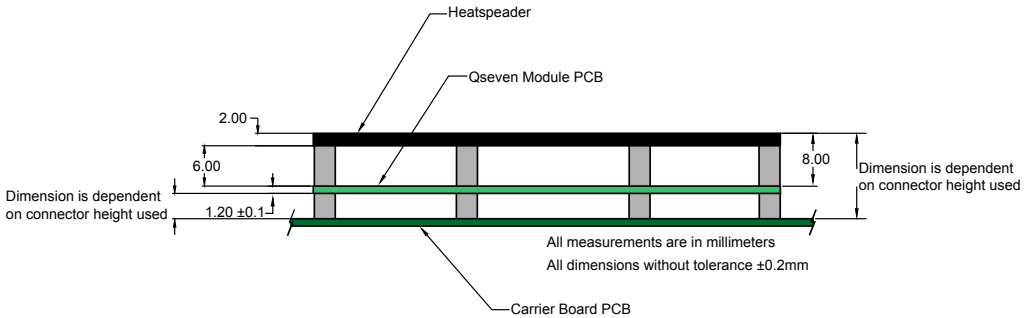
- Microsoft® Windows® 10
- Microsoft® Windows® IoT Enterprise
- Linux® (Yocto Project®)
- Android™
- RTS Hypervisor

Note

For the installation of Microsoft® Windows® 10 (64-bit), congatec GmbH recommends a minimum storage capacity of 20 GB. congatec will not offer technical support for systems with less than 20 GB storage capacity.

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm
- The Qseven® module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12 mm thick.

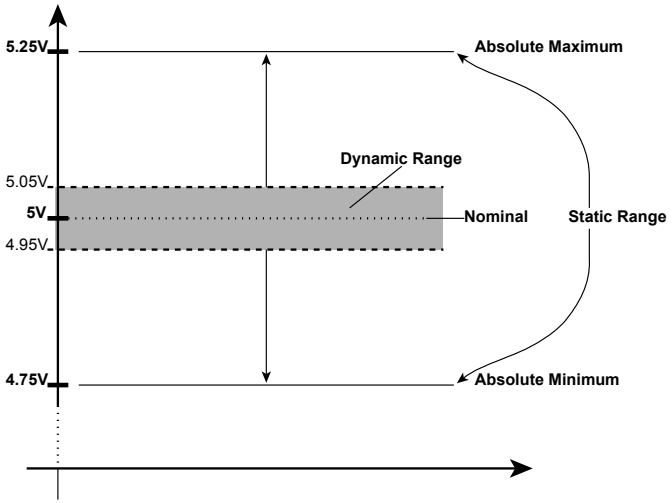


Rear View of Qseven Module

2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module, refer to the Qseven® specification.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-QA7 COM
- modified congatec carrier board
- conga-QA7 cooling solution
- Microsoft® Windows® 10 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool.

The power consumption values were recorded during the following system states:

Table 4 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

The tables below provide additional information about the power consumption data for each of the conga-QA7 variants offered. The values are recorded at various operating modes.

Table 5 Power Consumption Values

PN	RAM Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (A) @ 5V					
					Variant	Cores	Base / Burst Freq. (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
015800	16 GB	TBD	TBD	Windows® 10	Atom® x6425E	4	2.0 / 3.0	TBD	TBD	TBD	TBD	TBD	TBD
015801	8 GB	TBD	TBD	Windows® 10	Atom® x6413E	4	1.5 / 3.0	TBD	TBD	TBD	TBD	TBD	TBD
015802	4 GB	TBD	TBD	Windows® 10	Atom® x6211E	2	1.3 / 3.0	TBD	TBD	TBD	TBD	TBD	TBD
015810	8 GB	TBD	TBD	Windows® 10	Atom® x6425RE	4	1.9 / ---	TBD	TBD	TBD	TBD	TBD	TBD
015811	4 GB	TBD	TBD	Windows® 10	Atom® x6414RE	4	1.5 / ---	TBD	TBD	TBD	TBD	TBD	TBD
015812	4 GB	TBD	TBD	Windows® 10	Atom® x6212RE	2	1.2 / ---	TBD	TBD	TBD	TBD	TBD	TBD
015820	16 GB	TBD	TBD	Windows® 10	Pentium® J6426	4	2.0 / 3.0	TBD	TBD	TBD	TBD	TBD	TBD
015821	8 GB	TBD	TBD	Windows® 10	Celeron® J6413	4	1.8 /3.0	TBD	TBD	TBD	TBD	TBD	TBD

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 6 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	TBD µA
20°C	3V DC	TBD µA
70°C	3V DC	TBD µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-QA7.*

2.7 Environmental Specifications

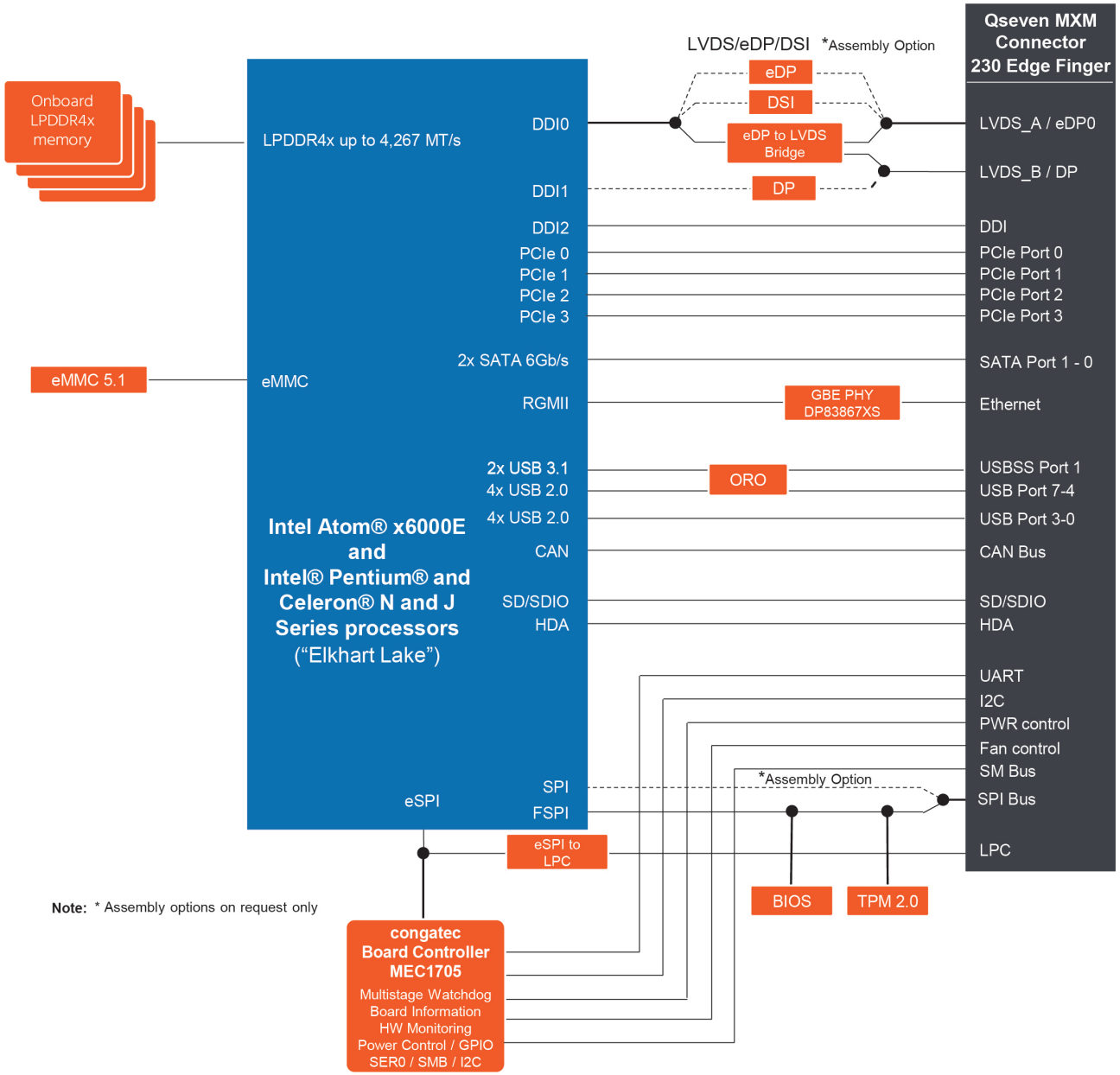
Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation:	-40° to 85°C	Storage: -40° to +85°C
Humidity	Operation:	10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



Note: * Assembly options on request only

4 Cooling Solutions

congatec GmbH offers the cooling solutions listed in the table below for conga-QA7. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 7 Cooling Solution Variants

Cooling Solution	PN	Description
HSP	015852	Heatspreader for conga-QA7 with open-die Intel Pentium/Celeron J and N processors. All standoffs are with 2.7mm bore hole.
	015856	Heatspreader for conga-QA7 with open-die Intel Pentium/Celeron J and N processors. All standoffs are M2.5mm threaded.
	015851	Heatspreader for conga-QA7 with lidded Intel Atom processor. All standoffs are with 2.7mm bore hole.
	015855	Heatspreader for conga-QA7 with lidded Intel Atom x6000E processors. All standoffs are M2.5mm threaded.
CSP	015853	Passive cooling solution for conga-QA7 with open-die Intel Pentium/Celeron processor. All standoffs are with 2.7mm bore hole.
	015857	Passive cooling solution for conga-QA7 with open-die Intel Pentium/Celeron J and N processors. All standoffs are M2.5mm threaded.
	015850	Passive cooling solution for conga-QA7 with lidded Intel Atom processor. All standoffs are with 2.7mm bore hole.
	015854	Passive cooling solution for conga-QA7 with lidded Intel Atom x6000E processors. All standoffs are M2.5mm threaded.

Note

1. *We recommend a maximum torque of 0.4 Nm for the mounting screws and to start with the two screws furthest from the CPU die.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

Caution

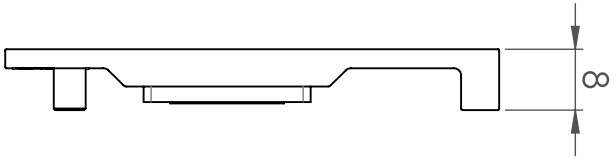
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

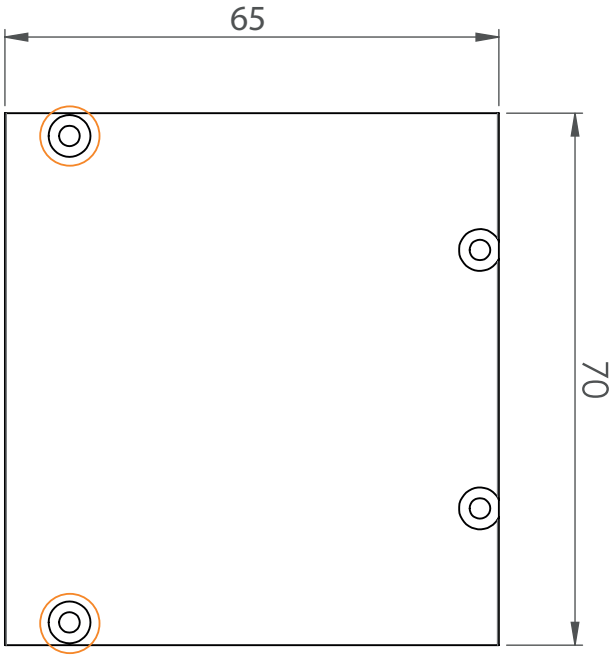
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

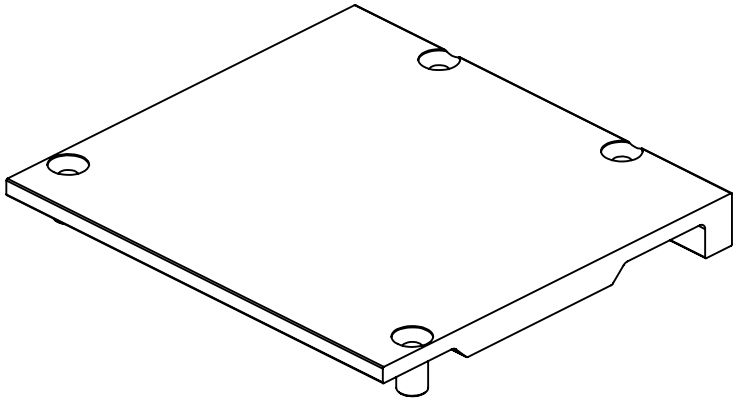
4.1 Heatspreader Dimensions

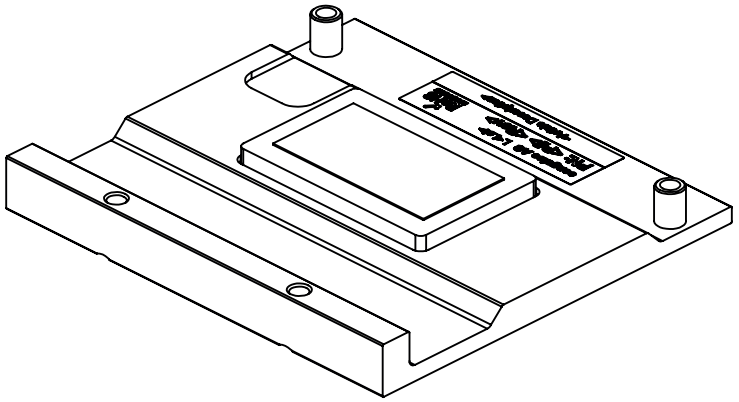
PN: 015852, 015856



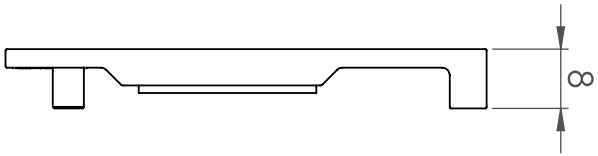
M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version



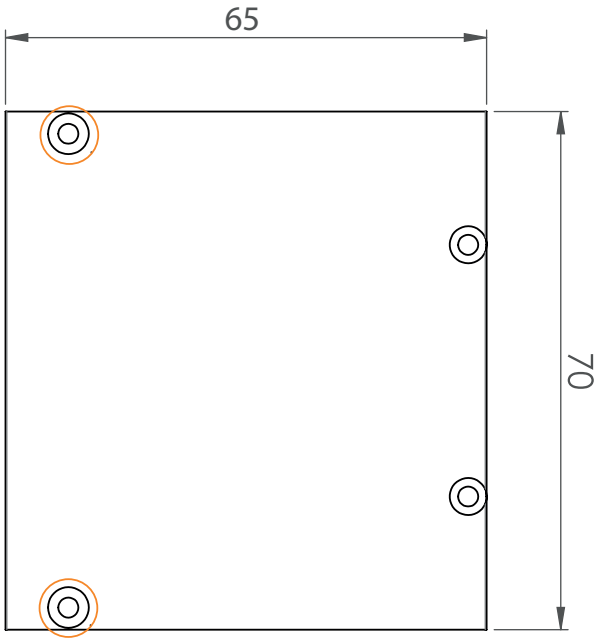


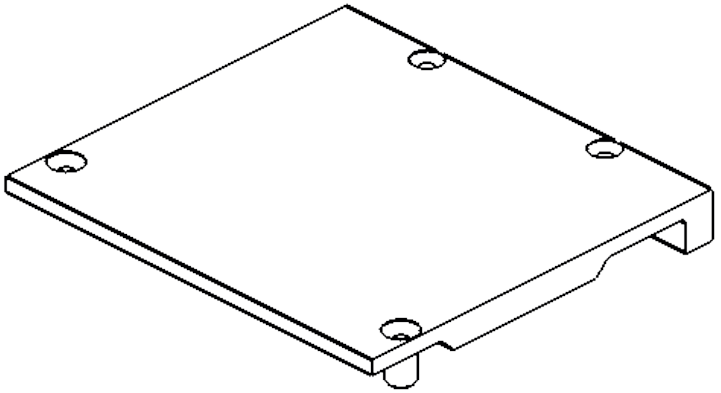


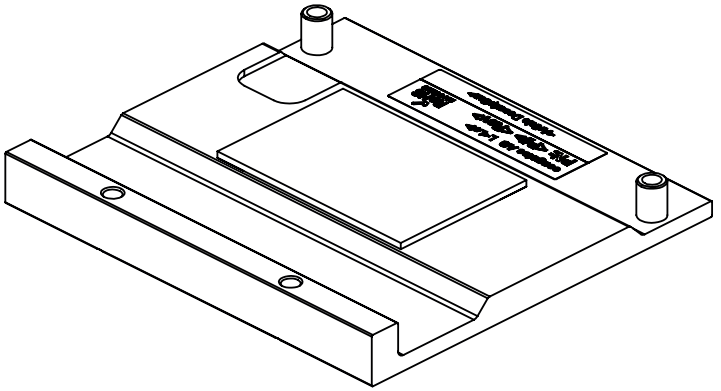
PN: 015851, 015855



M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version

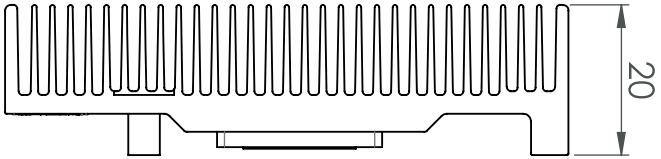


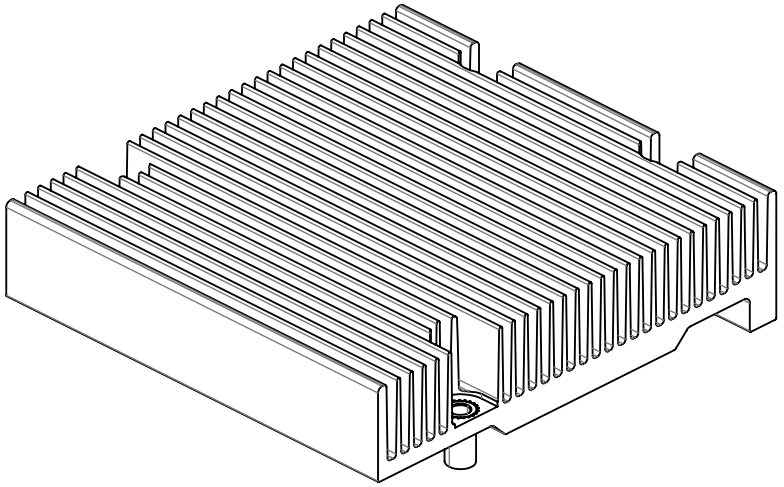




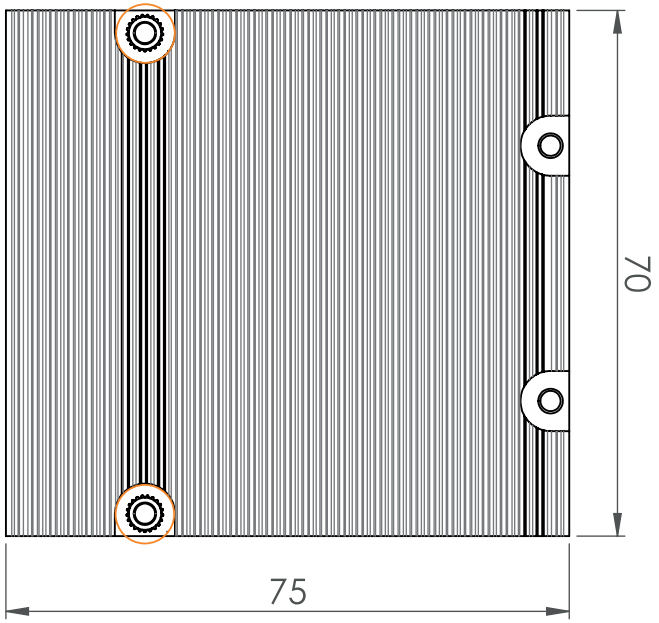
4.2 CSP Dimensions

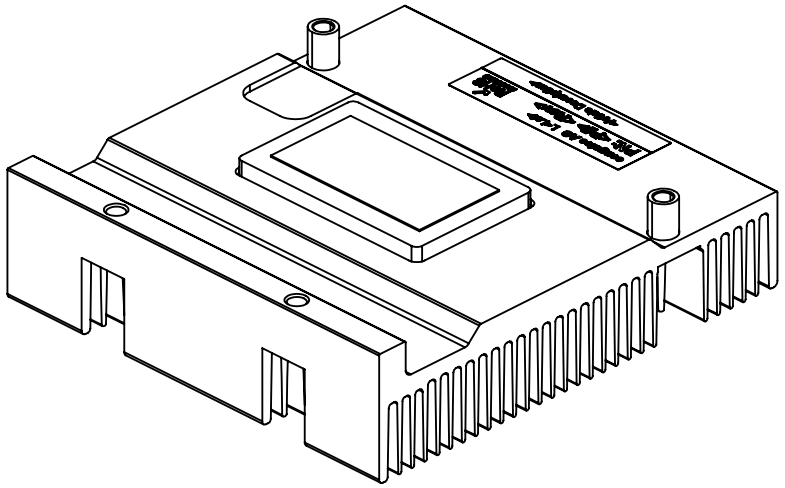
PN: 015853, 015857



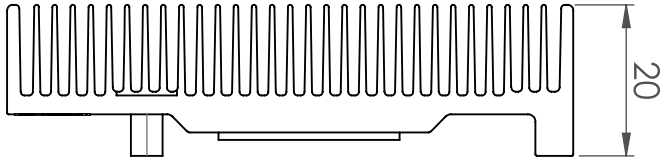


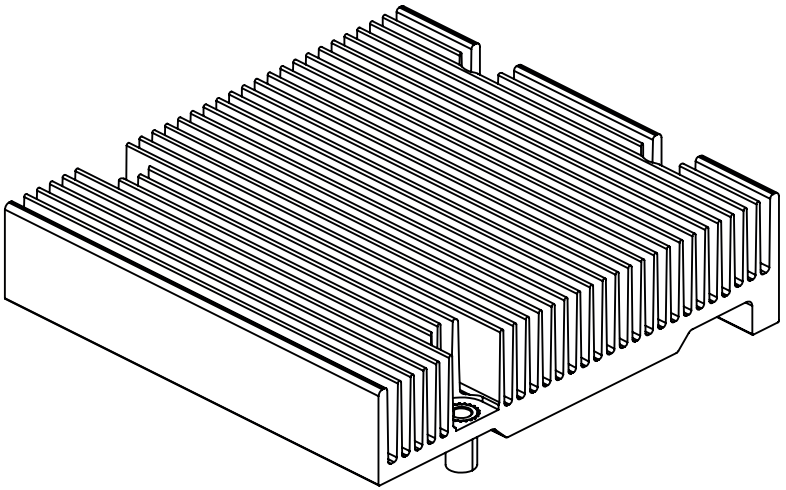
M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version



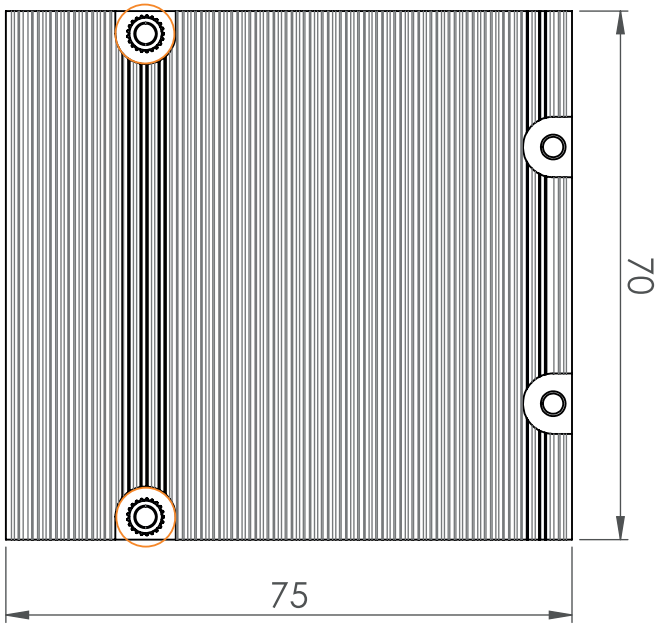


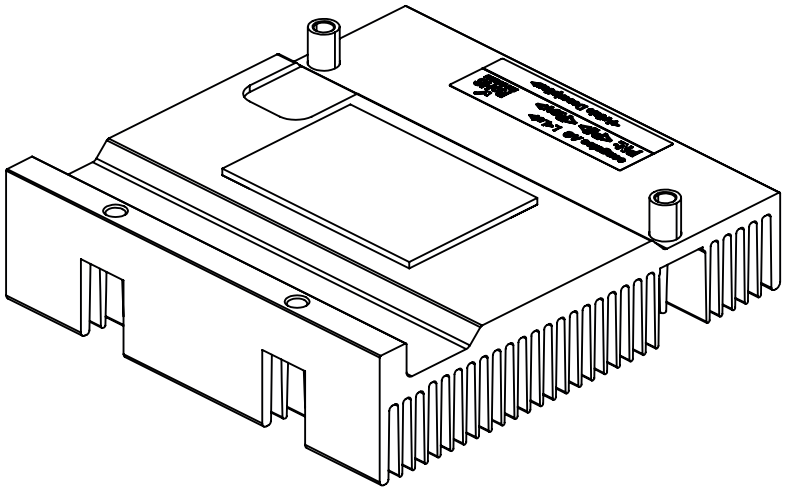
PN: 015850, 015854





M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version





5 Connector Subsystems

The conga-QA7 is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector is able to interface the available signals of the conga-QA7 with the carrier board peripherals.

5.1 PCI Express™

The conga-QA7 offers four PCIe lanes externally on the Edge finger. The lanes are Gen 3 compliant and offer support for full 8 Gb/s bandwidth in each direction per x1 link. Default configuration for the lanes is 4 x1 link. Other configurations are possible as shown in the table below but require a customized BIOS. Contact congatec technical support for more information.

The PCI Express interface is based on the PCI Express Specification 3.0 with Gen 1 (2.5 Gb/s), Gen 2 (5 Gb/s), and Gen 3 (8 Gb/s) speed. For more information, refer to the conga-QA7 pinout Table 14 "PCI Express Signal Descriptions".

Table 8 PCI Express™ Options

	x1	x2	x4
Default	4		
Option		2	
Option	2	1	
Option			1

Note

The options require a customized BIOS.

5.2 Gigabit Ethernet

The conga-QA7 offers a Gigabit Ethernet interface on the edge finger via the onboard TI DP83867 Physical Layer (PHY) connected to the GbE PSE0 controller of the SoC. The Ethernet interface supports TSN IEEE Std 1588™-2008 v2, IEEE Std 802.1AS, Qav,Qbu, Qbv, IEEE Std 802.3br. Use pin 124 of the Qseven® connector for the clock synchronization output. Other supported features are Wake-on-LAN (WoL), Network Booting, Out-of-Band (OOB) and In-Band (IB) Management.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be routed to a 10/100/1000 Base-T RJ45 connector with integrated or external isolation magnetics on the carrier board.

5.3 SATA

The conga-QA7 offers two SATA interfaces with support for:

- SATA 6 Gb/s, 3 Gb/s, and 1.5 Gb/s
- Serial ATA Specification, Revision 3.2
- Advanced Host Controller Interface (AHCI) Specification, Revision 1.3.1
- Hot-Plug operation

5.4 USB

The conga-QA7 offers four USB 2.0 ports and two USB 3.1 Gen 2 (SuperSpeed USB 10Gbps) ports by default.

Optionally, the conga-QA7 can offer other USB configurations as shown in the table below (assembly options):

Table 9 USB Options

Qseven 2.1 Pins	Default (4 + 2)	Option (7 + 1)	Option (2 + 2)
USB_P0	USB_P0	USB_P0	USB_P0
USB_P1	USB_P1	USB_P1	USB_P1
USB_P2	USB_P2	USB_P2	USB_P2
USB_P3	USB_P3	USB_P3	USB_P3
USB_P4 / USB_SSRX2	USB_P4	USB_P4	USB_SSRX1
USB_P5 / USB_SSTX2	USB_P5	USB_P5	USB_SSTX1
USB_P6 / USB_SSRX0	USB_SSRX0	USB_P6	USB_SSRX0
USB_P7 / USB_SSTX0	USB_SSTX0	USB_P7	USB_SSTX0
USB_SSTX1	USB_SSTX1	USB_SSTX1	---
USB_SSRX1	USB_SSRX1	USB_SSRX1	---

Note

1. *USB_P1 Dual Role is only supported under Linux. The port is a standard USB Host port under Windows.*
2. *SuperSpeed USB 10Gbps requires a retimer on the carrier board. Alternatively, the speed can be limited to SuperSpeed USB 5Gbps in the BIOS setup menu.*
3. *Option (2 + 2) is for backward compatibility to Qseven 2.0.*

5.5 UART

The conga-QA7 offers one fully legacy compatible 4-wire UART interface connected to the congatec Board Controller (cBC) by default. Optionally, the UART interface can be connected to the PCH SIO UART0 interface of the SoC instead (assembly option).

5.6 SDIO

The conga-QA7 offers a 4-bit SDIO interface with support for:

- SD Card specification version 3.01 @ 1.8 V Signaling (UHS-1@ SDR 104/50/25/12 & DDR50)
- SD Card specification version 3.01 @ 3.3 V Signaling (Default Speed Mode/High Speed Mode)
- SDIO specification version 3.0
- Card Detection (Insertion / Removal) (SD memory card only)

5.7 High Definition Audio (HDA)

The conga-QA7 offers a High Definition Audio (HDA) interface with support for one external codec on the carrier board. The I2S interface is not supported.

5.8 Display Interfaces

The conga-QA7 offers up to three independent displays as shown in the table below:

Table 10 Display Interface Options

	Display 1		Display 2		Display 3	
	External	Max. Resolution	Internal/External	Max. Resolution	Internal/ External	Max. Resolution
Default	DP++	4096x2160 @ 60Hz	LVDS (up to 2x 24 bit)	1920x1200 @ 60Hz (dual channel mode)	N.A	N.A
Option	DP++	4096x2160 @ 60Hz	eDP	4096x2160 @ 60Hz	DP++	4096x2160 @ 60Hz
Option	DP++	4096x2160 @ 60Hz	MIPI DSI®	3200x2000 @ 60Hz	DP++	4096x2160 @ 60Hz

Note

For non-default display configuration, you need a customized conga-QA7 variant.

5.8.1 DP++

The conga-QA7 offers one Dual-mode DisplayPort (DP++) interface by default with support for:

- VESA DisplayPort Standard 1.4
- VESA DisplayPort PHY Compliance Test Specification 1.4
- VESA DisplayPort Link Layer Compliance Test Specification 1.4
- Up to 4096x2160 @ 60 Hz (4k requires external redriver on carrier board)
- High-bandwidth Digital Content Protection (HDCP) 2.3 and 1.4
- HD Audio (AC-3 Dolby Digital, Dolby Digital Plus, DTS-HD, LPCM [192 kHz/24 bit, 6 Channel], Dolby TrueHD, DTS-HD Master Audio)
- VESA DSC 1.1
- Multi-Stream Transport (MST)
- Main link of 1, 2, or 4 data lanes
- Color depth of up to 36 bpp
- Spread Spectrum Clock (SSC)
- YCbCR 4:4:4, YCbCR 4:2:0, and RGB color format
- Adaptive sync

5.8.2 LVDS

The conga-QA7 offers one Low-Voltage Differential Signaling (LVDS) interface by default via an NXP PTN3460) eDP to LVDS bridge with support for:

- ANSI/TIA/EIA-644-A-2001 standard
- Single LVDS bus operation up to 112 mega pixels per second
- Dual LVDS bus operation up to 224 mega pixels per second
- Up to 1920x1200 @ 60 Hz resolution in dual LVDS bus mode
- Color depth of 18 bits per pixel (bpp) or 24 bpp
- RGB data packing as per JEIDA and VESA data formats
- Pixel clock frequency from 25 MHz to 112 MHz

5.8.3 eDP

Optionally, the conga-QA7 can offer one Embedded DisplayPort (eDP) interface with support for:

- VESA Embedded DisplayPort Standard 1.3
- Main link of 1, 2, or 4 data lanes
- Up to 4096x2160 @ 60Hz resolution
- Auxiliary channel
- Backlight PWM control signal
- VESA Data Stream Compression (DSC)
- Spread Spectrum Clock (SSC)
- Panel Self Refresh (PSR) 1 & 2
- Adaptive sync

5.8.4 MIPI DSI

Optionally, the conga-QA7 can offer one MIPI Display Serial Interface (MIPI DSI®) with support for:

- MIPI DSI® Specification Version 1.2
- 4 data lanes
- Data rate of 2.5 Gb/s per lane
- Up to 3200x2000 @ 60Hz resolution without compression
- Up to 5120x3200 @ 60Hz resolution with compression

Note

The Qseven® specification does not define support for MIPI DSI®. For more information, contact congatec technical support.

5.9 LPC and GPIO

The conga-QA7 offers a Low Pin Count (LPC) interface by default with support for:

- LPC Specification 1.1
- 3.3 V operation
- 24 MHz nominal bus clock frequency
- LPC I/O and Memory Cycles
- Serial IRQ Interface (Continuous and Quiet modes)

The LPC interface is connected to the Enhanced Serial Peripheral Interface (eSPI) controller of the SoC via a Microchip ECE1200 eSPI to LPC bridge (Secondary Slave) by default. Optionally, the eSPI to LPC bridge can be connected to the SoC as the Primary Slave (assembly option).

Optionally, the conga-QA7 can offer GPIO[0:7] signals instead of the LPC interface (assembly option).

5.10 SPI

The conga-QA7 offers a Serial Peripheral Interface (SPI) for an external 3.3V 256 Mbit BIOS Flash device powered from the standby rail. Optionally, the SPI can be connected to the PCH SPI1 of the SoC instead to support other SPI devices (assembly option).

5.11 I²C Bus

The conga-QA7 offers an Inter-Integrated Circuit (I^2C) bus inteface connected to the congatec Board Controller (cBC).

5.12 CAN Bus

The conga-QA7 offers a Controller Area Network (CAN) bus interface with support for:

- ISO 11898-1 (identical to Bosch CAN protocol specification 2.0 part A,B)
- ISO 11898-4 (Timetriggered communication on CAN)
- CAN FD protocol specification 1.0

Note

CAN FD is only supported by Linux (Yocto).

5.13 Power Control

The conga-QA7 supports ATX-style power supplies control. In order to do this the power supply must provide a constant source of VCC_5V_SB power. The AT-style power supply (5V only) is also supported. In this case, the conga-QA7's pin PWRBTN# should be left unconnected, pin SUS_S3# should control the main power regulators on the carrier board (+3.3V...) and pins VCC_5V_SB should be connected to the 5V input power rail according to the Qseven specification.

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit. This input is optional and should be left unconnected when not used. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QA7 module is capable of generating its own power good.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to control the main 5V rail of the power supply for module and all other main power supplies on carrier board. In order to accomplish this, the signal must be inverted with an inverter/transistor that is supplied by standby voltage (ATX-style) or system input voltage (AT-style) and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3.3V_SB using a 10k resistor. When PWRBTN# is asserted, it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5V input power is the sole operational power source for the conga-QA7. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-QA7 application:

- It has also been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem does not arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush current on the conga-QA7 VCC_5V_SB power rail can go up as high as TBD A and as high as TBD A on the conga-QA7 VCC power rail within a short time (approx 100µs) and with a voltage rise time of 100µs. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

5.14 Power Management

The conga-QA7 complies with the Advanced Configuration and Power Interface Specification Revision 5.0.

5.15 SMBus

The conga-QA7 provides an SMBus which is connected to the congatec Board Controller (cBC) by default.

Optionally, the SMBus can be connected to the SoC SMBus via an isolation switch controlled through BIOS.

5.16 MIPI CSI-2

The conga-QA7 does not support MIPI CSI-2.

6 Onboard Interfaces and Devices

6.1 Memory

The conga-QA7 offers onbaord Dynamic Random-Access Memory (DRAM) with support for:

- JESD209-4 Low Power Double Data Rate 4 (LPDDR4) including Addendum No. 1, Low Power Double Data Rate 4X (LPDDR4X)
- Memory capacity of up to 16 GB @ 3200 MT/s or up to 8 GB @ 4267 MT/s
- Suspend to RAM (STR)

The default DRAM of each conga-QA7 variant is listed in section 1.2 "conga-QA7 Options Information".

6.2 eMMC

The conga-QA7 offers an onboard eMMC 5.1 flash device. The default capacity of each conga-QA7 variant is listed in section 1.2 "conga-QA7 Options Information". Optionally, any conga-QA7 variant can offer up to 256 GB capacity (assembly option).

Note

1. *For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.*
2. *Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.*

6.3 congatec Board Controller (cBC)

The conga-QA7 offers an onboard Microchip MEC1705Q-C2-SZ-I microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.3.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.3.2 Fan Control

The conga-QA7 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

6.3.3 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

6.3.4 Watchdog

The conga-QA7 is equipped with a multi stage watchdog solution that can be triggered by software of external hardware. For more information about the watchdog feature, see the BIOS setup description of this document and the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

6.4 OEM BIOS Customization

The conga-QA7 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf at www.congatec.com or contact technical support.

The customization features supported are described below:

6.4.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.4.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.4.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.4.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.4.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.5 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-QA7 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.6 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.7 Security Features

The conga-QA7 offers an onboard Infineon Trusted Platform Module (TPM) SLB9670 device with support for:

- Trusted Platform Module Library Specification, Family "2.0"
- Random Number Generator (RNG) according to NIST SP800-90A
- Full personalization with Endorsement Key (EK) and EK certificate
- Built-in support by Linux Kernel

7 conga Tech Notes

The conga-QA7 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.7.1 Processor Core

The SoC features Dual or Quad 3-way Supersclar, Out-of-Order Execution processor cores. Some of the features supported by the core are:

- Intel® 64 architecture
- Intel® Streaming SIMD Extensions
- Support for Intel® VTx-2 and VT-d
- Thermal management support vial Intel® Thermal Monitor
- Uses Programmable Service Engine Interrupt Routing
- Uses 10 nm process technology

Note

Intel® Hyper-Threading technology is not supported (four cores execute four threads)

7.7.2 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

7.7.2.1 AHCI

The SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.7.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QA7 ACPI thermal solution offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

1. *The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.*

2. *If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.*

7.1 ACPI Suspend Modes and Resume Events

conga-QA7 supports S3 (STR= Suspend to RAM). S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by Windows® 10 and Linux (S4_OS= Hibernate).

The table below lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Table 11 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 12 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
I_{OL}	Output low current. The I_{OL} is the maximum output low current the module must be able to drive to an external circuitry.
I_{IL}	Input low current. The I_{IL} is the maximum input low current that must be provided to the Qseven® module via external circuitry in order to guarantee a proper logic low level of the signal.
P	Power Input
NC	Not Connected
PCIe	PCI Express differential pair signals
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
SATA	Serial Advanced Technology Attachment differential pair signals
LVDS	Low-Voltage Differential Signaling differential pair signals
TMDS	Transition Minimized Differential Signaling differential pair signals
CMOS	Logic input or output.
CMOS OD	Open Drain Logic input or output
eDP/DP	(embedded) Display Port Signal

Table 13 Edge Finger Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF [1]	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT# / GPO0 [2]	20	PWRBTN#
21	SLP_BTN# / GPII1	22	LID_BTN# / GPII0 [1]
23	GND	24	GND
	Key		Key
25	GND	26	PWGIN
27	BATLOW# / GPII2 [1]	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE# / BOOT_ALT#	42	SDIO_CLK
43	SDIO_CD#	44	reserved
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	reserved
53	reserved	54	reserved
55	reserved	56	USB_OTG_PEN
57	GND	58	GND
59	HDA_SYNC / I2S_WS [1]	60	SMB_CLK / GP1_I2C_CLK [1]
61	HDA_RST# / I2S_RST# [1]	62	SMB_DAT / GP1_I2C_DAT [1]
63	HDA_BITCLK / I2S_CLK [1]	64	SMB_ALERT#
65	HDA_SDI / I2S_SDI [1]	66	GP0_I2C_CLK
67	HDA_SDO / I2S_SDO [1]	68	GP0_I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7- [2] / USB_SSTX0-	76	USB_P6- [2] / USB_SSRX0-

Pin	Signal	Pin	Signal
77	USB_P7+ [2] / USB_SSTX0+	78	USB_P6+ [2] / USB_SSRX0+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5- / USB_SSTX2- [2] / USB_SSTX1- [2]	82	USB_P4- / USB_SSRX2- [2] / USB_SSRX1- [2]
83	USB_P5+ / USB_SSTX2+ [2] / USB_SSTX1+ [2]	84	USB_P4+ / USB_SSRX2+ [2] / USB_SSRX1+ [2]
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_VBUS [1]	92	USB_ID [1]
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	eDP0_TX0+ [2] / LVDS_A0+ / DSI0_D0+ [2]	100	DP1_TX0+ [2] / LVDS_B0+
101	eDP0_TX0- [2] / LVDS_A0- / DSI0_D0- [2]	102	DP1_TX0- [2] / LVDS_B0-
103	eDP0_TX1+ [2] / LVDS_A1+ / DSI0_D1+ [2]	104	DP1_TX1+ [2] / LVDS_B1+
105	eDP0_TX1- [2] / LVDS_A1- / DSI0_D1- [2]	106	DP1_TX1- [2] / LVDS_B1-
107	eDP0_TX2+ [2] / LVDS_A2+ / DSI0_D2+ [2]	108	DP1_TX2+ [2] / LVDS_B2+
109	eDP0_TX2- [2] / LVDS_A2- / DSI0_D2+ [2]	110	DP1_TX2- [2] / LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	eDP0_TX3+ [2] / LVDS_A3+ / DSI_D3+ [2]	114	DP1_TX3+ [2] / LVDS_B3+
115	eDP0_TX3- [2] / LVDS_A3- / DSI_D3- [2]	116	DP1_TX3- [2] / LVDS_B3-
117	GND	118	GND
119	eDP0_AUX+ [2] / LVDS_A_CLK+ / DSI0_CLK+ [2]	120	DP1_AUX+ [2] / LVDS_B_CLK+
121	eDP0_AUX- [2] / LVDS_A_CLK- / DSI0_CLK- [2]	122	DP1_AUX- [2] / LVDS_B_CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	124	GBE_PPS / GP_1-Wire_Bus [1] / HDMI_CEC [1]
125	LVDS_DID_DAT / GP2_I2C_DAT	126	eDP0_HPD# / LVDS_BLC_CLK [1]
127	LVDS_DID_CLK / GP2_I2C_CLK	128	DP1_HPD# / LVDS_BLC_CLK [1]
129	CAN0_TX	130	CAN0_RX
131	DP_LANE3+ / TMDS_CLK+ [1]	132	USB_SSTX1-
133	DP_LANE3- / TMDS_CLK- [1]	134	USB_SSTX1+
135	GND	136	GND
137	DP_LANE1+ / TMDS_LANE1+ [1]	138	DP_AUX+
139	DP_LANE1- / TMDS_LANE1- [1]	140	DP_AUX-
141	GND	142	GND
143	DP_LANE2+ / TMDS_LANE0+ [1]	144	USB_SSRX1-
145	DP_LANE2- / TMDS_LANE0- [1]	146	USB_SSRX1+
147	GND	148	GND
149	DP_LANE0+ / TMDS_LANE2+ [1]	150	HDMI_CTRL_DAT
151	DP_LANE0- / TMDS_LANE2- [1]	152	HDMI_CTRL_CLK
153	HDMI_HPD#	154	DP_HPD#
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#

Pin	Signal	Pin	Signal
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	UART0_TX	172	UART0_RTS#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	UART0_RX	178	UART0_CTS#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0 / GPIO0 [2]	186	LPC_AD1 / GPIO1 [2]
187	LPC_AD2 / GPIO2 [2]	188	LPC_AD3 / GPIO3 [2]
189	LPC_CLK / GPIO4 [2]	190	LPC_FRAME# / GPIO5 [2]
191	SERIRQ / GPIO6 [2]	192	LPC_LDRQ# / GPIO7 [2]
193	VCC_RTC	194	SPKR / GP_PWM_OUT2 [1]
195	FAN_TACHOIN / GP_TIMER_IN [1]	196	FAN_PWMOUT / GP_PWM_OUT1 [1]
197	GND	198	GND
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1# [1]
203	SPI_SCK	204	MFG_NC4
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	NC	212	NC
213	NC	214	NC
215	NC	216	NC
217	NC	218	NC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

Note

1. *Not supported*
2. *Assembly option*

Table 14 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 10k	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Note

Configured to four x1 PCI Express links by default. For other options, refer to section 5.1 "PCI Express™".

Table 15 UART Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	171	Serial Data Transmitter	O 3.3V		
UART0_RX	177	Serial Data Reciever	I 3.3V		
UART0_CTS#	178	Handshake signal, ready to send data	I 3.3V		
UART0_RTS#	172	Handshake signal, ready to receive data	O 3.3V		

Note

The UART interface is provided by the congatec Board Controller (cBC) by default. For other options, refer to section 5.5 "UART".

Table 16 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		
GBE_CTREF	15	Not supported.			
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3VSB PP		
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB PP		GBE_LINK100# and GBE_LINK10#
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3VSB PP		

Note

The IEEE 1588 PTP Clock Output is provided on pin 124 (Table 30 "Miscellaneous Signal Descriptions").

Table 17 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	OD		

Table 18 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair.	I/O		Dual role USB port supports Host and Client mode
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		
USB_P4+ USB_P4-	84 82	Universal Serial Bus Port 4 differential pair.	I/O		Assembly option: USB_SSRX1+ USB_SSRX1-
USB_P5+ USB_P5-	83 81	Universal Serial Bus Port 5 differential pair.	I/O		Assembly option: USB_SSTX1+ USB_SSTX1-
USB_SSRX0+ USB_SSRX0-	78 76	USB Superspeed receive signal differential pair.	I		Assembly option: USB_P6+ USB_P6-
USB_SSTX0+ USB_SSTX0-	77 75	USB Superspeed transmit signal differential pair.	O		Assembly option: USB_P7+ USB_P7-
USB_SSTX1+ USB_SSTX1-	134 132	USB Superspeed transmit signal differential pair.	O		
USB_SSRX1+ USB_SSRX1-	146 144	USB Superspeed receive signal differential pair.	I		
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k	
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k	
USB_ID	92				USB_ID is not supported.
USB_VBUS	91				USB_VBUS is not supported.
USB_DRIVE_ VBUS	56	USB power enable pin for USB Port 1. Enables the power for the USB Dual role port on the carrier	O 3.3V CMOS	PD 100k	

Note

1. *The assembly options are described in section 5.4 "USB".*

2. *SuperSpeed USB 10Gbps requires a retimer on the carrier board. Alternatively, the speed can be limited to SuperSpeed USB 5Gbps in the BIOS setup menu.*

Table 19 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 10k	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 50MHz 3.3V signaling and 208MHz 1.8V signaling	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP		
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 10k	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O 3.3V	PU 100k	
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3	49 48 51 50	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V OD/PP		

Note

The conga-QA7 also supports 1.8 V Signaling (UHS-1).

Table 20 HDA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	61	HD Audio Codec Reset.	O 3.3VSB	PD 100k	
HDA_SYNC	59	HD Audio Serial Bus Synchronization.	O 3.3VSB		
HDA_BITCLK	63	HD Audio 24 MHz Serial Bit Clock from Codec.	O 3.3VSB	PD 100k	
HDA_SDO	67	HD Audio Serial Data Output to Codec.	O 3.3VSB		
HDA_SDI	65	HD Audio Serial Data Input from Codec.	I 3.3VSB		

Note

The conga-QA7 does not support the I2S interface.

Table 21 LVDS and eDP Flat Panel Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V	PD 100k	
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V	PD 100k	
LVDS_BLT_CTRL / GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0- eDP0_TX0+ eDP0_TX0-	99 101	LVDS primary channel differential pair 0. embedded Display Port primary channel differential pair 0.	O LVDS/ O eDP		
LVDS_A1+ LVDS_A1- eDP0_TX1+ eDP0_TX1-	103 105	LVDS primary channel differential pair 1. embedded Display Port primary channel differential pair 1.	O LVDS/ O eDP		
LVDS_A2+ LVDS_A2- eDP0_TX2+ eDP0_TX2-	107 109	LVDS primary channel differential pair 2. embedded Display Port primary channel differential pair 2.	O LVDS/ O eDP		
LVDS_A3+ LVDS_A3- eDP0_TX3+ eDP0_TX3-	113 115	LVDS primary channel differential pair 3. embedded Display Port primary channel differential pair 3.	O LVDS/ O eDP		
LVDS_A_CLK+ LVDS_A_CLK- eDP0_AUX+ eDP0_AUX-	119 121	LVDS primary channel differential pair clock lines. embedded Display Port primary auxiliary channel.	O LVDS/ O eDP		
LVDS_B0+ LVDS_B0- DP1_TX0+ DP1_TX0-	100 102	LVDS secondary channel differential pair 0. Display Port secondary channel differential pair 0.	O LVDS/ O DP		
LVDS_B1+ LVDS_B1- DP1_TX1+ DP1_TX1-	104 106	LVDS secondary channel differential pair 1. Display Port secondary channel differential pair 1.	O LVDS/ O DP		
LVDS_B2+ LVDS_B2- DP1_TX2+ DP1_TX2-	108 110	LVDS secondary channel differential pair 2. Display Port secondary channel differential pair 2.	O LVDS/ O DP		
LVDS_B3+ LVDS_B3- DP1_TX3+ DP1_TX3-	114 116	LVDS secondary channel differential pair 3. Display Port secondary channel differential pair 3.	O LVDS/ O DP		

LVDS_B_CLK+ LVDS_B_CLK- DP1_AUX+ DP1_AUX-	120 122	LVDS secondary channel differential pair clock lines. Display Port secondary auxiliary channel.	O LVDS/ O DP		
LVDS_DID_CLK / GP2_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.	I/OD 3.3V	PU 2k2	
LVDS_DID_DAT / GP2_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/OD 3.3V	PU 2k2	
DP1_HPD#	128	DisplayPort secondary Hotplug detection.	I/OD 3.3V	PU 10k	LVDS_BLC_CLK is not supported.
eDP0_HPD#	126	embedded DisplayPort primary Hotplug detection.	I/OD 3.3V	PU 10k	LVDS_BLC_DAT is not supported.

Note

eDP0 and DP1 are assembly options. Either LVDS or eDP signals can be supported. For more information, see section 5.8 "Display Interfaces".

Table 22 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3 (Shared with TMDS_CLK+ and TMDS_CLK-)	O DP		
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2 (Shared with TMDS_LANE0+ and TMDS_LANE0-)	O DP		
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1 (Shared with TMDS_LANE1+ and TMDS_LANE1-)	O DP		
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0 (Shared with TMDS_LANE2+ and TMDS_LANE2-)	O DP		
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O DP		
DP_HPD#	154	Hot plug detection signal that serves as an interrupt request.	I 3.3V	PU 10k	Supports open drain and PushPull driver.

Note

The DisplayPort signals are shared with the TMDS signals.

Table 23 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines. (Shared with DP_LANE3- and DP_LANE3+)	O TMDS		Passive level shifter shall use PD 470R.
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0. (Shared with DP_LANE2- and DP_LANE2+)	O TMDS		Passive level shifter shall use PD 470R.
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1. (Shared with DP_LANE1- and DP_LANE1+)	O TMDS		Passive level shifter shall use PD 470R.
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2. (Shared with DP_LANE0- and DP_LANE0+)	O TMDS		Passive level shifter shall use PD 470R.
HDMI_CTRL_CLK	152	DDC based control signal (clock)	I/OD 3.3V	PU 2k2	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
HDMI_CTRL_DAT	150	DDC based control signal (data)	I/OD 3.3V	PU 2k2	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
HDMI_HPD#	153	Hot plug active low detection signal that serves as an interrupt request.	I 3.3V	PU 10k	Supports open drain and PushPull Driver.

Note

The conga-QA7 does not natively support TMDS. A passive or active DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.

Table 24 LPC and GPIO Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	Multiplexed Command, Address and Data.	I/O 3.3V		Assembly option: GPIO0 GPIO1 GPIO2 GPIO3
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	I/O 3.3V		Assembly option: GPIO4
LPC_LDRQ#	192	LPC DMA request.	I 3.3V		Assembly option: GPIO5
LPC_CLK	189	LPC clock (24 MHz)	O 3.3V		Assembly option: GPIO6
SERIRQ	191	Serialized Interrupt.	I/O 3.3V		Assembly option: GPIO7

Note

Optionally, the conga-QA7 can offer GPIO[0:7] instead of the LPC bus interface (assembly option). For more information, see section 5.9 "LPC and GPIO".

Table 25 SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3VSB		
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3VSB		
SPI_SCK	203	SPI clock output.	O 3.3VSB		
SPI_CS0#	200	SPI chip select 0 output.	O 3.3VSB		
SPI_CS1#	202	Not supported	O 3.3VSB	PU 10k	

Note

1. *The SPI only supports a BIOS flash device by default. The BIOS flash device must be powered from the standby rail. For other options, see section 5.10 "SPI".*

2. *Route the SPI signals as short as possible because of their limited drive strength.*

Table 26 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		

Table 27 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	219-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		VCC_5V_SB should be connected to VCC if not used on carrier board.
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.6 - 3.3 V).	P		
GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 28 Power Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that all power rails located on the carrier board are ready for use.	I 5V	PU 10k 3.3V	Supports open drain and PushPull driver.
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	

Table 29 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3V	PU 10k	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k	GPII2 is not supported.
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		Assembly option: GPO0
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB	PD 100k	
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB	PD 100k	
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k	GPII1 is not supported.
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k	GPII0 is not supported.

Table 30 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V	PU 10k	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V	PD 100k	
GP0_I2C_CLK	66	Clock line of I²C bus.	I/OD 3.3V	PU 2k2	
GP0_I2C_DAT	68	Data line of I²C bus.	I/OD 3.3V	PU 2k2	

GP1_SMB_CLK	60	Clock line of System Management Bus.	I/OD 3.3VSB	PU 2k2	GP1_I2C_CLK is not supported.
GP1_SMB_DAT	62	Data line of System Management Bus.	I/OD 3.3VSB	PU 2k2	GP1_I2C_DAT is not supported.
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/OD 3.3VSB	PU 10k	
SPKR	194	Output for audio enunciator, the "speaker" in PC AT systems.	O 3.3V		GP_PWM_OUT2 is not supported.
BIOS_DISABLE# / BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module's onboard BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3VSB	PU 10k	
GBE_PPS	124	IEEE 1588 PTP Clock Output.	I/O 3.3V		GP_1-Wire_Bus and HDMI_CEC are not supported.

Table 31 Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes.	N.A	N.A	JTAG_TCK
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes.	N.A	N.A	JTAG_TDO
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes.	N.A	N.A	JTAG_TDI
MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes.	N.A	N.A	JTAG_TMS
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes.	N.A	N.A	JTAG_TRST#

Table 32 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 10k	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V	PU 10k	

Table 33 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	196	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature.	O 3.3V	PU 10k	GP_PWM_OUT1 is not supported.
FAN_TACHOIN	195	Fan tachometer input.	I 3.3V	PU 10k	GP_TIMER_IN is not supported.

9 System Resources

TBD

10 BIOS Setup Description

The BIOS setup description of the conga-QA7 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-QA7 is identified as QA70R1xx, where:

- QA70 is the project name
- R is the identifier for a BIOS ROM file
- 1 is the feature number
- xx is the major and minor revision number.

The binary size of conga-QA7 BIOS is 32 MB.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-QA7 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information, refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.4 Supported Flash Devices

The conga-QA7 supports the following flash device:

- TBD

The flash device listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" at www.congatec.com.