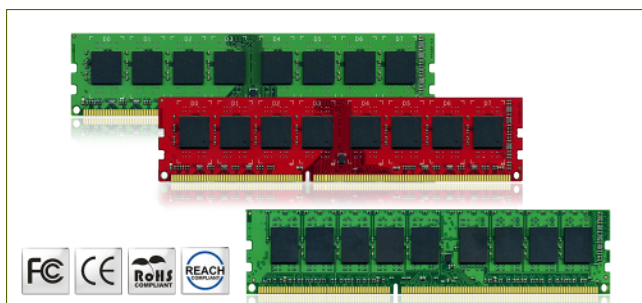


❖ Specification

DDRIII SO-DIMM		DDRIII SO-DIMM w/ECC	
■ Interface	JEDEC Standard 204-pin Dual In-Line Memory Module	■ Interface	JEDEC Standard 204-pin Dual In-Line Memory Module
■ Grade	0°C~+70°C / -40°C~+85°C	■ Grade	0°C~+70°C / -40°C~+85°C
■ IC Data Rate	Non-Fixed / DDRIII-1600	■ IC Data Rate	DDRIII-1600
■ Bandwidth	64 bits	■ Bandwidth	72 bits
■ DIMM Data Rate	1600MHz / 1333MHz / 1066MHz	■ DIMM Data Rate	1600MHz / 1333MHz / 1066MHz
■ Capacity	1GB / 2GB / 4GB / 8GB	■ Capacity	1GB / 2GB / 4GB / 8GB
■ Pin Number	204 Pins	■ Pin Number	204 Pins
■ Height	30 mm + 0.15 mm	■ Height	30 mm + 0.15 mm
■ Voltage	1.5V & 1.35V	■ Voltage	1.5V & 1.35V
■ Warranty	5 years	■ Warranty	5 years

❖ Features

- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt ± 0.075 & 1.35 Volt ± 0.1
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support
- SDRAMs are 78-ball BGA Package
- JEDEC Standard 1.5V (1.425V~1.575V) & 1.35V (1.28V~1.45V)
- Two different termination values (Rtt_Nom & Rtt_WR)
- 30u" gold fingers.
- Low-profile NON-ECC optional & Low-voltage optional



❖ Specification

DDRIII U-DIMM		DDRIII U-DIMM w/ECC	
■ Interface	JEDEC Standard 240-pin Dual In-Line Memory Module	■ Interface	JEDEC Standard 240-pin Dual In-Line Memory Module
■ Grade	0°C~+70°C / -40°C~+85°C	■ Grade	0°C~+70°C / -40°C~+85°C
■ IC Data Rate	Non-Fixed / DDRIII-1600	■ IC Data Rate	DDRIII-1600
■ Bandwidth	64 bits	■ Bandwidth	72 bits
■ DIMM Data Rate	1600MHz / 1333MHz / 1066MHz	■ DIMM Data Rate	1600MHz / 1333MHz / 1066MHz
■ Capacity	1GB / 2GB / 4GB / 8GB	■ Capacity	2GB / 4GB / 8GB
■ Pin Number	240 Pins	■ Pin Number	240 Pins
■ Height	30 mm + 0.15 mm	■ Height	30 mm + 0.15 mm
■ Voltage	1.5V & 1.35V	■ Voltage	1.5V & 1.35V
■ Warranty	5 years	■ Warranty	5 years

❖ Features

- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt ± 0.075 & 1.35 Volt ± 0.1
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support
- SDRAMs are 78-ball BGA Package
- JEDEC Standard 1.5V (1.425V~1.575V) & 1.35V (1.28V~1.45V)
- Two different termination values (Rtt_Nom & Rtt_WR)
- 30u" gold fingers.
- Low-profile NON-ECC optional & Low-voltage optional