PCLD-788

RELAY MULTIPLEXER BOARD

USER'S MANUAL

Part No. 2003788000 Rev. A1
Printed in Taiwan Mar. 1990

TABLE OF CONTENTS

CHAPTER 1. GENERAL INFORMATION

1.1. Introduction

PCLD-788 Relay Multiplexer Board is a daughter board controlled by the digital output port of PCL-711, PCL-718, PCL-812 and other data acquisition card with digital output port.

The PCLD-788 can multiplex sixteen analog inputs to one output and can be cascaded up to 16 boards and 256 channels.

The multiplexer has break-before-make mechanism which makes two channels never short together. This board also offers channel-close signal for measurement devices to make correct measurement.

PCLD-788 also contains cold junction sensing circuit and allows the measurement of thermocouple transducer. All types of thermocouple can be handled with software compensation and linearization.

1.2. Product Features

A summary of PCLD-788 features are as follow :

* 16 channel input and 1 channel output
* Break-before-make switching (3 milliseconds between opening and closing)
* Channel-close signal output
* Cold junction temperature output
* Expandable to 256 input channels maximum
* Using PC power or external power selectable
* Input voltage isolation withstand 100V DC maximum

1.3. Specifications

Input Channel :	16 differential channels
Output Channel :	3 output terminals
Maximum switching power :	10 VA
Maximum switching voltage :	100 VDC or Peak AC
Maximum switching current :	0.50A
Maximum carry current :	1.00A
Life Expectancy :	100 million operations at 10 VDC, 1mA
Maximum switch time :	6 milliseconds (including break-before-make) and bounce
Isolation Resistance :	100 Mega Ohms
Cold junction compensation :	+24.4 mV/Deg.c (0.0V at 0.0 Deg.c)
Power consumption :	+5V (380mA Maximum) +12V (100mA Maximum)
Connection type :	
Multiplexer control signals :	20 pin flat cable connectors
Others :	Screw terminal
Dimensions :	20.5 cm (L) * 11.43 cm (W) or 8.07 " (L) * 4.5 " (W)

CHAPTER 2. INSTALLATION

2.1. Initial Inspection

Inside the shipping container, you should find this operating manual and the PCLD-788 card. The PCLD-788 was carefully inspected both mechanically and electrically before shipment. It should be free of marks and scratches and in perfect electrical order on receipt.

When unpacking, check the unit for signs of shipping damage (damaged box,scratches, dent, etc). If there is damage to the unit or it fails to meet specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing material for the inspection by the carrier. We will make arrangements to repair or replace the unit.

Remove the PCLD-788 interface card from its protective packaging carefully. Keep the anti-vibration package. Whenever you are not using the board, please store it in the package for protection.

Discharge any static electricity by touching the back of the system unit before you handle the board. You should avoid contact with materials that create static electricity such as plastic, vinyl, and styrofoam. The board should be handled only by the edges to avoid static electric discharge which could damage the integrated circuits on the PCLD-788.

2.2. Connector

CN1 : Sixteen channels of input (CH0 to CH15).

CN2 & CN3 : CN2 and CN3 are 20 pins connectors and the both have same pins assignment. The signals on these connectors are multiplexer control signals and the pin assignments are described as Fig. 2-2-1. The bits C3 to C0 are used as multiplexer channel selection control. The binary value of C3 to C0 corresponds

to the channel number selected. For example, when C3 to C0 are 1010, channel 10 is closed. The bits C7 to C4 are board selection Signals. The output of PCLD-788 is enabled only when the bit pattern of C7 to C4 is matched with the setting of SW1 (Card ID). Pin #17 to pin #20 are power supply from PC. Others pins are not used.

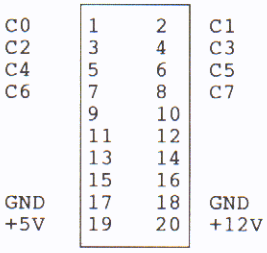


Fig. 2-2-1

CN4 : CJC signal output. 0V at 0°C, 24.4mV/°C

CN5 : Channel-close signal output. It offers both inversed and non-inversed logic.

CN6 & CN7 : The output signal of the relay multiplexer

CN8 : External power input terminal. External power input is used when not using PC power. The jumper JP1 needs position as following :

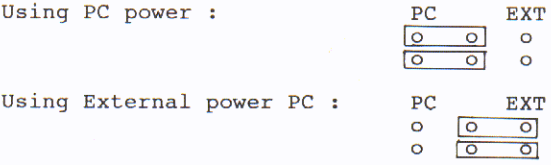
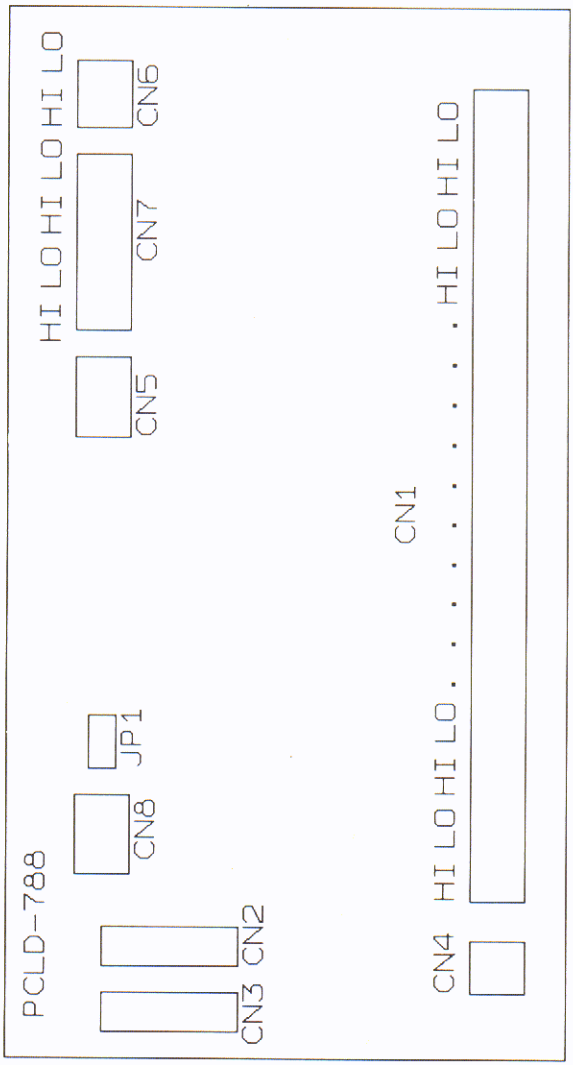


Fig. 2-2-2

Fig. 2-2-3


PCLD-788
JP1
CN8
CN2
CN3
HI LO HI LO HI LO
CN5
CN7
CN6
CN1
CN4 HI LO HI LO . . . . . HI LO HI LO

2.3. Channel Selection

PCLD-788 has 16 input channels (CN1). One of sixteen channels will be chosen according to CN2 (CN3) bit C0 to bit C3. Following is the relation of bit C3 to bit C0 and channel selected.

Bit 3	Bit 2	Bit 1	Bit 0	Channel
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

The bit 0 to bit 3 signals are controlled by Digital Output of Data Acquisition Board and determine the channel to be closed.

2.4. Board Address Setting

PCLD-788 has 16 channels and can expand up to 256 channels, so the maximum expansion can use up to 16 PCLD-788 boards and each board has its own address. The DIP Switch (SW1) is used to select PCLD-788 board address. The address format is as following :

Switch Position (SW1)				
1	2	3	4	ADDR.
ON	ON	ON	ON	0
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	10
OFF	ON	OFF	OFF	11
OFF	OFF	ON	ON	12
OFF	OFF	ON	OFF	13
OFF	OFF	OFF	ON	14
OFF	OFF	OFF	OFF	15

The control signals bit C7 to bit C4 on connector CN2 (CN3) are used to select the board which the multiplexer output is enabled. If the board is not selected, the output is disabled and is left open. The format of bit C7 to C4 is as following :

Bit C7	Bit C6	Bit C5	Bit C4	ADDR.
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

When more than one PCLD-788 boards are cascaded, as following figure, every PCLD-788 boards has its individual address. To access

the PCLD-788 with address 1 and channel 2, the control signals on CN2 (CN3) bit C7 to bit C0 should be 00010010 hex12.

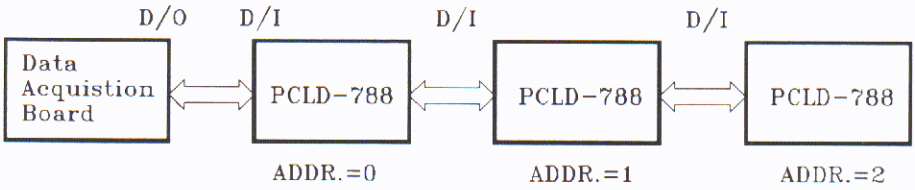


Fig. 2-4-1

2.5. CJC Output

PCLD-788 provides cold junction compensation for the thermocouple applications. CN4 is for the CJC output. Then, the data acquisition card can measure the voltage and transfer it to cold junction temperature. The formula to calculate temperature is :

T = V*1000/24.4

T : Temperature of cold junction
V : CJC output voltage

VR1 (see Appendix B) is used to adjust CJC output. If the data of temperature is not correct, VR1 needs to be adjusted to get the correct temperature data.

2.6. Power Source Selection

PCLD-788 requires both +12V and +5V power supply. The connector 2 pin # 19 and # 20 are used for power supply connection. Since the PC offers +5V and +12V power supply, the PCLD-788 can be powered directly from the PC I/O bus by connecting the PCLD-788 with the PCL-718, 711, and 812. Please refer to each product's

connector pin assignment for proper connections.

PCLD-788 can also use external power source. The CN8 is the power input connector and the jumper JP1 selects the power source (PC or External) to be used.

The +12V power input is converted by a DC/DC converter to generate +/-15V DC outputs. This device greatly reduce the input power noise and offer stable output of CJC compensation.

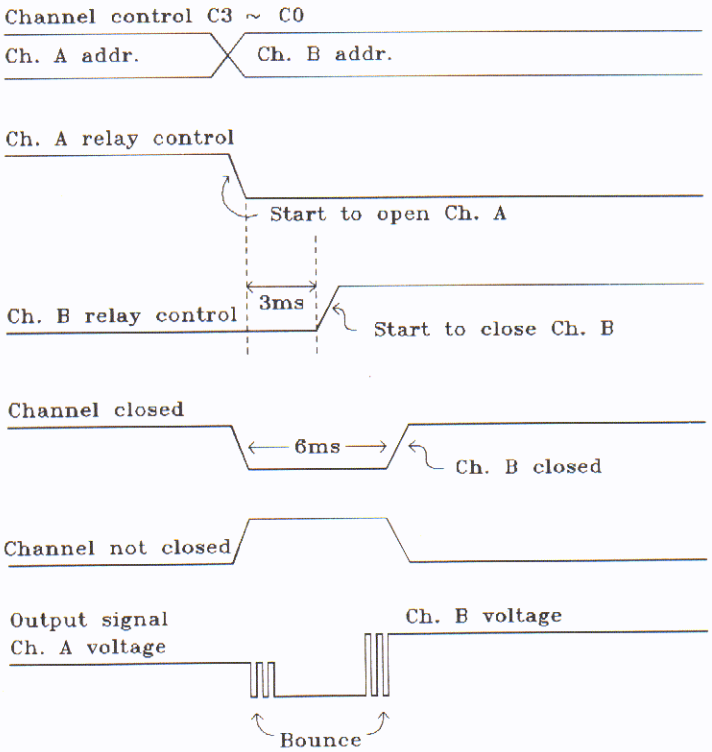
CHAPTER 3. OPERATIONS

3.1. Function Description

PCLD-788 is a Relay Multiplexer Board which can be used to select one of sixteen input channels to output. When the multiplexer changes from channel A to channel B (see Fig. 3-1-1), 3 milliseconds break-before-make and 6 milliseconds channel-not-close will occur at this moment. CN5 is a connector which offers channel-close and channel-not-close signals output. The timing sequence is shown as following :

Fig. 3-1-1

Break-Before-Make Timing Diagram



When channel-close is low, do not measure signal through this multiplexer since the relay contacts are not stable.

3.2. Signal Connection

PCLD-788 can multiplex up to 16 analog input signals. Input channel selection and board selection are controlled by an 8 bit TTL/CMOS digital signal issued by the data acquisition control card.

CHAPTER 4: SOFTWARE PROGRAMMING

PCLD-788 is a Relay Multiplexer Daughter Board which can be connected with PCL-711, PCL-718, PCL-812 and PCL-860 which attach with D/O port and +5V, +12V power supply. A flat cable which has 20 pins always be used to connect from the board's Digital Output Port to PCLD-788 CN2 or CN3 (digital input). For instance following diagram is that PCL-860 be connected with PCLD-788 using 20 pin's flat cable :

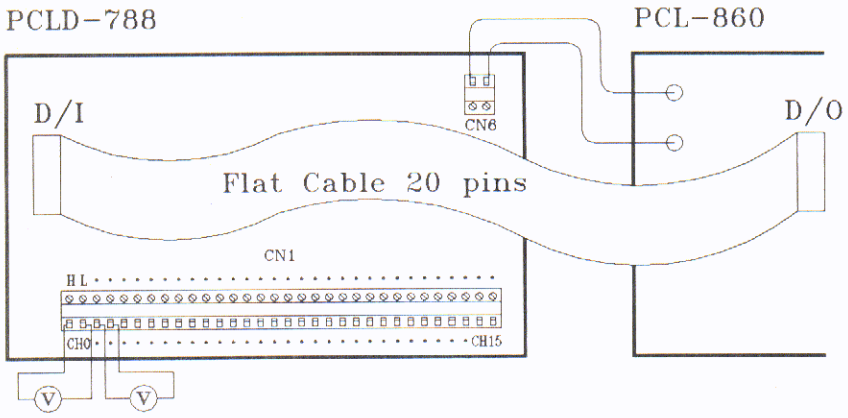


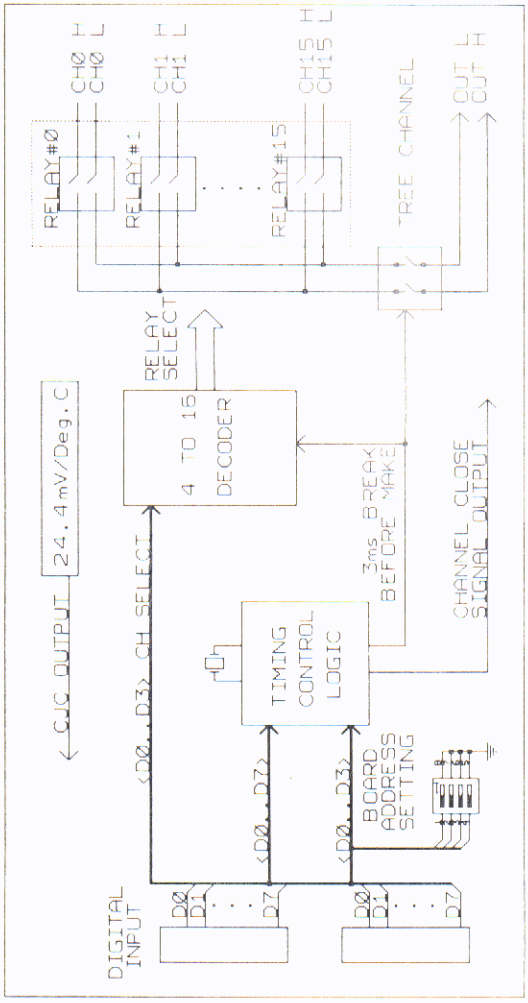
Fig. 4-1-1

In the above diagram shows that PCL-860 D/O PORT connect with PCLD-788 D/I PORT, so PCL-860 D/O PORT can use to control PCLD-788. The PCL-860 D/O PORT bit 0 to bit 3 select PCLD-788 channel and bit 4 to bit 7 select PCLD-788 address. Following is an example program shows how to program PCLD-788 :

```
/*    PCL-860   DVM Card      DEMO PROGRAM   3   */
/*  combine with PCL-788 example */
#include "stdio.h"
#include "conio.h"
#include "dos.h"
#include "time.h"
char dvm[5]="$DVM";
char volt[11];
main()
{
 FILE *f1;
 struct time timep;
 int  i;
 textbackground(1);
 clrscr();
 gotoxy(20,1);
 textcolor(11);
 cprintf("      PCL-860 Auto measurement system  \n");
 gotoxy(10,2);
 cprintf("=============================================================
          ===========\n");
 if((f1=fopen(dvm,"r+"))== NULL)     /* open $DVM driver */
    {
      printf("Can't open DVM.sys !\n");
      goto quit;
    }
 fprintf(f1,"set 20 v dc set speed 10 wait on hold on \n");
 fflush(f1);                 /* range : 20v DC */
 gotoxy(10,4);               /* speed : 2.5 reading/sec  */
 textcolor(13);
 cprintf("  Time      Channel 0  Voltage      Time      Channel 1
          Votage\n");
 gotoxy(10,5);
 cprintf("-----------------------------------------------------------
          ----------\n");
 textcolor(14);
 for(i=1;i<11;i++)
 {
 rewind(f1);
 fprintf(f1,"out lo 0\n");       /* PCL-788 channel 0 */
 /* delay(6); */          /* PCL-788 relay responce time 6 ms */
 fprintf(f1,"trig read value\n");
 rewind(f1);
 fgets(volt,10,f1);
 fflush(f1);
 gotoxy(12,i+6);
 gettime(&timep);
  c p r i n t f ( " % 2 d          % . 2 d : % . 2 d : % . 2 d
%s",i,timep.ti_hour,timep.ti_min,timep.ti_sec,volt);
 rewind(f1);
 fprintf(f1,"out lo 1 \n");
 /* delay(6); */
```

```
 fprintf(f1,"trig read value\n");
 rewind(f1);
 fgets(volt,10,f1);
 fflush(f1);
 rewind(f1);
 gotoxy(44,i+6);
 gettime(&timep);
  cprintf(" %2d        %.2d:%.2d:%.2d
%s",i,timep.ti_hour,timep.ti_min,timep.ti_sec,volt);
  }
 gotoxy(10,20);
 textcolor(13);
 cprintf("=========================  END
         ==============================");
quit:
 textbackground(0);
 textcolor(7);
 getch();
 clrscr();
}
```

APPENDIX A BLOCK DIAGRAM



APPENDIX B CONNECTOR, JUMPER AND VR LOCATIONS