CHAPTER 4. REGISTER STRUCTURE AND FORMAT

The PCL-812PG requires 16 consecutive addresses in I/O space. The most important issue in programming the PCL-812PG is understanding the meaning of the 16 registers addressable from the selected I/O port base address. A summary map of the functions of each address and the data format of each register are given in the following sections.

4.1. I/O Port Address Map

The following table shows the location of each register and driver relative to the base address, and its usage.

Location	Read	Write
Base + 0	Counter 0	Counter 0
+ 1	Counter 1	Counter 1
+ 2	Counter 2	Counter 2
+ 3	N/U*	Counter control
+ 4	A/D low byte	CH1 D/A low byte
+ 5	A/D high byte	CH1 D/A high byte
+ 6	D/I low byte	CH2 D/A low byte
+ 7	D/I high byte	CH2 D/A high byte
+ 8	N/U	Clear interrupt request
+ 9	N/U	Gain control
+10	N/U	MUX control
+11	N/U	Mode control
+12	N/U	Software A/D trigger
+13	N/U	D/O low byte
+14	N/U	D/O high byte
+15	N/U	N/U

* N/U = Not Used

4.2. A/D Data Registers

The A/D data registers use address BASE +4 and +5.

Data Format :

1. A/D Low byte and data.

BASE +4	D7	D6	D5	D4	D3	D2	D1	D0
	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

2. A/D High byte.

BASE +5	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	DRDY	AD11	AD10	AD9	AD8

Legend :

AD11 to AD0 - Analog to digital data. AD0 is the least significant byte (LSB) and AD11 is the most significant byte (MSB) of the A/D data.

DRDY - Data ready signal. When the A/D data is not ready, this bit is 1. This bit becomes 0 when A/D conversion completed and it is set to 1 when reading A/D low byte register BASE +4.

4.3. MUX Control Register

The Multiplexer control register is a write only register using address BASE +10. The low nybble provides the scan channel number. The multiplexer switches to the new channel when writing to this register.

Data Format :

BASE +10	D7	D6	D5	D4	D3	D2	D1	D0
Mux channel	X	X	X	X	CL3	CL2	CL1	CL0

Legend :

CL3 to CL0 - Multiplexer channel number.

4.4. Digital I/O Registers

The PCL-812PG offers 16 digital input channels and 16 digital output channels. These I/O channels use the input address BASE +6 and BASE +7. The output ports are at BASE +13 and BASE +14. The data format of each port is as follows :

Data Format :

BASE +6 (read port) D/I low byte	D7 DI7	D6 DI6	D5 DI5	D4 DI4	D3 DI3	D2 DI2	D1 DI1	D0 DI0
BASE +13 (write port) D/O low byte	D7 DO7	D6 DO6	D5 DO5	D4 DO4	D3 DO3	D2 DO2	D1 DO1	D0 DO0
BASE +7 (read port) D/I high byte	D7 DI15	D6 DI14	D5 DI13	D4 DI12	D3 DI11	D2 DI10	D1 DI9	D0 DI8
BASE +14 (write port) D/O high byte	D7 DO15	D6 DO14	D5 DO13	D4 DO12	D3 DO11	D2 DO10	D1 DO9	D0 DO8

4.5. D/A Output Registers

The D/A output registers are write registers using address BASE +4, +5, +6 and +7.

Data Format :

BASE +4	D7	D6	D5	D4	D3	D2	D1	D0
D/A #1 low byte	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
BASE +5	D7	D6	D5	D4	D3	D2	D1	D0
D/A #1 high byte	X	X	X	X	DA11	DA10	DA9	DA8

BASE +6	D7	D6	D5	D4	D3	D2	D1	D0
D/A #2 low byte	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
BASE +7	D7	D6	D5	D4	D3	D2	D1	D0
D/A #2 high byte	X	X	X	X	DA11	DA10	DA9	DA8

Legend :

DA11 to DA0 - Digital to analog data. DA0 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data. The register of the D/A low byte BASE +4 (BASE +6) is double buffered. The data is stored in a buffer when writing BASE +4 (BASE +6). When writing BASE +5 (BASE +7), the data in BASE +4 (BASE +6) is sent to D/A converter with high byte data at the same time.

4.6. Gain Control Register

The gain control register is a write-only register using address BASE +9. It is used to set the gain of the analog input programmable amplifier. The data format of this register and gain is defined as below :

Data Format :

BASE + 9	D7	D6	D5	D4	D3	D2	D1	D0
GAIN	X	X	X	X	X	R2	R1	R0

Gain Definition :

R2	R1	R0	GAIN
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Invalid

1	1	0	Invalid
1	1	1	Invalid

The analog input range, maximum input voltage and gain has the relation as the following equation :

$$\text{Analog input range} = \frac{\text{maximum input voltage}}{\text{gain}}$$

The maximum input voltage is selected by JP9. It can be +/- 5V or +/- 10V. The default maximum input voltage is +/- 5 volts. From this equation, the analog input ranges are +/-5V, +/-2.5V, +/-1.25V, +/- 0.625V and +/- 0.3125V.

4.7. Mode Control Register

The Mode control register is a write-only register using address BASE +11. This register provides the way to control on the operating modes of the PCL-812PG.

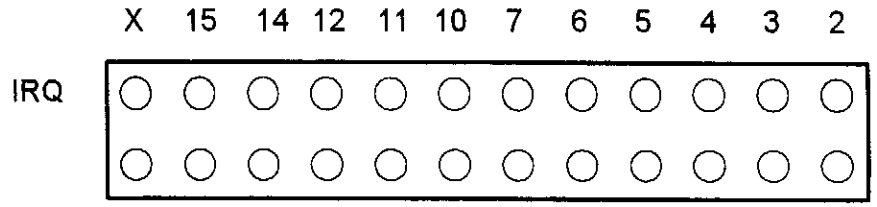
Data Format :

BASE +11	D7	D6	D5	D4	D3	D2	D1	D0
Control register	X	X	X	X	X	S2	S1	S0

A. Under internal trigger condition (JP1 is set to internal)

S2 S1 S0

0 0 0 : Disable software & pacer trigger.
0 0 1 : Enable software trigger and program transfer only. Power ON status.
0 1 0 : Enable pacer trigger and DMA transfer only
1 1 0 : Enable pacer trigger and program transfer or interrupt transfer. If using program transfer, the jumper JP4 must be set to the "X" position, as below :

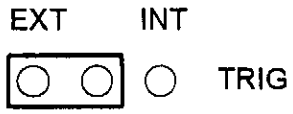


JP5 (IRQ)

B: Under external trigger source condition (JP1 is set to external)

S2	S1	S0	
0	0	X	Enable external trigger only
0	1	0	Enable external trigger and DMA trasfer data only
1	1	0	Enable program transfer and interrupt transfer using external trigger source. For program transfer, the jumper JP4 must be set to "X"

*Note: Set up trigger jumper JP1 on EXT as below before using external trigger mode:



JP1

4.8 Programmable Interval Timer/Counter Registers

The four registers located at address BASE 0, 1, 2 and 3 are used for Intel 8253 programmable timer/counter. Please refer to Chapter 8 or the 8253 product literature for detailed application information.

CHAPTER 5. A/D CONVERSION

This chapter provides a complete explanation of how to use the PCL-812PG A/D conversion functions. It covers A/D data format, input range selection, MUX multiplexer channel control, trigger modes and data transfer in the first five sections. The last section gives step by step implementation guidelines on A/D operations.

5.1. A/D Data Format and Status Register

When the PCL-812PG performs 12 bit A/D conversions, an 8 bit register is not big enough to accommodate all 12 bits of data. Therefore A/D data are stored in two registers located at address BASE +4 and BASE +5. The A/D low byte data are in the positions D0 (AD0) through D7 (AD7) of BASE +4 and high byte data are in the positions D0 (AD8) through D3 (AD11) of BASE +5. The least significant bit is AD0 and the most significant bit is AD11. The A/D channel number from which the conversion data derived is available at register BASE +10 position D0 (CL0) to D3 (CL3). The gain is set at register BASE + 9 position D0 (R0) to D2 (R2).

The data format of the A/D data registers is :

A/D Low byte and Channel number.

BASE	+4	D7	D6	D5	D4	D3	D2	D1	D0
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

A/D High byte.

BASE	+5	D7	D6	D5	D4	D3	D2	D1	D0
		0	0	0	DRDY	AD11	AD10	AD9	AD8

5.2. MUX Setting

Data Format :

BASE +10	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	CL3	CL2	CL1	CL0

5.3. Gain Setting

Data Format :

BASE +9	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	R2	R1	R0

5.4. Trigger Mode

The PCL-812PG A/D conversions can be triggered in any one of three ways - software trigger, on-board programmable pacer or external pulse trigger.

1. The software trigger is controlled by the application program issued software command. Writing to register BASE +12 with any value causes a software trigger. This trigger mode normally is not used in high speed A/D applications due to the limitations of the applications program execution time.

2. The PCL-812PG uses the INTEL 8253 programmable interval timer/counter. Counters 1 and 2 of the INTEL 8253 are configured to be a pacer to offer A/D converter trigger pulses with precise periods in the pacer trigger mode. The pacer output of the PCL-812PG is between 0.5 MHz and 35 minutes per pulse. Chapter 8 covers the details of using the INTEL 8253 timer/counter. The pacer trigger mode is ideal for interrupt and DMA data transfer which normally used in A/D applications requiring a higher conversion speed.

3. The PCL-812PG direct external trigger pulses are controlled through EXT.TRG (connector CN5 pin 1). This type of trigger mode is mostly used in A/D applications requiring A/D conversions not periodically but conditionally, e.g., thermocouple temperature control.

5.5. A/D Data Transfer

There are three possible ways to perform the PCL-812PG A/D data transfer - by program control, interrupt routine or DMA.

1. The program control data transfer uses the polling concept. After the A/D converter has been triggered, the application program checks the data ready (DRDY) bit of the A/D high byte register. If the DRDY bit is 0, the converted data is moved from the A/D data register to computer memory by application program control.

2. In interrupt routine transfer, data is transferred from the A/D data registers to a previously defined memory segment by the interrupt routine handler. At the end of each conversion, the data ready signal generates an interrupt which enables the interrupt handler routine to perform the transfer. The interrupt level selection on JP5, interrupt vector, interrupt controller 8259 and interrupt control bit in the PCL-812PG control register (BASE +11) must be specified before the use of interrupt routine. A write action to the A/D status register address (BASE +8) with any value resets the PCL-812PG interrupt request and re-enables the PCL-812PG interrupt.

3. Direct memory access (DMA) transfer moves the A/D data from the PCL-812PG hardware device to the PC system memory without operation of the system CPU. DMA is very useful in high speed data transfer, but it is complicated to operate. The DMA level selection jumper, JP5 and JP6, and the DMA enable bit in the PCL-812PG control register as well as the 8237 DMA controller registers must be set up before performing DMA operations. It is recommended that users use the PCL-812PG driver to perform DMA operation. For more information regarding the 8237 DMA controller and the PCL-812PG DMA operations, please read Chapter 9.

5.6. How to Execute an A/D Conversion

You may execute A/D operations with a program writing all I/O port instructions directly, or by a program utilizing the PCL-812PG driver. It is suggested that you invoke the driver functions in your program. This will make your programming job easier and enhance the program performance. See Software Drivers User's Manual for more information.

To perform pacer trigger and program control data transfer without the PCL-812PG driver.

Step 1 : Set the input channel by writing the channel number to the multiplexer control register BASE +10.

Step 2 : Set the analog input range by writing the gain control register BASE +9.

Step 3 : Set the pacer trigger mode by writing the mode control register.

Step 4 : Wait for data ready by checking the A/D high byte register (BASE +5) DRDY bit.

Step 5 : Read data from A/D converter by reading the A/D data registers (BASE +5 and BASE +4). Must first read high byte.

Step 6 : Data conversion by converting the binary A/D data to an integer.

CHAPTER 6. D/A CONVERSION

6.1. General Information

The PCL-812PG provides two D/A channels those use double buffered 12 bit multiplying D/A converters. The D/A registers are write registers using address BASE +4, +5, +6 and +7. DA0 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data. A summary of each register's data format is given below :

BASE +4	D7	D6	D5	D4	D3	D2	D1	D0
D/A #1 low byte	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
BASE +5	D7	D6	D5	D4	D3	D2	D1	D0
D/A #1 high byte	X	X	X	X	DA11	DA10	DA9	DA8
BASE +6	D7	D6	D5	D4	D3	D2	D1	D0
D/A #2 low byte	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
BASE +7	D7	D6	D5	D4	D3	D2	D1	D0
D/A #2 high byte	X	X	X	X	DA11	DA10	DA9	DA8

When writing to the D/A channels, please note that the low byte should be written first. It is then temporarily held by a register in the D/A and not released to the output. After the high byte is written, the low byte and high byte are added and passed to the D/A converter. This double buffering process protects the D/A data integrity through a single step update.

The PCL-812PG provides an internal precision fixed -5V or -10V reference. If this voltage is used as D/A input reference, the D/A output range will be 0 to +5V or 0 to +10V. You may select other external DC or AC sources as the D/A reference inputs. The maximum reference voltage is -10V and +10V, and the maximum D/A output range is 0 to +10V and 0 to -10V respectively.

Connector CN2 supports all D/A signal connections. The pin assignment of connector CN2 is described in Chapter 2, Section 2.3, Section 3.3 covers D/A signal connection, and gives an illustration of a wiring diagram.

6.2. D/A Applications

A variety of D/A operations can be supported by your PCL-812PG. For example the PCL-812PG can function as a digital attenuator by inputing variable AC or DC references, or can be used to generate arbitrary waveform outputs. As with the PCL-812PG programming, the D/A functions can be performed in two ways - by using the PCL-812PG driver functions in the application program, or writing I/O instructions to the registers directly.

CHAPTER 7. DIGITAL INPUT AND OUTPUT

The PCL-812PG provides 16 digital input channels and 16 digital output channels. These I/O channels use the input at address BASE +6 and BASE +7 and output registers at BASE +13 and BASE +14. A summary of each register's data format is listed below.

BASE +6 (read port) D/I low byte	D7	D6	D5	D4	D3	D2	D1	D0
	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
BASE +7 (read port) D/I high byte	D7	D6	D5	D4	D3	D2	D1	D0
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
BASE +13 (write port) D/O low byte	D7	D6	D5	D4	D3	D2	D1	D0
	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
BASE +14 (write port) D/O high byte	D7	D6	D5	D4	D3	D2	D1	D0
	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

It is fairly straight forward to use your PCL-812PG digital input and output functions. Attention should be paid to the pin assignments of connector CN3 (digital output) and connector CN4 (digital input). Section 3.4 offers some suggestions about digital signal connections.

CHAPTER 8. PROGRAMMABLE INTERVAL TIMER

8.1. The Intel 8253

The PCL-812PG uses the INTEL 8253 programmable interval timer/counter. The 8253 is a very popular timer/counter device consisting of three independent 16 bit down counters. Each counter has a clock input, control gate and an output. It can be programmed to act as one of six operation modes. The PCL-812PG provides a 2 MHz input frequency through an on-board crystal oscillator.

Counters 1 and 2 are cascaded and operated in fixed divider configuration. The counter 2 input is connected to the 2 MHz frequency and the output of counter 2 is connected to the input of counter 1. The output of counter 1 is internally configured to provide trigger pulses to the A/D converter. Counter 0 is not reserved by the PCL-812PG for any internal use, and you may access counter 0 through connector CN5. Please refer to Section 2-3 for details of the connector CN5 pin assignment.

8.2. Counter Read/Write and Control Registers

The 8253 programmable interval timer uses four registers at address BASE +0, 1, 2 and 3. The function of each register is :

BASE +0	Counter 0 Read/Write
BASE +1	Counter 1 Read/Write
BASE +2	Counter 2 Read/Write
BASE +3	Counter Control Word

Since the 8253 counter uses a 16 bit structure, each read/write data is split into the least significant byte and the most significant byte. It is important to ensure your read/write operations are in pairs and keep track of the byte order.

The data format of the control register is :

BASE +3	D7	D6	D5	D4	D3	D2	D1	D0
Control	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

Legend :

* SC1 & SC0 - Select Counter.

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Illegal

* RW1 & RW0 - Select the Read/Write operation.

RW1	RW0	Operation
0	0	Counter latch
0	1	Read/Write LSB
1	0	Read/Write MSB
1	1	Read/Write LSB first, then MSB.

* M2, M1 and M0 - Select the Operation Mode.

M2	M1	M0	Mode
0	0	0	0 - Interrupt on terminal count
0	0	1	1 - Programmable one shot
X	1	0	2 - Rate generator
X	1	1	3 - Square wave rate generator
1	0	0	4 - Software triggered strobe
1	0	1	5 - Hardware triggered strobe

* BCD - Select Binary or BCD Counting.

BCD	Type
0	Binary counter 16-bits
1	Binary coded decimal (BCD) counter (4 decades)

If it is set to be binary, the count can be any number from 0 up to 65535. If it is set to be BCD (binary coded decimal), the count can be set as any number from 0 to 9999.

8.3. Counter Operating Modes

8.3.1. Mode 0 - Interrupt on Terminal Count

The output will initially be low after setting this mode operation. After the count is loaded into the selected count register, the output will remain low and the counter will start to count. When the terminal count is reached, the output will go high and remain high until the selected counter is reloaded with the mode, or a new count is loaded. The counter continues to decrement after the terminal count has been reached. Rewriting a counter register during counting generates the following results :

1. Write the first byte stops the current counting.

2. Write the second byte starts the new count.

8.3.2. Mode 1 - Programmable One-Shot

The output will go low on the count following the rising edge of the gate input. The output will go high on the terminal count. If a new count value is loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable, thus the output will remain low for the full count after any rising edge of the gate input.

8.3.3. Mode 2 - Rate Generator

The output will be low for one period of the input clock. The period from one output pulse to the next is equal to the number of input counts in the counter register. If the counter register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Therefore the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until the count register is loaded and the output can also be synchronized by software.

8.3.4. Mode 3 - Square Wave Rate Generator

Similar to Mode 2, except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by one. Subsequent clock pulses decrement the count by two. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by three. Subsequent clock pulses decrement the count by two until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

8.3.5. Mode 4 - Software Triggered Strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

8.3.6. Mode 5 - Hardware Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable.

8.4. Counter Operations

8.4.1. Read/Write Operations

For each counter, the type of read/write operation, operating mode and counter type all must be properly specified in the control byte and the control byte must be written before the initial count is written.

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 & SC0), no instructions on the operating sequence are required. Any programming sequence following the 8253 conventions is acceptable.

There are three types of counter operation - read/load LCB, read/load MSB and read/load LSB followed by MSB. It is important to ensure your read/write operations are in pairs and keep track of the byte order.

8.4.2. Counter Latch Operation

It is often desirable to read the value of a counter without disturbing the count in progress. Usually the method used is the counter latch command method which allows the user to read the latched count value of the selected counter.

The 8253 supports counter latch operations in two ways. The first way is set the RW1 & RW0 to be (0,0) which latches the count of the selected counter in a 16 bit hold register. This method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the held value.

The second approach is to perform the latch operation by setting the MODE Register.

- Mode Register for Latching Count.

  A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

  SC1, SC0 - Specify counter to be latched.

  D5, D4 - 00 designates counter latching operation.

  X - Don't care

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

8.5. Counter Applications

The 8253 programmable interval timer/counter on your PCL-812PG interface card is a very useful device. In this section, two of the most popular usages of the 8253 timer/counter are introduced.

1. If you are using the A/D function of the PCL-812PG, the 8253 can be programmed to serve as a pacer to generate A/D trigger pulse.

2. Counter 0 of the 8253 is not reserved to any internal use. Users may configure Counter 0 to perform any 8253 supported functions, e.g., to act as a square wave generator.

CHAPTER 9. DIRECT MEMORY ACCESS

Direct memory access (DMA) improves system performance by allowing external devices to directly transfer information to or from the system memory without operation of the system CPU. The PCL-812PG is designed with A/D data DMA transfer capability. This feature significantly improves system performance during high speed A/D applications.

9.1. Introduction to The PC 8237 DMA Controller

DMA is controlled by the 8237 DMA controller chip on the PC's system board. It has four priority direct memory access channels. Channel 0 is reserved by the PC system to perform dynamic RAM refresh. Channel 2 is always assigned to support floppy disk operations. Channel 3 is normally used by the hard disk operations. Channel 1 is not reserved for any internal operations and is available for user applications.

Each channel has two control signals associated with it. The DMA request signal (DRQ) triggers a DMA operation, and the DMA acknowledge signal (DACK) authorizes the DMA to start data transfer.

In addition to four DMA channels, the 8237 DMA chip has four operating modes (single, demand, block and cascade) and four control registers. These registers are:

1. Operation mode register (set operation mode).
2. Address register (specify memory segment starting address).
3. Word count register (specify the number of transfers).
4. Initialization register (enable and disable DMA channels).

Please note that all four registers must be properly set up before the DMA operation can be requested.

9.2. How to Use DMA Transfer with The PCL-812PG

DMA transfer is a powerful but complicated operation. Different subjects regarding the DMA transfer have been covered in many chapters of this manual. The following is a summarization of how to use DMA transfer with the PCL-812PG. For detailed explanation on different subjects, please refer to the specific chapters.

1. During hardware configuration, check your PC DMA channel availability (level 1 or level 3) and set the PCL-812PG jumper JP5, JP6 (jumper) accordingly.

2. If you choose to use the PCL-812PG driver to support the DMA transfer programming, See Software Drivers User's Manual for more detailed information.

3. If you choose to conduct your own DMA operation, you need to have a solid understanding of the PC, 8237 DMA controller and the PCL-812PG device. To complete a DMA transfer, make sure you have covered the following operations.

    a. Initialize 8237 DMA controller register and page register.

    b. Set JP5 and JP6 to correct DMA channel.

    c. Send DMA enable and trigger source data to the PCL-812PG control register located at address BASE +11.

    d. Set up external trigger pulse or pacer trigger rate.

    e. Enable trigger source to start A/D conversion.

CHAPTER 10. CALIBRATION

In data acquisition and control, it is important to constantly calibrate your measurement device to maintain its accuracy. The default I/O port address setting in the program is Hex 220. Once the calibration program has been executed, it uses the graphic display and prompts to guide you through the calibration process.

In addition to the calibration program, it is necessary to have a 5 1/2 digit multimeter and a voltage calibrator or very stable and noise free DC voltage source to perform the calibration. A slot extension card will make your access to the VRs easier. The PC-LabCard product PCL-757 (ISA Bus Switch /Extension Card) is an ideal product to support the slot extension.

10.1. VR Assignment

There are 5 variable resistors (VR) on the PCL-812PG to allow you making accurate adjustment on A/D and D/A channels. The location of each VR is indicated in Fig. 2.1. The function of each VR is listed below :

VR1 : D/A 1 gain adjustment
VR2 : D/A 2 gain adjustment
VR3 : A/D gain adjustment
VR4 : Programmable amplifier offset adjustment
VR5 : A/D offset adjustment

10.2. A/D Calibration

Since the PCL-812PG provides many A/D input ranges, the calibration on one A/D range may cause a small offset on other ranges. It is suggested that you calibrate the A/D range which you need best accuracy.

The calibration program will prompt you to specify the following items :

1. Input range setting
2. Channel number

It then leads you to adjust the programmable amplifier offset, A/D offset, and A/D gain.

10.3. D/A Calibration

The D/A input reference should be connected to the channel to be calibrated. You may use the on-board -5V or -10V reference even external references. The full scale gain of each D/A channel are adjusted through different VR. The reading should be 4.9997V for the full scale gain.