PCI-1753/1753E
96/192-bit Digital I/O Card

User's manual

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CE Notification
The PCI-1753/1753E, developed by ADVANTECH CO., LTD., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

On-line Technical Support
For technical support and service please visit our support website at **http://support.advantech.com**

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CHAPTER 1

General Information

1.1 Introduction

The PCI-1753 is a 96-bit digital I/O card for the PCI bus, which can be extended to 192 digital I/O channels by connecting with its extension board, PCI-1753E. The card emulates mode 0 of the 8255 PPI chip, but the buffered circuits offer a higher driving capability than the 8255. The 96 I/O lines are divided into twelve 8-bit I/O ports: A0, B0, C0, A1, B1, C1, A2, B2, C2, A3, B3 and C3. Users can configure each port as input or output via software.

Easy to Install: Plug and Play

The PCI-1753 uses a PCI controller to interface the card to the PCI bus. The controller fully implements the PCI bus specification Rev 2.1. All bus relative configurations, such as base address and interrupt assignment, are automatically controlled by software.

Dry Contact Support for Digital Input

Each digital input channel at the PCI-1753/1753E accepts either 0 ~ 5 V_{DC} wet contact or dry contact inputs. This dry contact capability allows the channel to respond to changes in external circuitry (e.g., the closing of a switch in the external circuitry) when no voltage is present in the external circuit.

Reset Protection Fulfills the True Requirement of Industrial Applications

When the system is hot reset (the power is not turned off), the PCI-1753/1753E can either retain the last I/O port settings and outputs value, or return to its default configuration, depending on the jumper setting. This function protects the system from wrong operations during unexpected system resets.

Interrupt Functions Ensure Faster System Response

Two lines of each port C (i.e., ports C0, C1, C2 and C3) are connected to an interrupt circuit. The “Interrupt Control Register” of the PCI-

1753/PCI-1753E controls how these signals generate an interrupt. More than one interrupt request signals can be generated at the same time, and then the software can process these request signals by ISR. The multiple interrupt sources provide the card with more capability and flexibility.

The PCI-1753/1753E also provides “Pattern Match” interrupt function for port A0. The card monitors the states of port A0 and compares them with a pre-set pattern. When the received state matches the pre-set pattern, the PCI-1753/1753E generates an interrupt signal to the system.

“Change of State” interrupt function is provided at port B0. When any signal line of port B0 changes its state, the card generates an interrupt to the system to handle this event.

These interrupt functions release the CPU from the burden of pulling all I/O points, enabling a PC to handle more I/O points with higher performance.

Cost Savings for Increasing the Number of Input/Output Lines

Industrial users are needing more and more digital I/O lines to transmit data or to monitor/control outside devices. To meet this trend and to satisfy user’s budget considerations, Advantech has developed an extension board for the PCI-1753 called the PCI-1753E. The PCI-1753E has almost the same structure as the PCI-1753, without the interface controller. It shares PCI-1753’s interface controller through a 10-cm flat cable connecting, so users can spend less money while doubling the number of input/output lines.

Accessories for PCI-1753/1753E

The PCI-1753/1753E uses a 100-pin SCSI female connector. For easy signal wiring, a PCI-1753 can be connected to two ADAM-3968s by a 100-pin to 2x68-pin SCSI cable (part number PCL-10268). The ADAM-3968 allows easy access for wiring the individual pins of a 68-pin SCSI connector. An ADAM-3968/50 adapter board converts the 68-pin connector to two opto-22 compatible 50-pin box headers for connecting the PCI-1753/1753E to daughterboards, such as PCLD-782B and PCLD-785B.

1.2 Features

- 96/192 TTL digital I/O lines
- Emulates mode 0 of 8255 PPI
- Buffered circuits for higher driving capacity than 8255
- Multiple-source interrupt handling
- Interrupt output pin for simultaneously triggering external devices with the interrupt
- Output status read-back
- “Pattern match” and “Change of state” interrupt functions for critical I/O monitoring
- Keeps I/O setting and digital output values when hot system reset
- Supports dry contact and wet contact
- High-density 100-pin SCSI connector

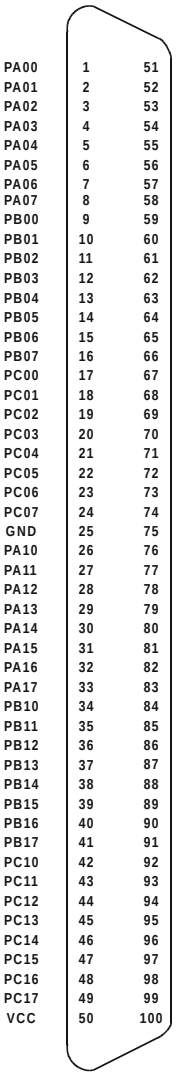
1.3 Applications

- Industrial AC/DC I/O devices monitoring and controlling
- Relay and switch monitoring and controlling
- Parallel data transfer
- TTL, DTL and CMOS logic signal sensing
- Indicator LED driving

1.4 Specifications

I/O Channels	96 digital I/O lines (PCI-1753 only) 192 digital I/O lines (using PCI-1753E extension)
Programming Mode	8255 PPI mode 0
Input Signal	Logic level 0: 0.8 V max. Logic level 1: 2.0 V min.
Output Signal	Logic level 0: 0.44 V max. @ 24 mA (sink) Logic level 1: 3.76 V min. @ 24 mA (source)
Transfer Rate	1.6 Mbytes/sec (tested under DOS, K6 300MHz CPU)
Power Consumption	+5 V @ 400 mA (typical) +5 V @ 2.7 A (max.)
Operating Temperature	0 ~ +60°C (32 ~ 140°F) (refer to IEC 68-2-1, 2)
Storage Temperature	-20 ~ +70°C (-4 ~ 158°F)
Operating Humidity	5 ~ 95%RH non-condensing (refer to IEC 68-2-3)
Connector	One 100-pin SCSI female connector
Dimensions	PCI-1753: 175 x 100 mm (6.9" x 3.9") PCI-1753E: 175 x 100 mm (6.9" x 3.9")
MTBF	over 75,013 hrs @ 25°C, ground fix environment

1.5 Pin Assignments



PA00	1	51	PA20
PA01	2	52	PA21
PA02	3	53	PA22
PA03	4	54	PA23
PA04	5	55	PA24
PA05	6	56	PA25
PA06	7	57	PA26
PA07	8	58	PA27
PB00	9	59	PB20
PB01	10	60	PB20
PB02	11	61	PB22
PB03	12	62	PB23
PB04	13	63	PB24
PB05	14	64	PB25
PB06	15	65	PB26
PB07	16	66	PB27
PC00	17	67	PC20
PC01	18	68	PC21
PC02	19	69	PC22
PC03	20	70	PC23
PC04	21	71	PC24
PC05	22	72	PC25
PC06	23	73	PC26
PC07	24	74	PC27
GND	25	75	GND
PA10	26	76	PA30
PA11	27	77	PA31
PA12	28	78	PA32
PA13	29	79	PA33
PA14	30	80	PA34
PA15	31	81	PA35
PA16	32	82	PA36
PA17	33	83	PA37
PB10	34	84	PB30
PB11	35	85	PB31
PB12	36	86	PB32
PB13	37	87	PB33
PB14	38	88	PB34
PB15	39	89	PB35
PB16	40	90	PB36
PB17	41	91	PB37
PC10	42	92	PC30
PC11	43	93	PC31
PC12	44	94	PC32
PC13	45	95	PC33
PC14	46	96	PC34
PC15	47	97	PC35
PC16	48	98	PC36
PC17	49	99	PC37
VCC	50	100	VCC

PA00 ~ PA07 : I/O pins of Port A0

PA10 ~ PA17 : I/O pins of Port A1

PA20 ~ PA27 : I/O pins of Port A2

PA30 ~ PA37 : I/O pins of Port A3

PB00 ~ PB07 : I/O pins of Port B0

PB10 ~ PB17 : I/O pins of Port B1

PB20 ~ PB27 : I/O pins of Port B2

PB30 ~ PB37 : I/O pins of Port B3

PC00 ~ PC07 : I/O pins of Port C0

PC10 ~ PC17 : I/O pins of Port C1

PC20 ~ PC27 : I/O pins of Port C2

PC30 ~ PC37 : I/O pins of Port C3

GND : Ground

VCC : +5V voltage output (1A max.)

1.6 Block Diagram

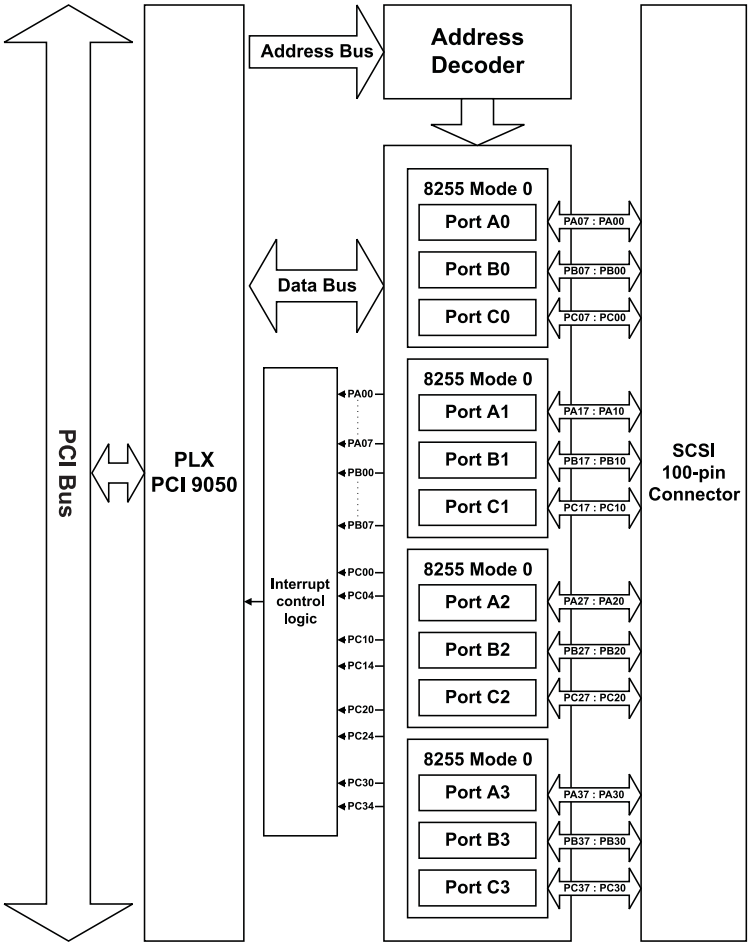


Figure 1-1: PCI-1753/1753E Block Diagram

CHAPTER 2

Installation

2.1 Initial Inspection

Before starting to install the PCI-1753/1753E, make sure there is no visible damage on the card. We carefully inspected the card both mechanically and electrically before shipment. It should be free of marks and in perfect order on receipt.

As you unpack the PCI-1753/1753E, check it for signs of shipping damage (damaged box, scratches, dents, etc.). If it is damaged or fails to meet its specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing materials for inspection by the carrier. We will then make arrangements to repair or replace the unit.

2.2 Unpacking

The PCI-1753/1753E contains components that are sensitive and vulnerable to static electricity. Discharge any static electricity on your body to ground by touching the back of the system unit (grounded metal) before you touch the board.

Remove the PCI-1753/1753E card from its protective packaging by grasping the card's rear panel. Handle the card only by its edges to avoid static discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, please store the card in this package for its protection.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

Check the product contents inside the packing. In PCI-1753's package, there should be one card, one CD-ROM, and this manual; in PCI-1753E's package, there should be one card and a 10-cm 20-pin flat cable. Please make sure nothing is missing.

2.3 Jumper Settings

We designed the PCI-1753/1753E with ease-of-use in mind. It is a "plug and play" card, i.e. the system BIOS assigns the system resources such as base address and interrupt automatically. There are only two functions with 17 jumpers on the PCI-1753, and one function with 16 jumpers on the PCI-1753E. The following section describes how to configure the card. You may want to refer to the figure below for help in identifying card components.

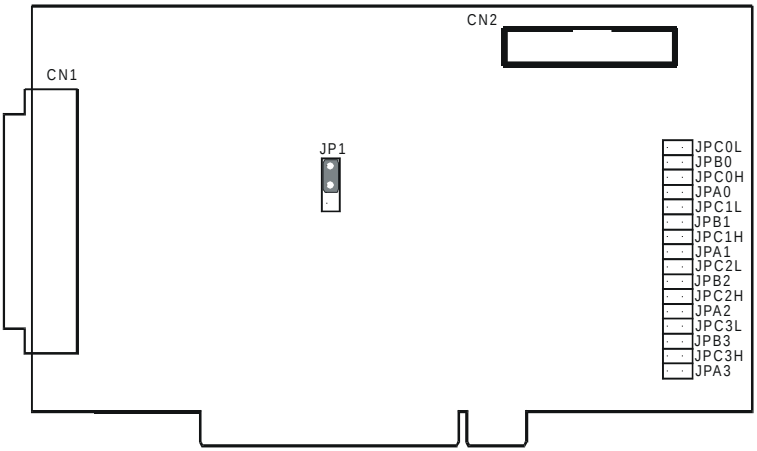


Figure 2-1: Location of connectors and jumpers

Jumper Settings to Set Ports as Input or Output by Software

When the two pins of jumpers JPA0, JPB0, JPC0L, JPC0H, JPA1, JPB1, JPC1L, JPC1H, JPA2, JPB2, JPC2L, JPC2H, JPA3, JPB3, JPC3L or JPC3H are not shorted (i.e., by setting a jumper), the corresponding ports are set to be configurable as input or output ports by software. (JPA0 means jumper for port A0, JPB0 means jumper for port B0, etc. See Table 2-1) If jumper JP1 is not enabled (i.e., by shorting the upper two pins of JP1), all ports configured by software are automatially set as input ports during system startup a reset, with a default signal level of logic 1(high). (But see Jumper JP1 discussion below.)

Using Jumpers to Set Ports as Output Ports

By shorting the two pins of the jumpers JPA0, JPB0, JPC0L, JPC0H, JPA1, JPB1, JPC1L, JPC1H, JPA2, JPB2, JPC2L, JPC2H, JPA3, JPB3, JPC3L or JPC3H, a user sets the corresponding ports to be output ports. (JPA0 means jumper for port A0, JPB0 means jumper for port B0, etc.) Shorting the two pins of a port's jumper disables the port from being software configurable as an input port. The initial state of each of these ports after system power on or reset will be logic 0 (voltage low), unless jumper JP1 determines otherwise. (See Jumper JP1 below.)

Jumper JP1 Restores Ports to Their Condition Prior to Reset

Jumper JP1 gives the PCI-1753/1753E a new and valuable capability. With JP1 enabled (i.e., by shorting the lower two pins of JP1), the PCI-1753/1753E "memorizes" all port I/O settings and output values, and, in the event of a "hot" reset, the settings and output values present at the port just prior to reset are restored to each port following reset. This feature applies to both ports set by software, and to ports configured as output ports via jumper. Depending on the application, this capability may allow a card to be reset without requiring a complete shutdown of processes controlled by the card (since port values are left unchanged and are interrupted only momentarily).

Complete loss of power to the chip clears chip memory. Thus, even if JP1 is enabled, if the power to the card is disconnected, the card's initial power-on state will be the state of an input port with voltage high input (for software-set ports) or the state of an output port with voltage low output (for jumper-set ports).

When jumper JP1 is not enabled (i.e., by shorting the upper two pins of JP1), both power-off and reset results in ports returning to the state of an input port with voltage high input (for software-set ports) or returning to the state of output port with voltage low output (for jumper-set ports).

Table 2-1: Summary of jumper settings

Names of Jumpers	Function description	
JPA0, JPA1, JPA2 and JPA3: Jumpers for ports A0, A1, A2 and A3 **JPB0, JPB1, JPB2 and JPB3**: Jumpers for ports B0, B1, B2 and B3 **JPC0L, JPC1L, JPC2L and JPC3L**: Jumpers for low nibble of ports C0, C1, C2 and C3 **JPC0H, JPC1H, JPC2H and JPC3H**: Jumpers for high nibble of ports C0, C1, C2 and C3		Sets port as an output port
		Sets port to be software configurable as input or output **(default)**
JP1		**Enables the reset protection function.** All ports return to the state held just prior to reset
		**Disables the reset protection function.** All ports return to the default state (for software-set) or to output port, output low (for jumper-set ports) **(default)**

2.4 Installation Instructions

The PCI-1753/1753E can be installed in any PCI slot in the computer. However, refer to the computer user's manual to avoid any mistakes and danger before you follow the installation procedure below:

1. Turn off your computer and any accessories connected to the computer.

Warning!: *TURN OFF your computer power supply whenever you install or remove any card, or connect and disconnect cables.*

2. Disconnect the power cord and any other cables from the back of the computer.
3. Remove the cover of the computer.
4. Select an empty 5 V PCI slot. (If you also need to intall the extension board, the PCI-1753E, to control more than 96 I/O points, please find two adjacent 5V PCI slots.) Remove the screw that secures the expansion slot cover to the system unit. Save the screw to secure the interface card retaining bracket.
5. Carefully grasp the upper edge of the PCI-1753. Align the hole in the retaining bracket with the hole on the expansion slot and align the gold striped edge connector with the expansion slot socket. Press the card into the socket gently but firmly. Make sure the card fits the slot tightly.

5.1. Repeat Step 5 for the PCI-1753E.

5.2. Connect the PCI-1753 and PCI-1753E with the 10-cm 20-pin flat cable, which is shipped with the PCI-1753E.

Caution!: *Please note that the first pin* of the cable connector should match the first pin* of the connector CN2 on the PCI-1753/1753E. (* first pin as marked by the arrow ▼ on each connector*

6. Secure the PCI-1753/1753E card by screwing the mounting bracket to the back panel of computer.
7. Attach any accessories (100-pin cable, wiring terminal board, etc.) to the card.
8. Replace the cover of your computer. Connect the cables you removed in step 2.
9. Turn the computer power on.

CHAPTER 3

Operation

3.1 Overview

This chapter describes the operating characteristics of the PCI-1753/1753E. The driver software bundled with this card allows a user to access all of the card's functions without register level programming. Please see the User's Manual included on the driver CD-ROM for more information. For users who prefer to implement their own bit-level programming to drive the card's functions, information useful for making such a program is included in this chapter.

3.2 Digital I/O Ports

3.2.1 Introduction

The PCI-1753 and 1753E each emulate four 8255 programmable peripheral interface (PPI) chips in mode 0, but with higher driving capability than a standard 8255 chip. Each of these 8255 chip emulators has 24 programmable I/O pins that are divided into three 8-bit ports. The total 96 digital I/O pins on either the PCI-1753 or the PCI-1753E are divided into 12 ports, designated PA0, PB0, PC0, PA1, PB1, PC1, PA2, PB2, PC2, PA3, PB3 and PC3. Each port can be programmed as an input or an output port. The I/O pins in port A0 are designated PA00, PA01,..., PA07; the pins in port B0 are designated PB00, PB01,..., PB07, etc. These port names are used both in this manual and in the software library. Please refer to Section 1.5, Pin Assignments.

3.2.2 8255 Mode 0

The basic 8255 mode 0 features included on the PCI-1753/1753E cards are:

- 8-bit I/O ports - port A (PA) and port B (PB)
- Port C is divided into two nibble-wide (4-bit) I/O ports - PC upper and PC lower
- Any port can be used for either input or output.
- Output status can be read back.

3.2.3 Input/Output Control

A control word can be written to a port's configuration register (Base+3, 7, 11 and 15 respectively for ports 0, 1, 2 and 3 on the PCI-1753, and Base+35, 39, 43 and 47 respectively for ports 0, 1, 2 and 3 on the PCI-1753E) to set the port as an input or an output port, unless the ports are set as output ports via jumpers (refer to Section 2.3, Jumper Settings). Table 3-1 shows the format of a control word.

Table 3-1: Bit map of port configuration register

D7	D6	D5	D4	D3	D2	D1	D0
Not read	Not read	Not read	Port A 0: output 1: input	Port C upper bits 0: output 1: input	Not read	Port B 0: output 1: input	Port C lower bits 0: output 1: input

Note!: *A control word has no effect if the corresponding port is set as an output port by a jumper.*

Warning! *Before setting any port as an output port via software, make sure that a safe output value has also been set. An output voltage will appear at the pins immediately following the control word taking effect. If no output value was specified, the value will be indeterminate (either 0 or 1), which may cause a dangerous condition.*

3.2.4 Initial Configuration

The initial configuration of each port depends on the input/output jumper setting of each port, on the setting of the jumper JP1, and on whether the power was actually disconnected or whether the system was hot reset.

If jumper JP1 is not enabled, all ports configured by software are automatically set as input ports during system start up or reset, with a default signal level of logic 1 (high). All ports set via jumpers as output ports are set as output ports during system start up or reset, signal level logic 0 (0 V).

If the jumper JP1 is enabled and the initial configuration is caused by a reset, all ports will return to the states they had just prior to the reset. The reset must be a "hot" reset (power not disconnected) for enabled JP1 to return ports to their prior values. Otherwise, the card behaves as though JP1 were not enabled. Please refer to "Jumper settings" in **Chapter 2** for more information.

3.2.5 Dry Contact Support for Digital Input

Each digital input channel accepts either dry contact or 0 ~ 5 V_{DC} wet contact inputs. Dry contact capability allows the channel to respond to changes in external circuitry (e.g., the closing of a switch in the external circuitry) when no voltage is present in the external circuit. Figure 3-1 shows external circuitry with both wet and dry contact components, connected as an input source to one of the card's digital input channels.

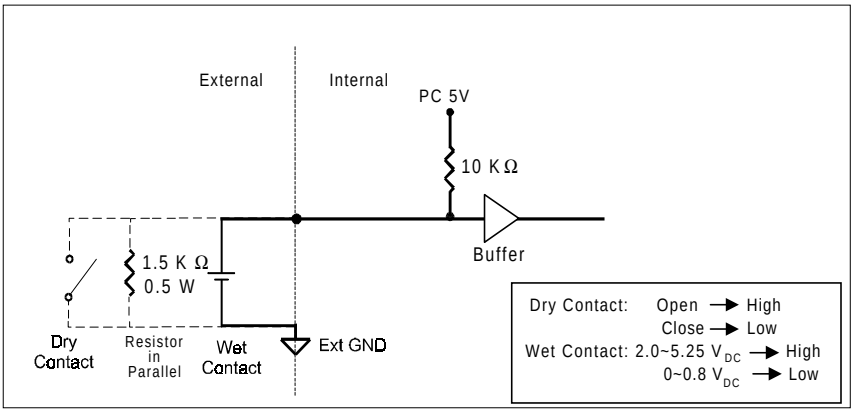


Figure 3-1: Wet and dry contact inputs

Note!: *For wet contact configurations, a malfunction may occur if the internal resistance of the voltage source is significant (> 1.5 kΩ). It is advisable to connect a 1.5 kΩ resistor in parallel with such a voltage source to avoid a voltage rise inside the voltage source.*

3.3 Interrupt Functions

3.3.1 Introduction

Two lines of each I/O port C, plus ports A0 and B0, are connected to the interrupt circuitry. The “Interrupt Control Register” of the PCI-1753/1753E controls how the combination of these signals generates an interrupt. Six interrupt request signals can be generated at the same time, and then the software can service these six request signals by IRQ. The multiple interrupt sources provide the card with more capability and flexibility.

3.3.2 IRQ Level

The IRQ level is set automatically by the PCI plug-and-play BIOS and is saved in the PCI controller. There is no need for users to set the IRQ level. Only one IRQ level is used by this card, although it has six interrupt sources.

3.3.3 Interrupt Control Registers

The “Interrupt Control Registers” (Base + 16, 17, 18 and 19 for the PCI-1753, and Base + 48, 49, 50 and 51 for the PCI-1753E) control the interrupt signal sources, edges and flags. The following table shows the bit map of each interrupt control register. These registers are readable/writable. When writing to one of them, it is used as a control register, and when reading from it, it is used as a status register.

Table 3-2: Interrupt control register bit map

Base+16/48	Port 0							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F0	E0	M01	M00	F02	M2	F01	M1
Base+17/49	Port 1							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F1	E1	M11	M10	-	-	-	-
Base+18/50	Port 2							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F2	E2	M21	M20	-	-	-	-
Base+19/51	Port 3							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F3	E3	M31	M30	-	-	-	-

Mn0 and Mn1: "mode bits" of port Cn (n = 0 ~ 3)

M1: pattern match port enable control bit of port A0

M2: change of state port enable control bit of port B0

En: triggering edge control bit (n = 0 ~ 3)

Fn: interrupt flag bit of port Cn (n = 0 ~ 3)

F01: pattern patch interrupt flag bit of port A0

F02: change of state interrupt flag bit of port B0

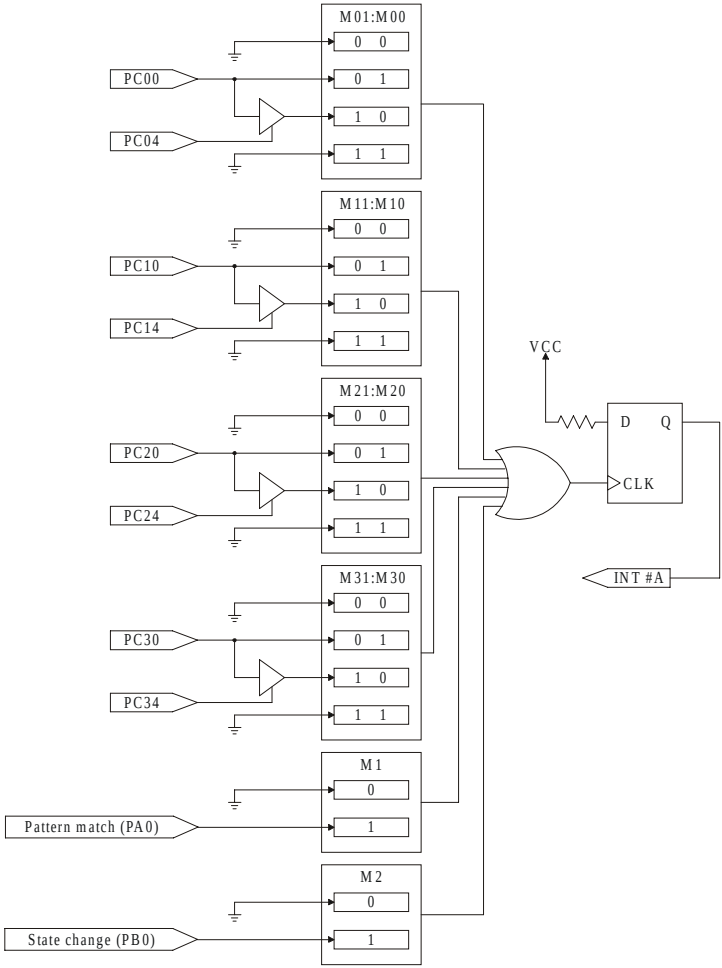


Figure 3-2: Interrupt sources

3.3.4 Interrupt Source Control

The “mode bits” in the interrupt control registers determine the allowable sources of signals generating an interrupt. For the PCI-1753, bit 4 and bit 5 of Base+16 determines the interrupt source of port C0, bit 4 and bit 5 of Base+17 determines the interrupt source for port C1, and so forth. Because of sharing the same PCI controller with the PCI-1753, the PCI-1753E’s interrupt sources are also controlled by the PCI-1753’s interrupt control register. Bit 4 and bit 5 of Base+48 determines the interrupt source of port C0 on the PCI-1753E, bit 4 and bit 5 of Base+49 determines the interrupt source of port C1, and so forth. Please refer the table in Appendix A to find the corresponding address for the interrupt source control of each port C.

The following table shows the relationship between an interrupt source and the values in the mode bits.

Table 3-3: Interrupt mode bit values

Base+16/48		**Port 0**	**Base+17/49**		**Port 1**
M01	M00	Description	M11	M10	Description
0	0	Disable interrupt	0	0	Disable interrupt
0	1	Source = PC00	0	1	Source = PC10
1	0	Source = PC00 and PC04	1	0	Source = PC10 and PC14
1	1	Disable interrupt	1	1	Disable interrupt
Base+18/50		**Port 2**	**Base+19/51**		**Port 3**
M21	M20	Description	M31	M30	Description
0	0	Disable interrupt	0	0	Disable interrupt
0	1	Source = PC20	0	1	Source = PC30
1	0	Source = PC20 and PC24	1	0	Source = PC30 and PC34
1	1	Disable interrupt	1	1	Disable interrupt

3.3.5 Interrupt Triggering Edge Control

The interrupt can be triggered by a rising edge or a falling edge of the interrupt signal, selectable by the value written in the "triggering edge control" bit in the interrupt control register, as shown in following table.

Table 3-4: Triggering edge control bit values

En (n = 0 ~ 3)	Triggering edge of interrupt signal
1	Rising edge trigger
0	Falling edge trigger

3.3.6 Interrupt Flag Bit

The "interrupt flag" bit is a flag indicating the status of an interrupt. It is a readable and writable bit. Read the bit's value to find the status of the interrupt; write "1" to this bit to clear the interrupt. This bit must be cleared in the ISR to service the next incoming interrupt.

Table 3-5: Interrupt flag bit values

F01, F02 and Fn (n = 0 ~ 3)		**Interrupt Status**
Read	1	Interrupt exists
	0	No interrupt
Write	1	Clear interrupt
	0	Don't care

F01: pattern patch interrupt flag bit of port A0

F02: change of state interrupt flag bit of port B0

Fn: interrupt flag bit of port Cn (n = 0 ~ 3)

3.3.7 Pattern Match Interrupt Function

The PCI-1753/1753E provides the pattern match interrupt function for port A0. It monitors the status of the enabled input channels, which are chosen in Base+24 (or Base+56 for the PCI-1753E), and compares the received state values with the pre-set state values written in Base+20 (Base+52 for the PCI-1753E). When the actual state values match the pre-set state values, the PCI-1753 will deliver an interrupt signal to the system. This function releases the CPU from the burden of polling all of the I/O points, enabling a PC to handle more I/O points with higher performance. The following is an example.

Example 3.1 Assume that the pattern match function for the I/O channels PA01, PA02, PA06 and PA07 of the PCI-1753 is enabled (i.e. PA00, PA03, PA04 and PA05 on the PCI-1753 and port A0 on the PCI-1753E are ignored during the pattern match monitoring process). The user can set the pattern match values for the enabled input channels, and these will be compared to the actual channel states of the enabled channels. The following is an example.

a) First, enable the pattern match interrupt function for channels PA01, PA02, PA06 and PA07

Bit #	7	6	5	4	3	2	1	0
Base+24	1	1	0	0	0	1	1	0

b) Write the pre-set pattern-match state of the enabled channels

Bit #	7	6	5	4	3	2	1	0
Base+20	1	0	X	X	X	1	1	X

c) Finally, enable the pattern match function for port A0 of the PCI-1753 by writing a “1” in bit 0 of Base+16.

M1	Description
1	Enable the pattern match interrupt function for port A0
0	Disable the pattern match interrupt function for port A0

d) When the input signals at channels PA01, PA02 and PA07 are high and PA06 is low, an interrupt signal will be generated. This result is not affected by the states of channels PA00, PA03, PA04 and PA05.

3.3.8 Change of State Interrupt Function

The PCI-1753/1753E also provides the change of state interrupt function for port B0. It monitors the status of the enabled channels of port B0, which are chosen in Base+28 (or Base+60 for the PCI-1753E). When one of the enabled channels changes its state, the PCI-1753 delivers an interrupt signal to the system to handle this event. The following is an example.

Example 4.2 Assume that the change of state interrupt function for the I/O channels PB01, PB02, PB06 and PB07 on the PCI-1753E are enabled (i.e. the signals in PB00, PB03, PB04 and PB05 on the PCI-1753E and port B0 of the PCI-1753 are ignored during the change of state process). When a change of state occurs in either PB01 or PB02 or PB06 or PB07, an interrupt signal will be delivered to the system.

a) First, enable the change of state interrupt function for PB01, PB02, PB06 and PB07 of the PCI-1753E.

Bit #	7	6	5	4	3	2	1	0
Base+60	1	1	0	0	0	1	1	0

b) Then, enable the change of state interrupt function for port B0 of the PCI-1753E by writing a “1” in bit 2 of Base+48.

M2	Description
1	Enable the change of state interrupt function for port A0
0	Disable the change of state interrupt function for port A0

c) When a change of state occurs in PB01 or PB02 or PB06 or PB07 on the PCI-1753E, an interrupt signal is generated.

APPENDIX A

Register Format of PCI-1753/1753E

A.1 PCI-1753 Register Format

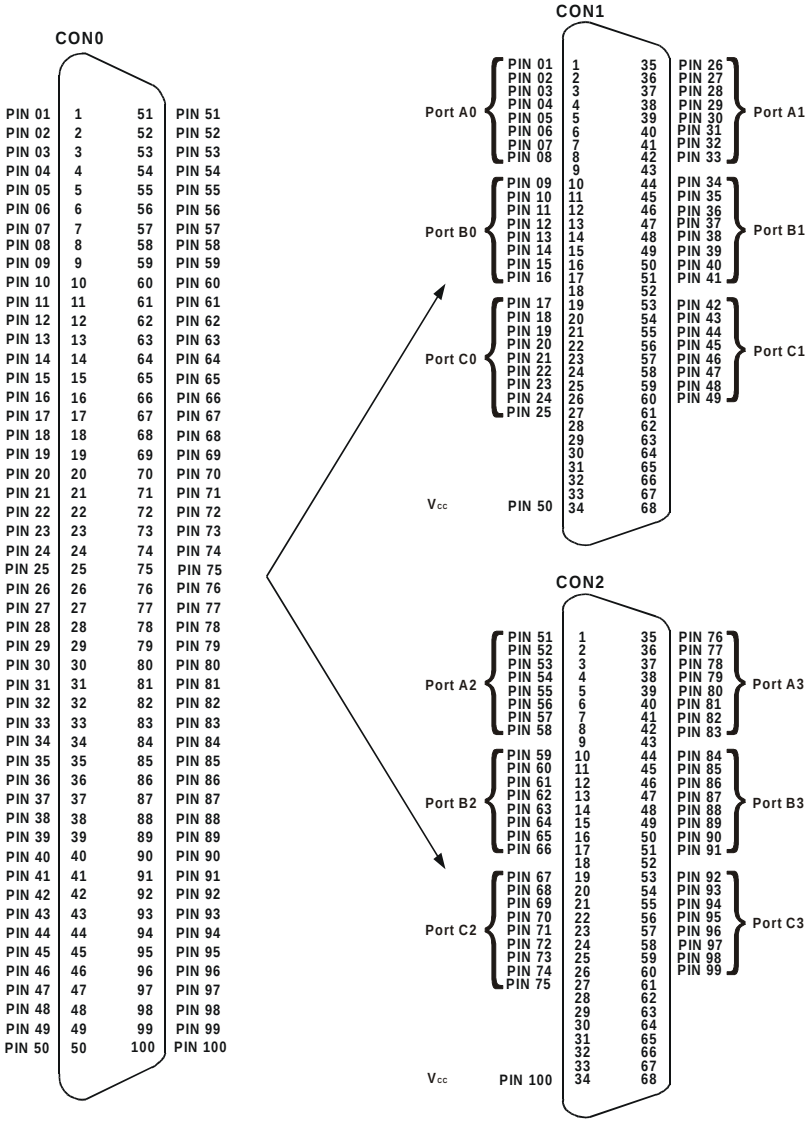
Base Address + (Decimal)	Function	
	Read	Write
0	Port A0	Port A0
1	Port B0	Port B0
2	Port C0	Port C0
3		Port 0 Configuration Register
4	Port A1	Port A1
5	Port B1	Port B1
6	Port C1	Port C1
7		Port 1 Configuration Register
8	Port A2	Port A2
9	Port B2	Port B2
10	Port C2	Port C2
11		Port 2 Configuration Register
12	Port A3	Port A3
13	Port B3	Port B3
14	Port C3	Port C3
15		Port 3 Configuration Register
16	Interrupt Control Register for Port 0	Interrupt Control Register for Port 0
17	Interrupt Control Register for Port 1	Interrupt Control Register for Port 1
18	Interrupt Control Register for Port 2	Interrupt Control Register for Port 2
19	Interrupt Control Register for Port 3	Interrupt Control Register for Port 3
20		Pattern Match Value Register for Port A0
24		Pattern Match Enable Register for Port A0
28		Change of State Enable Register for Port B0

A.2 PCI-1753E Register Format

Base Address + (Decimal)	Function	
	Read	Write
32	Port A0	Port A0
33	Port B0	Port B0
34	Port C0	Port C0
35		Port 0 Configuration Register
36	Port A1	Port A1
37	Port B1	Port B1
38	Port C1	Port C1
39		Port 1 Configuration Register
40	Port A2	Port A2
41	Port B2	Port B2
42	Port C2	Port C2
43		Port 2 Configuration Register
44	Port A3	Port A3
45	Port B3	Port B3
46	Port C3	Port C3
47		Port 3 Configuration Register
48	Interrupt Control Register for Port 0	Interrupt Control Register for Port 0
49	Interrupt Control Register for Port 1	Interrupt Control Register for Port 1
50	Interrupt Control Register for Port 2	Interrupt Control Register for Port 2
51	Interrupt Control Register for Port 3	Interrupt Control Register for Port 3
52		Pattern Match Value Register for Port A0
56		Pattern Match Enable Register for Port A0
60		Change of State Enable Register for Port B0

APPENDIX B

Pin Assignments of Cable PCL-10268



* CON0, CON1 and CON2 are female Connectors