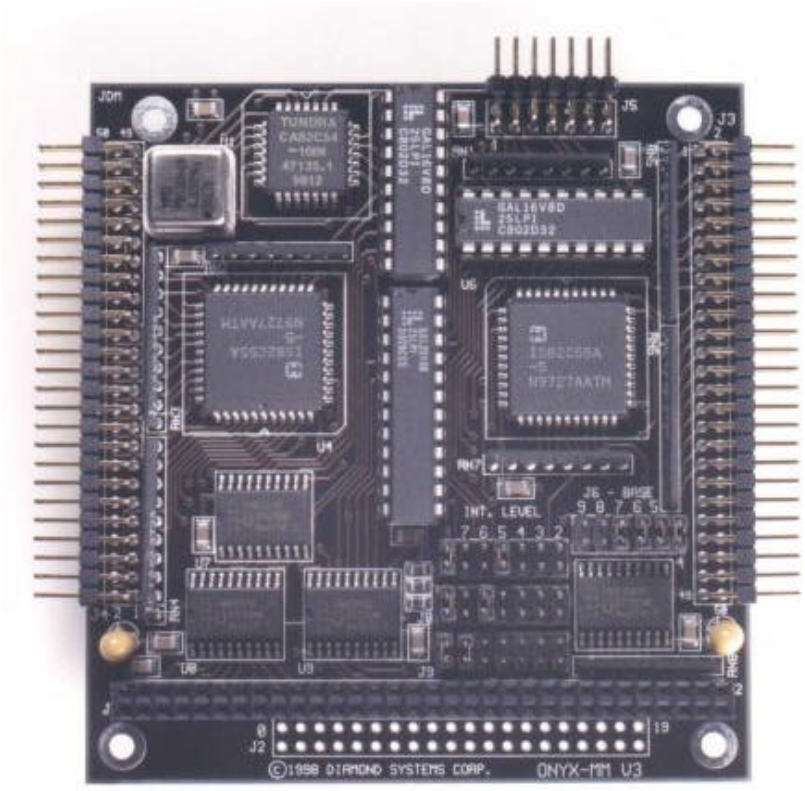
DIAMOND SYSTEMS CORPORATION

ONYX-MM-XT

PC/104 Format
Counter/Timer & Digital I/O Module
User Manual V1.4



Diamond Systems Corporation
8430-D Central Ave.
Newark, CA 94560 USA
Tel (510) 456-7800
Fax (510) 456-7878
techinfo@diamondsystems.com

Table of Contents

1. General Information and Features

ONYX-MM is a PC/104-compliant I/O module with 48 digital I/O lines, 3 16-bit counter/timers, and 3 interrupts. It is an 8-bit module, so it does not contain the 16-bit expansion bus connector. This connector is available as an option by requesting the –B16 suffix when ordering.

Three right-angle pin headers are provided for I/O. Two identical 50-pin (2x25) headers contain 24 digital I/O lines each and +5/ground, and a third 14-pin (2x7) header provides the counter/timer signals, external interrupt pin, and +5/ground. J2, with 24 digital I/O lines, is on the right side of the module in the standard PC/104 I/O position. J3, with 24 additional digital I/O lines, is on the left side of the module, and J4, with the counter/timer and interrupt signals, is on the top edge of the module. (The bottom edge of the module is defined as the edge with the PC/104 ISA bus connectors.)

All I/O signals are TTL compatible.

The boards operate on +5V power supply only.

Digital I/O

48 TTL digital I/O lines are provided by 2 82C55 chips (24 per chip). Each line can source 2.5mA in a logic 0 state and sink 2.5mA in a logic 1 state. I/O lines are unbuffered, i.e. there is a direct connection between the 82C55 and the I/O header. Bit C0 of each 82C55 can be used to generate an interrupt on the PC bus (see **Interrupts** below).

All digital I/O lines are connected to +5V through 10K pull -up resistors.

Digital I/O lines are accessed through two 50-pin headers, J3 and J4, with 24 lines (one 82C55) on each header. See page 8 for I/O header pinouts.

Counter/Timer I/O

Onyx-MM contains three 16-bit counter/timers provided by an 82C54 chip. Each counter/timer has an input pin, a gate pin, and an output pin. The input pin responds to positive edges. The gate pin is active high; a counter will count whenever its associated gate pin is high and will not count when the gate pin is low. The input and gate pins are connected to +5V through 10K pull -up resistors.

Counter/timer I/O lines are accessed through a 14-pin header J5. See page 8 for the pinout of J5.

An on-board oscillator provides a 4MHz clock that can be used to drive any counter. Each counter has a maximum input rate of 10MHz.

Programmable features include input source selection and counter cascading:

Counter 0 input can be either IN0 from the I/O header or 4MHz.
Counter 1 input can be either IN1, 4MHz, or Counter 0 output.
Counter 2 input can be either IN2, 4MHz, or Counter 1 output.

All three counter outputs can be programmed to generate PC bus interrupts as described below. With appropriate configuration, two or three counters can be cascaded to form a 32-bit or 48-bit counter, and the output of this cascaded counter can generate an interrupt.

Interrupts

ONYX-MM provides a means to generate up to three active-high interrupt signals on the PC/104 bus. Three pin headers are provided to select interrupt levels for each interrupt signal. Interrupt levels 2 through 7 are available on each header.

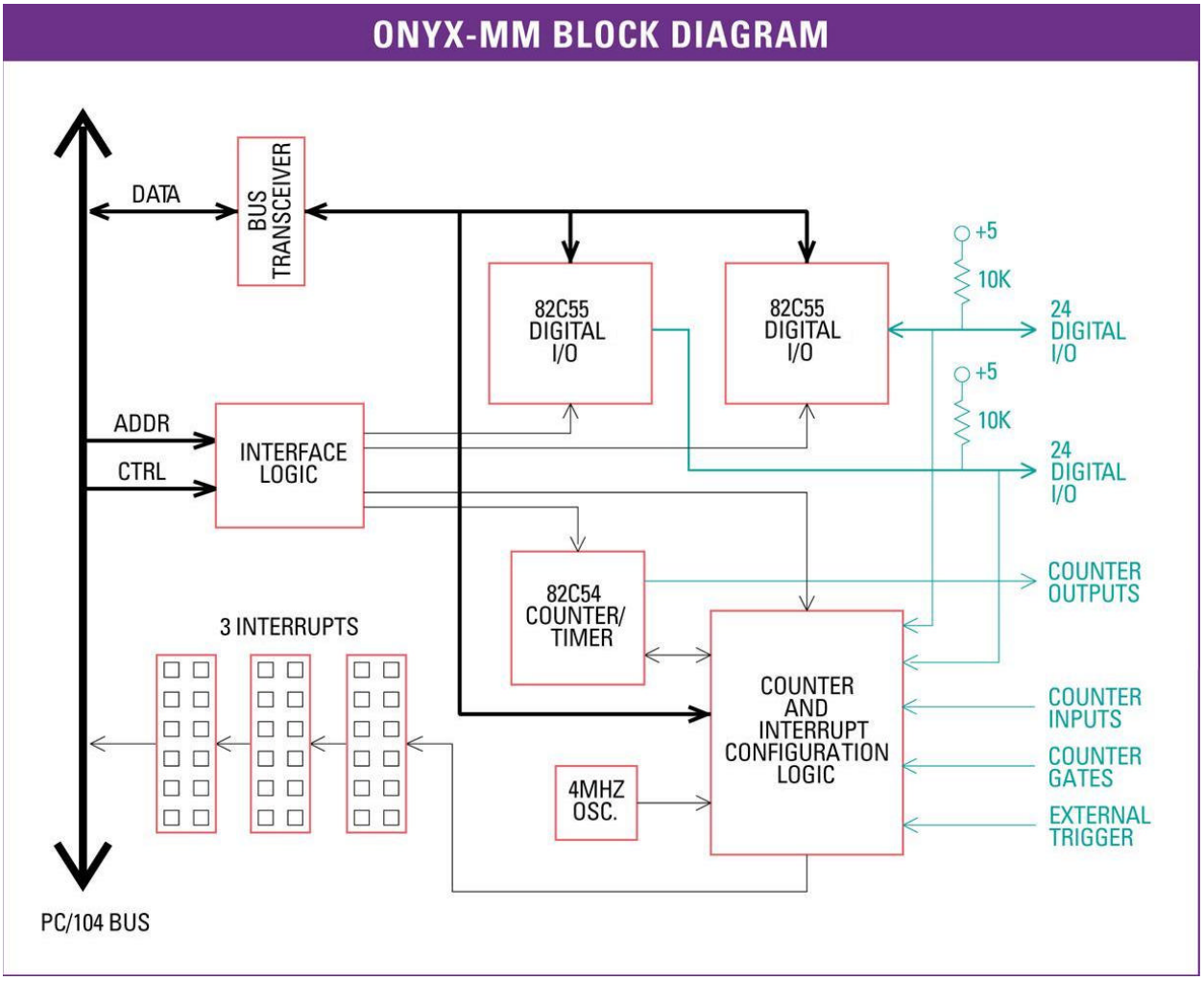
To enable interrupt sharing, a 1K pull-down resistor can be jumpered to each interrupt line, and interrupt signals are driven by tristate drivers. When an interrupt is pending, the interrupt line is driven high, and when it is not pending, the output is in high-impedance mode, and the 1K resistor pulls it down to a logic 0 state.

Interrupt sources are programmable. Interrupts can be generated from both digital I/O and counter/timer signals as follows:

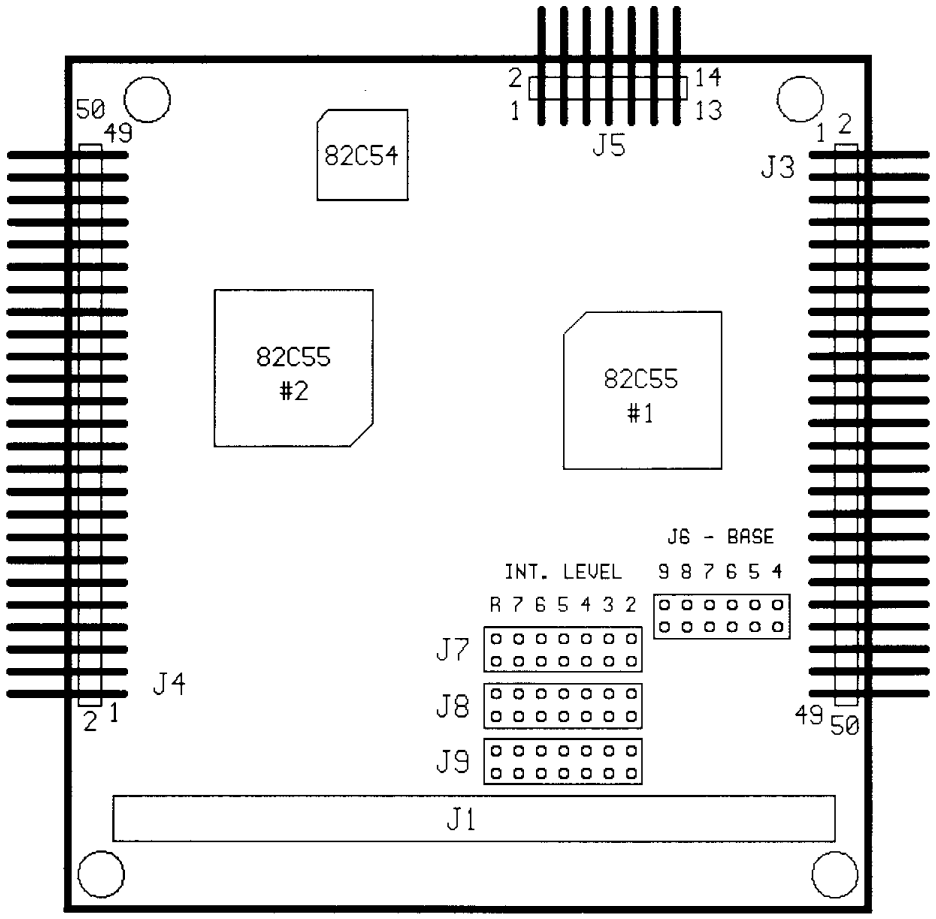
Interrupt no. 1:	Bit C0 from 82C55 #1 or Counter 0 output
Interrupt no. 2:	Bit C0 from 82C55 #2 or Counter 1 output
Interrupt no. 3:	External interrupt pin or Counter 2 output

Interrupts are enabled and disabled under software control by manipulating a control register.

Block Diagram



2. Onyx-MM Board Drawing



Item	Description
J1	PC/104 bus connector
J3	Digital I/O ports 1A, 1B, 1C
J4	Digital I/O ports 2A, 2B, 2C
J5	Counter/timer signals
J6	Board base address configuration
J7	Interrupt 0 configuration
J8	Interrupt 1 configuration
J9	Interrupt 2 configuration

3. I/O Header Pinouts

J3: Digital I/O Header for 82C55 #1
J4: Digital I/O Header for 82C55 #2

Each of these headers is identical in pinout. They provide 24 digital I/O lines, +5, and ground. Pin 1 of J3 is in the upper right corner of the board, and pin 1 of J4 is in the lower left corner.

A7	1	2	Gnd
A6	3	4	Gnd
A5	5	6	Gnd
A4	7	8	Gnd
A3	9	10	Gnd
A2	11	12	Gnd
A1	13	14	Gnd
A0	15	16	Gnd
C7	17	18	Gnd
C6	19	20	Gnd
C5	21	22	Gnd
C4	23	24	Gnd
C3	25	26	Gnd
C2	27	28	Gnd
C1	29	30	Gnd
C0	31	32	Gnd
B7	33	34	Gnd
B6	35	36	Gnd
B5	37	38	Gnd
B4	39	40	Gnd
B3	41	42	Gnd
B2	43	44	Gnd
B1	45	46	Gnd
B0	47	48	Gnd
+5	49	50	Gnd

J5: Counter/Timer and Interrupt Header

This header is a 14-pin header with all counter/timer signals, the external interrupt pin, +5, and ground.

In 0	1	2	In 1
Gate 0	3	4	Gate 1
Out 0	5	6	Out 1
In 2	7	8	External Interrupt
Gate 2	9	10	Gnd
Out 2	11	12	Gnd
+5	13	14	Gnd

4. Base Address Configuration

ONYX-MM's base address is set with header J6, located at the lower right corner of the board. Each of the six pairs of pins on J6 corresponds to a different address bit. A pair left open is equal to a 1, and a pair with a jumper installed is equal to a 0. The header is used to select address bits 9-4, resulting in an 16-byte I/O decode. The leftmost pair selects address bit A9, and the rightmost pair selects address bit A4. Although any 16-byte location is selectable, certain locations are reserved or may cause conflicts. The table below lists recommended base address settings for ONYX-MM. The default setting is 300 Hex. "Open" means an open position, and "Inst" means a position with a jumper installed.

Base Address		**Header J6 Position**					
Hex	**Decimal**	**9**	**8**	**7**	**6**	**5**	**4**
220	544	Open	Inst	Inst	Inst	Open	Inst
240	576	Open	Inst	Inst	Open	Inst	Inst
250	592	Open	Inst	Inst	Open	Inst	Open
260	608	Open	Inst	Inst	Open	Open	Inst
280	640	Open	Inst	Open	Inst	Inst	Inst
290	656	Open	Inst	Open	Inst	Inst	Open
2A0	672	Open	Inst	Open	Inst	Open	Inst
2B0	688	Open	Inst	Open	Inst	Open	Open
2C0	704	Open	Inst	Open	Open	Inst	Inst
2D0	720	Open	Inst	Open	Open	Inst	Open
2E0	736	Open	Inst	Open	Open	Open	Inst
300	768 (Default)	Open	Open	Inst	Inst	Inst	Inst
330	816	Open	Open	Inst	Inst	Open	Open
340	832	Open	Open	Inst	Open	Inst	Inst
350	848	Open	Open	Inst	Open	Inst	Open
360	864	Open	Open	Inst	Open	Open	Inst
380	896	Open	Open	Open	Inst	Inst	Inst
390	912	Open	Open	Open	Inst	Inst	Open
3A0	928	Open	Open	Open	Inst	Open	Inst
3C0	960	Open	Open	Open	Open	Inst	Inst
3E0	992	Open	Open	Open	Open	Open	Inst

5. Interrupt Configuration

Each interrupt signal has its own configuration jumper block. The jumper block configures the interrupt level and the 1K Ohm pull-down resistor. A pull-down resistor is required on each active interrupt line on the PC/104 bus. Only one resistor should be installed per interrupt level for the entire system.

J7: Interrupt #0
J8: Interrupt #1
J9: Interrupt #2

Position	**Function**	**Open**	**Jumper**
R	1K Ohm Resistor	No pulldown	Pulldown (max 1 per level)
7	IRQ7		
6	IRQ6	Install only one jumper in each header	
5	IRQ5	in any of these 6 locations	
4	IRQ4	to select the interrupt level	
3	IRQ3		
2	IRQ2		

All three interrupt sources can be set to the same level if desired. However only one pulldown resistor should be installed for each interrupt level.

6. Register Map

Base +	Function	Comments
0	DIO port 1A	0 - 3 are 82C55 #1 registers
1	DIO port 1B	
2	DIO port 1C	
3	DIO port 1 configuration register	
4	DIO port 2A	4 - 7 are 82C55 #2 registers
5	DIO port 2B	
6	DIO port 2C	
7	DIO port 2 configuration register	
8	Counter/timer 0 data	8 - 11 are 82C54 registers
9	Counter/timer 1 data	
10	Counter/timer 2 data	
11	Counter/timer mode configuration register	
12	Counter/timer input configuration register	
13	(maps to register 12)	
14	Interrupt configuration register	
15	(maps to register 14)	

Note that locations 12 and 13 both map to the same physical register on Onyx-MM. Likewise locations 14 and 15 both map to the same physical register on the board.

7. Register definitions

Base + 0: Digital I/O Register A, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1A7	1A6	1A5	1A4	1A3	1A2	1A1	1A0

1A7-1A0 Digital I/O port 1A, port A on 82C55 no. 1

Base + 1: Digital I/O Register B, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0

1B7-1B0 Digital I/O port 1B, port B on 82C55 no. 1

Base + 2: Digital I/O Register C, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1C7	1C6	1C5	1C4	1C3	1C2	1C1	1C0

1C7-1C0 Digital I/O port 1C, port C on 82C55 no. 1

Base + 4: Digital I/O Register A, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2A7	2A6	2A5	2A4	2A3	2A2	2A1	2A0

2A7-2A0 Digital I/O port 2A, port A on 82C55 no. 2

Base + 5: Digital I/O Register B, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2B7	2B6	2B5	2B4	2B3	2B2	2B1	2B0

2B7-2B0 Digital I/O port 2B, port B on 82C55 no. 2

Base + 6: Digital I/O Register C, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2C7	2C6	2C5	2C4	2C3	2C2	2C1	2C0

2C7-2C0 Digital I/O port 2C, port C on 82C55 no. 2

Base + 3: Digital I/O Configuration Register, 82C55 no. 1

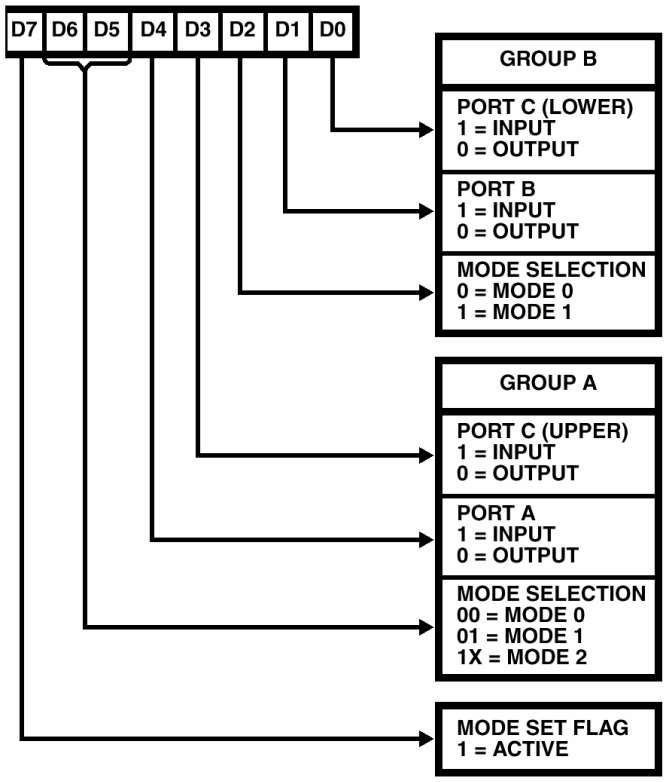
Base + 7: Digital I/O Configuration Register, 82C55 no. 2

These control registers determine the direction and mode of the 82C55 digital I/O lines. The diagram below comes from the 82C55 chip datasheet which is included at the back of this manual. Base + 3 is the control register for chip 1, and Base + 7 is the control register for chip 2.

Most applications use the simple I/O configuration in which bit 7 is set to 1 and the Mode is set to 0 for all ports.

Here is a list of common configuration register control bytes:

Configuration Byte				
Hex	**Decimal**	**Port A**	**Port B**	**Port C (both halves)**
9B	155	Input	Input	Input
92	146	Input	Input	Output
99	153	Input	Output	Input
90	144	Input	Output	Output
8B	139	Output	Input	Input
82	130	Output	Input	Output
89	137	Output	Output	Input
80	128	Output	Output	Output



Base + 8: Counter/Timer 0 Data

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Divisor bits 7-0 or 15-8

Base + 9: Counter/Timer 1 Data

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Divisor bits 7-0 or 15-8

Base + 10: Counter/Timer 2 Data

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Divisor bits 7-0 or 15-8

Base + 11: Counter/Timer Configuration

The diagram below is from the 82C54 datasheet which is included at the back of this manual.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

The registers described below are built in to the Onyx-MM circuitry and are separate from the 82C55 and 82C54 chips. In the register maps below, blank locations are unused. See the accompanying schematic diagrams on the following pages.

Base + 12: Counter/timer input configuration register

Bit	7	6	5	4	3	2	1	0
Name				S21	S20	S11	S10	S0

S21 - S20 Counter 2 input select:

S21	S20	Input source
0	0	In2
0	1	4MHz oscillator
1	X	Out1

S11 - S10 Counter 1 input select:

S11	S10	Input source
0	0	In1
0	1	4MHz oscillator
1	X	Out0

S0 Counter 0 input select
0 In0
1 4MHz oscillator

Base + 14: Interrupt configuration register

Bit	7	6	5	4	3	2	1	0
Name			SRC2	SRC1	SRC0	INTE2	INTE1	INTE0

SRC2 Interrupt source 2:
0 External interrupt pin
1 Counter 2 output

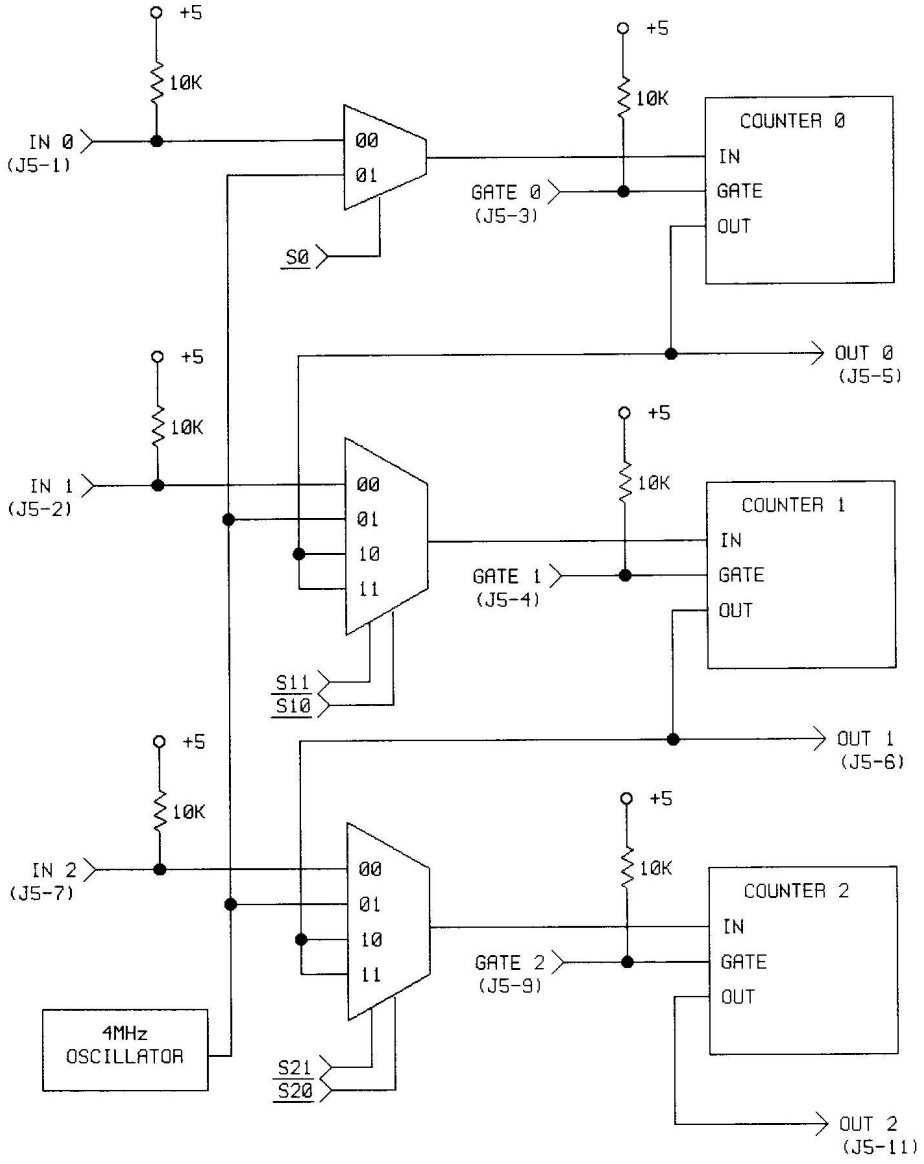
SRC1 Interrupt source 1:
0 Bit C0 from 82C55 #2 (base + 6, bit 0)
1 Counter 1 output

SRC0 Interrupt source 0:
0 Bit C0 from 82C55 #1 (base + 2, bit 0)
1 Counter 0 output

INTE2 - 0 Interrupt enable signals
0 Disabled
1 Enabled

8. Counter/Timer Circuit Schematic

The schematic below illustrates the counter/timer configuration and how the counter/timer input configuration register controls it. See the control register description on page 12.

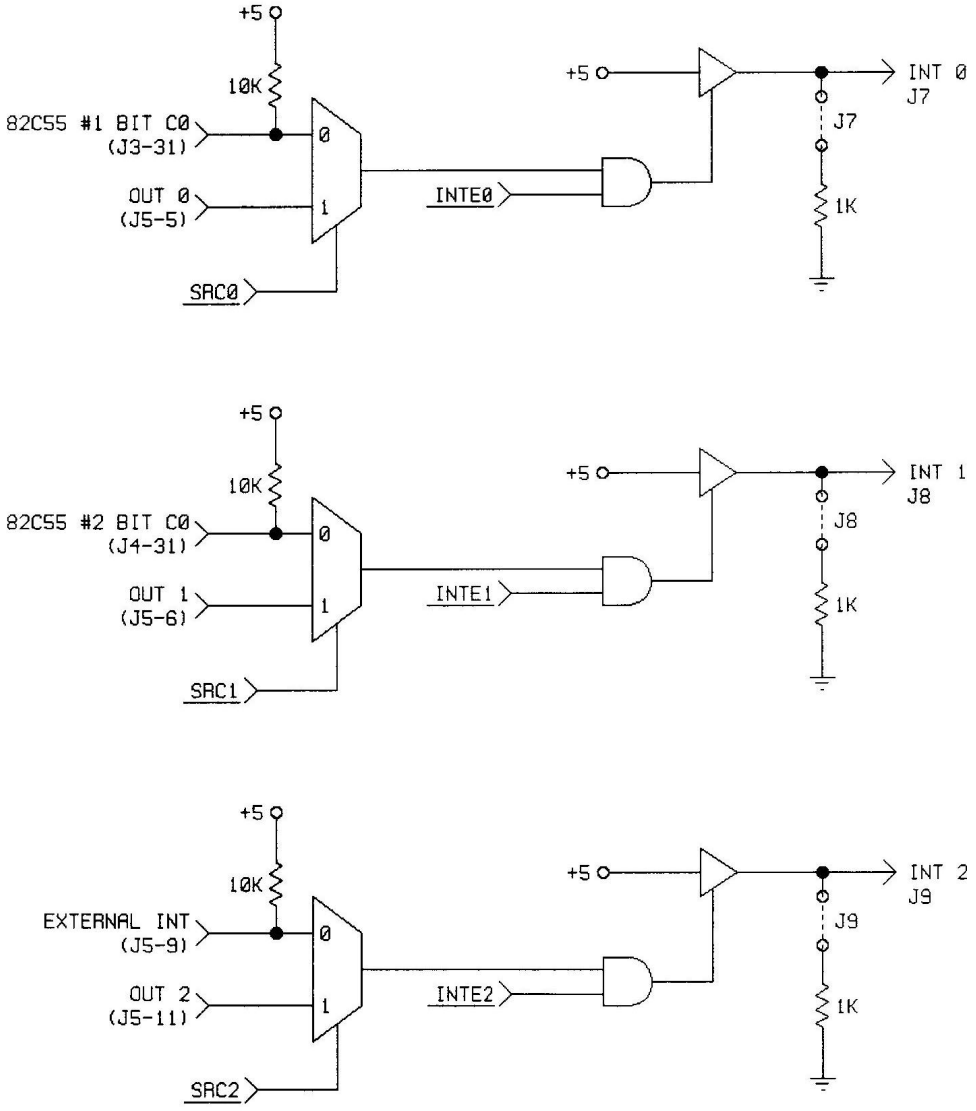


S20 UNDERLINE INDICATES CONTROL REGISTER BIT

(J5-11) PARENTHESES INDICATE I/O HEADER AND PIN NO.

9. Interrupt Circuit Schematic

The schematic below illustrates the interrupt circuit configuration and how the interrupt configuration register controls it. See the control register description on page 12.



10. Specifications

Counter/Timer Circuitry

Chip	82C54-2
Counter/timers	3, 16 bits wide
Maximum input frequency	10MHz
On-board oscillator	4MHz ± .01% (100 ppm)
Signal type	TTL
Input voltage, all inputs:	
Low	-0.5V min, 0.8V max
High	2.0V min, 5.5V max
Input current	-200 A max (low), 2 A max (high)
Output voltage, all outputs:	
Low	0.0V min, 0.4V max
High	3.0V min, Vcc - 0.4V max
Output current	±2.5mA max, each line
Pullup resistors	10K all input lines

Digital I/O Circuitry

Chip	82C55A (x2)
Number of I/O lines	48
Direction	All lines programmable for input or output in groups of 4/8
Input voltage:	
Low	-0.5V min, 0.8V max
High	2.0V min, 5.5V max
Output voltage:	
Low	0.0V min, 0.4V max
High	3.0V min, Vcc - 0.4V max
Output current	±2.5mA max, each line
Pullup resistors	10K all lines

Interrupt Circuitry

No. of interrupts	3
Pull-down resistor	1K resistor selectable via jumper on each interrupt
Interrupt levels	2 - 7

General

Dimensions	3.550” x 3.775”
Power supply (Vcc)	5.0VDC ±10%, 200mA typical (all outputs open)
Card type	8-bit PC/104 bus compliant
Temperature range	-40 - +85^{o}C, operating and storage

82C55A

CMOS Programmable Peripheral Interface

June 1998

Features

- **Pin Compatible with NMOS 8255A**
- **24 Programmable I/O Pins**
- **Fully TTL Compatible**
- **High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88**
- **Direct Bit Set/Reset Capability**
- **Enhanced Control Word Read Capability**
- **L7 Process**
- **2.5mA Drive Capability on All I/O Ports**
- **Low Standby Power (ICCSB) 10μA**

Ordering Information

PART NUMBERS		PACKAGE	TEMPERATURE RANGE	PKG. NO.
5MHz	8MHz			
CP82C55A-5	CP82C55A	40 Ld PDIP	0^oC to 70^oC	E40.6
IP82C55A-5	IP82C55A		-40^oC to 85^oC	E40.6
CS82C55A-5	CS82C55A	44 Ld PLCC	0^oC to 70^oC	N44.65
IS82C55A-5	IS82C55A		-40^oC to 85^oC	N44.65
CD82C55A-5	CD82C55A	40 Ld CERDIP	0^oC to 70^oC	F40.6
ID82C55A-5	ID82C55A		-40^oC to 85^oC	F40.6
MD82C55A-5/B	MD82C55A/B		-55^oC to 125^oC	F40.6
8406601QA	8406602QA	SMD#		F40.6
MR82C55A-5/B	MR82C55A/B	44 Pad CLCC	-55^oC to 125^oC	J44.A
8406601XA	8406602XA	SMD#		J44.A

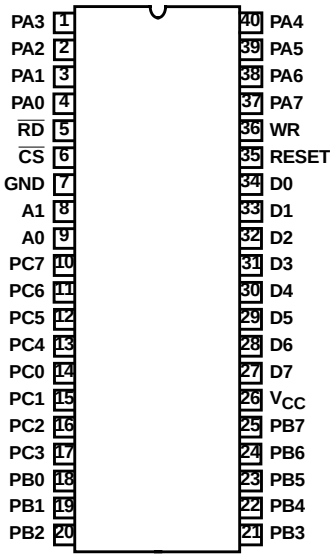
Description

The Intersil 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

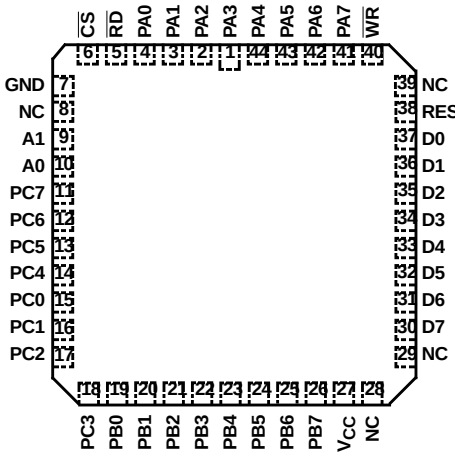
Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Intersil advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Pinouts

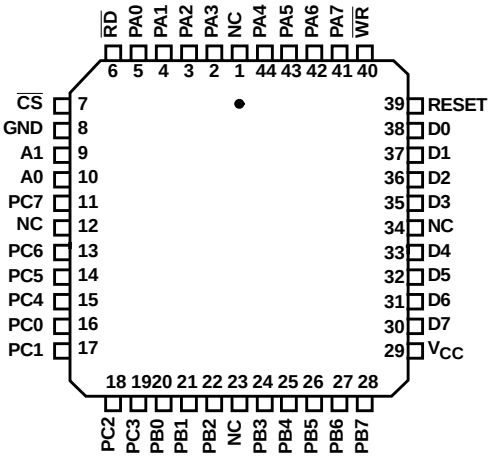
82C55A (DIP)
TOP VIEW



82C55A (CLCC)
TOP VIEW



82C55A (PLCC)
TOP VIEW

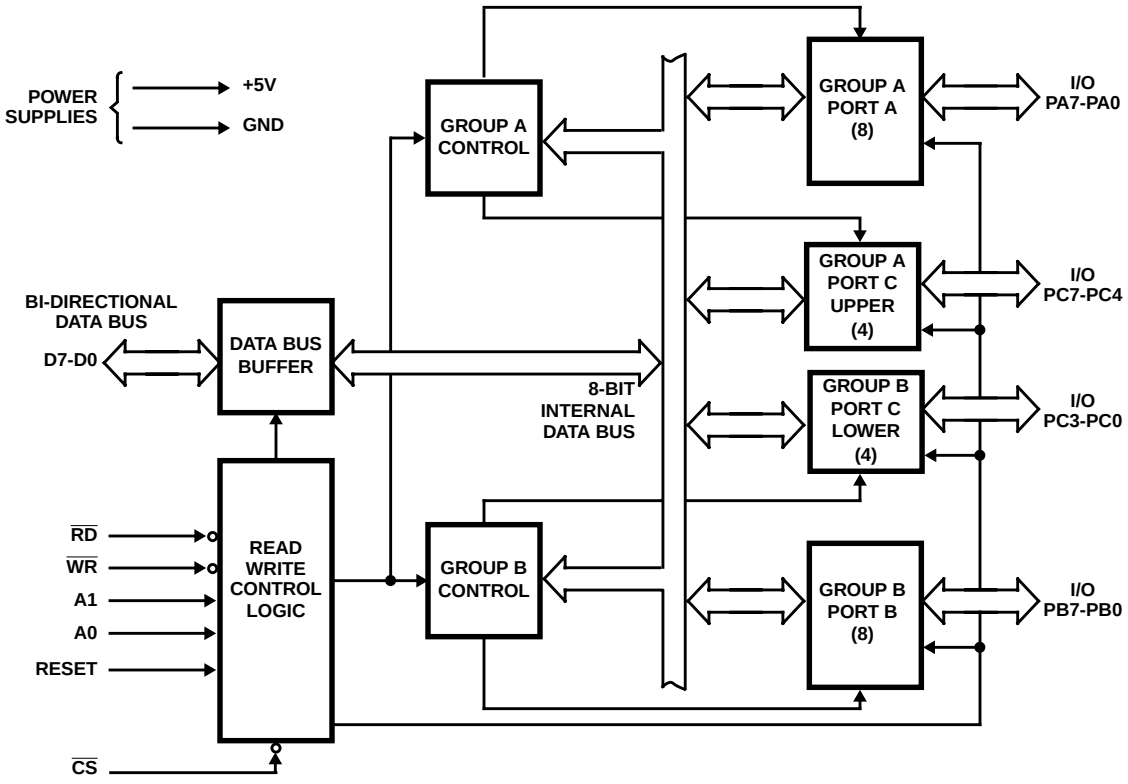


File Number **2969.2**

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the “Bus Hold” circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Functional Diagram



Functional Description

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A “low” on this input pin enables the communcation between the 82C55A and the CPU.

(RD) Read. A “low” on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to “read from” the 82C55A.

(WR) Write. A “low” on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

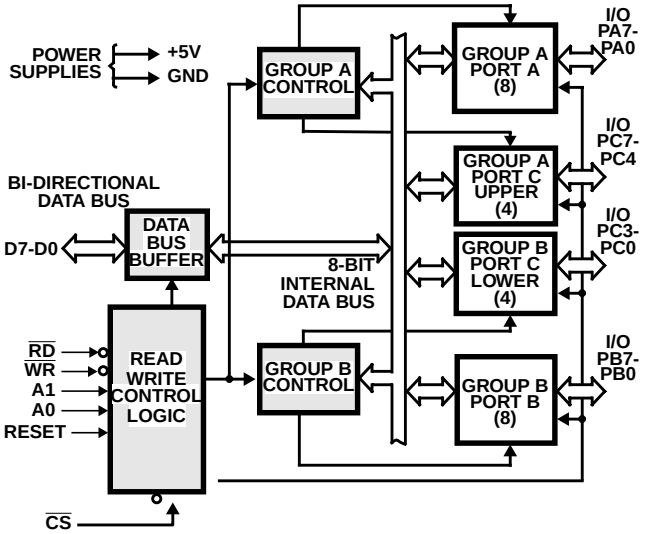


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A “high” on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. “Bus hold” devices internal to the 82C55A will hold the I/O port inputs to a logic “1” state with a maximum hold current of 400µA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the 82C55A. The control word contains information such as “mode”, “bit set”, “bit reset”, etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the “Basic Operation” table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.

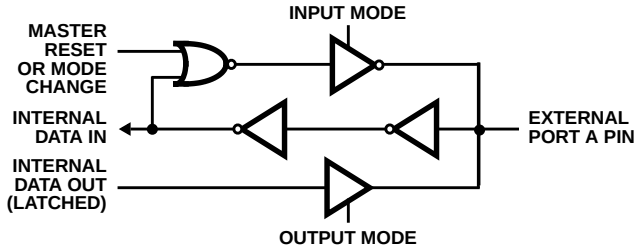


FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

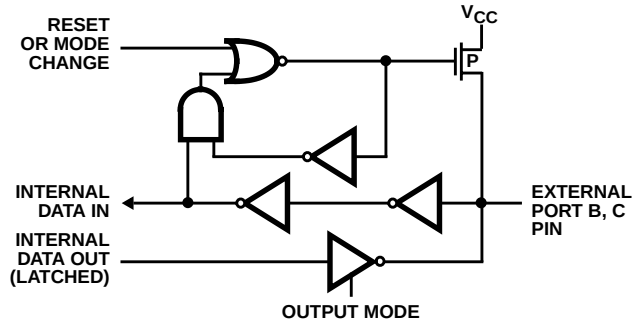


FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pull-down resistors in all-CMOS designs. The control word register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.

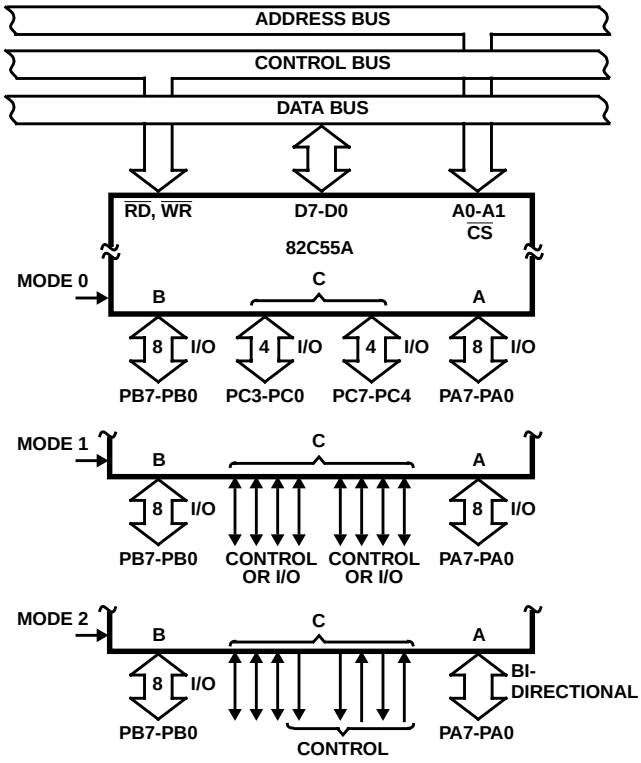


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

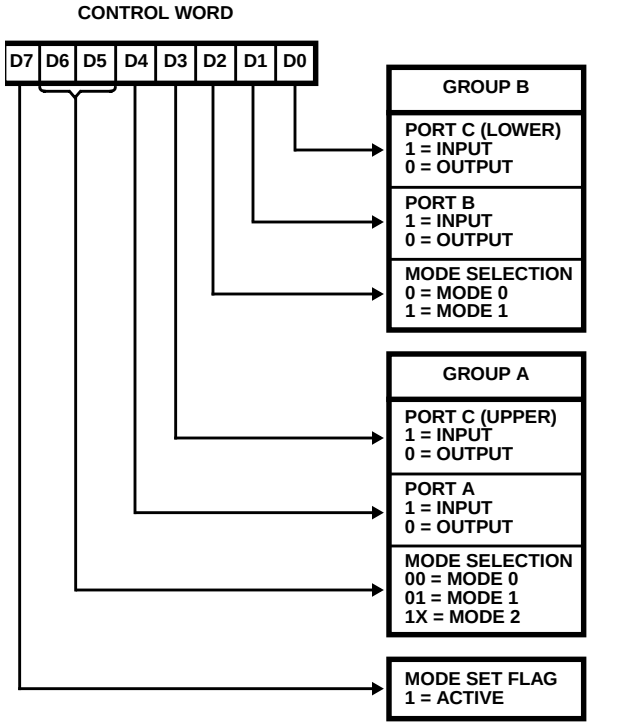


FIGURE 4. MODE DEFINITION FORMAT

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be “tailored” to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

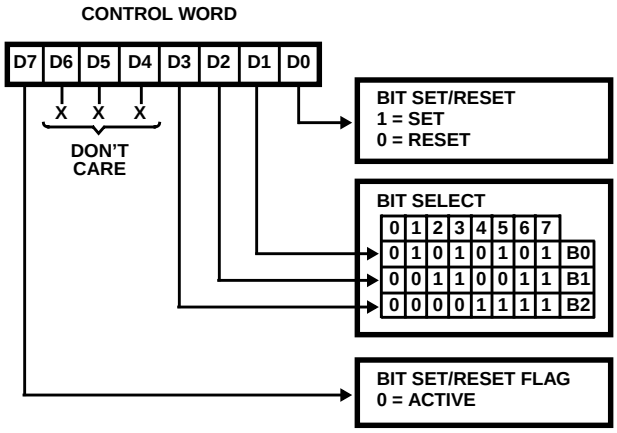


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

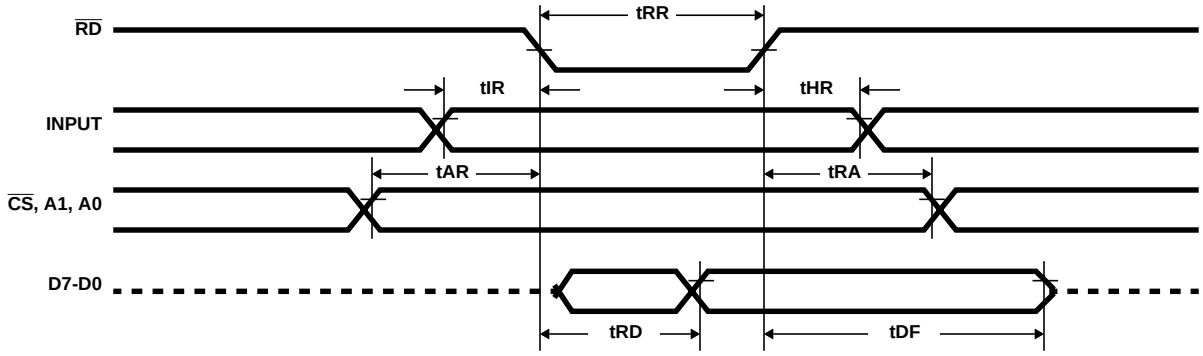
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

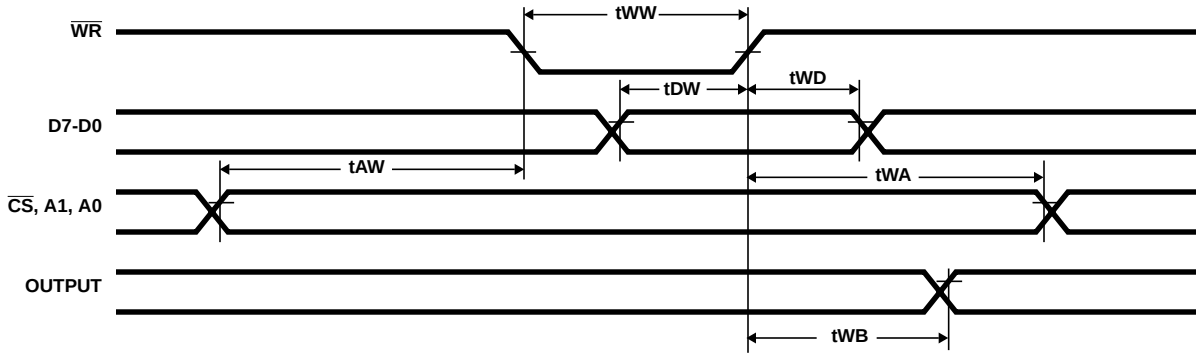
MODE 0 PORT DEFINITION

A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 (Basic Input)



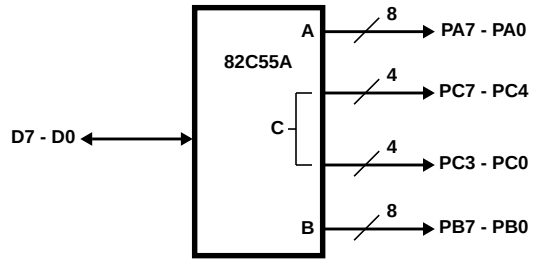
Mode 0 (Basic Output)



Mode 0 Configurations

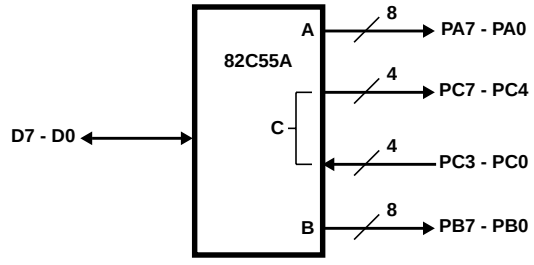
CONTROL WORD #0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0



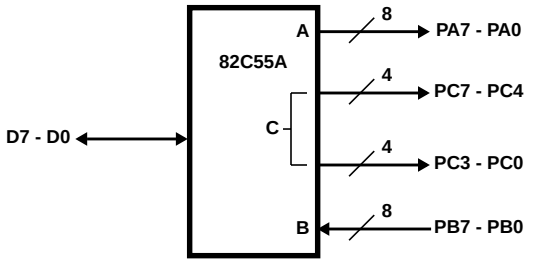
CONTROL WORD #1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1



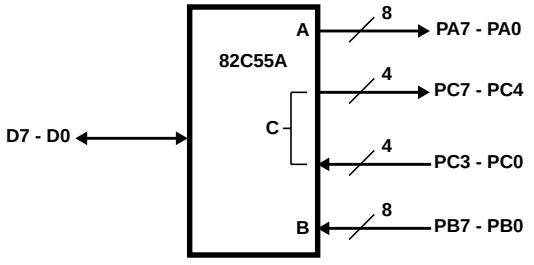
CONTROL WORD #2

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0



CONTROL WORD #3

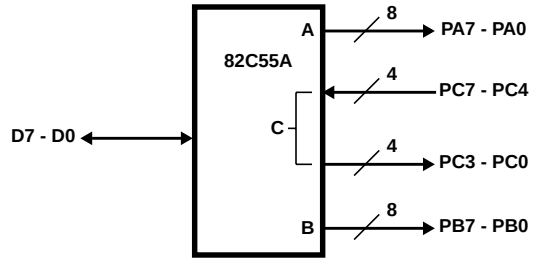
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1



Mode 0 Configurations (Continued)

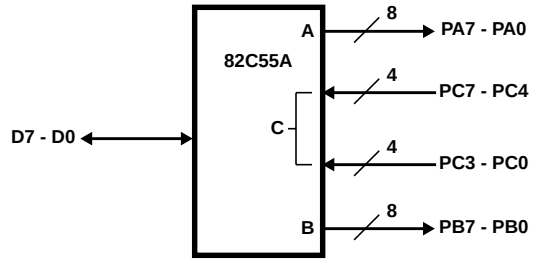
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



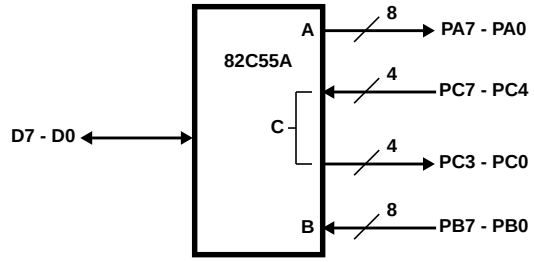
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	1



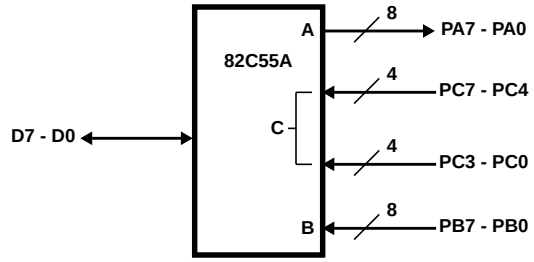
CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



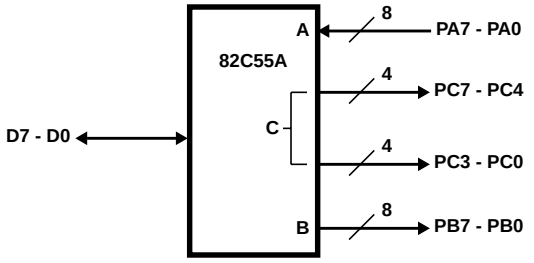
CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1



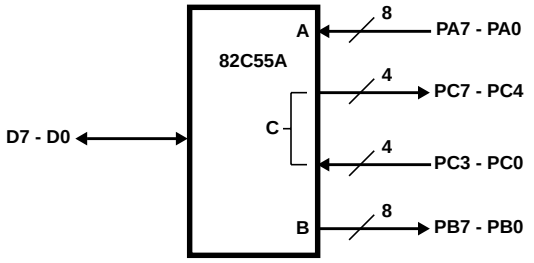
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0



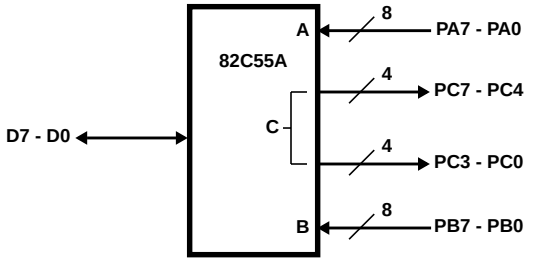
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1



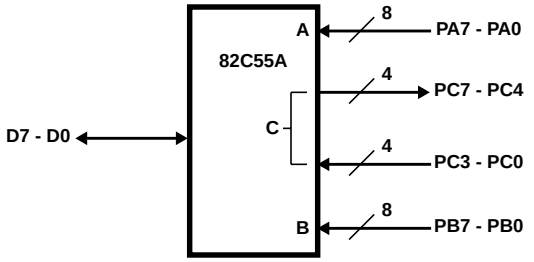
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0



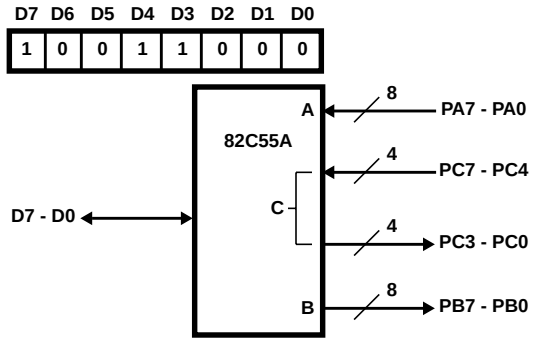
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

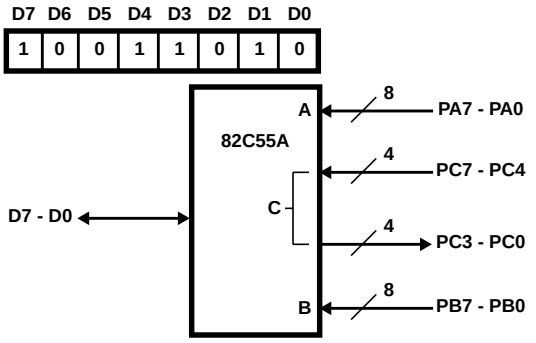


Mode 0 Configurations (Continued)

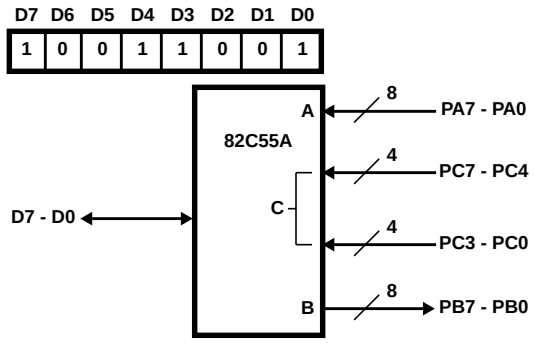
CONTROL WORD #12



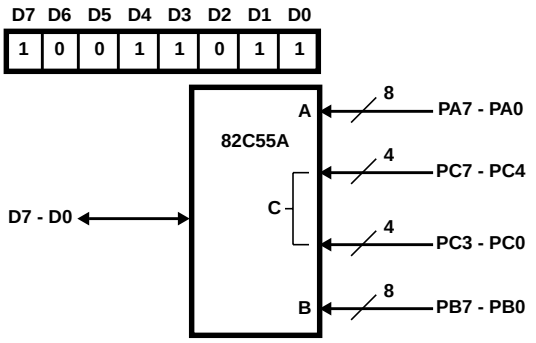
CONTROL WORD #14



CONTROL WORD #13



CONTROL WORD #15



Operating Modes

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “hand shaking” signals. In mode 1, port A and port B use the lines on port C to generate or accept these “hand shaking” signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A “low” on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A “high” on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

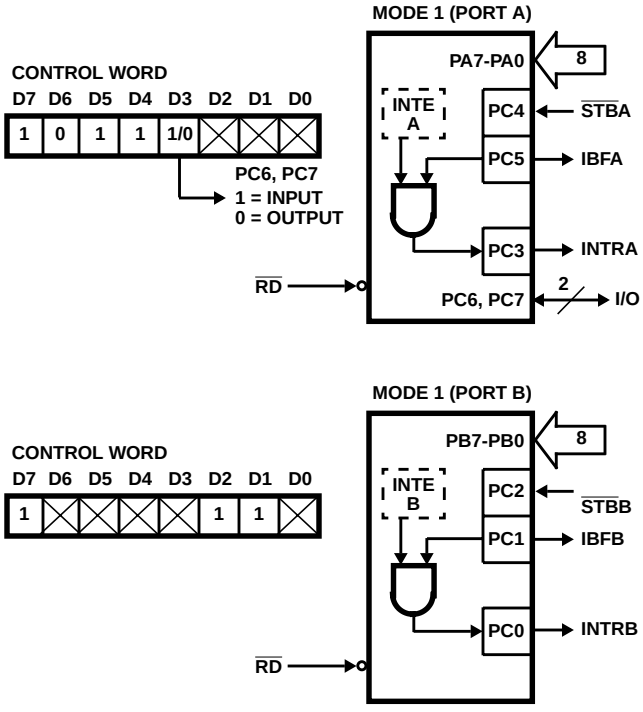


FIGURE 6. MODE 1 INPUT

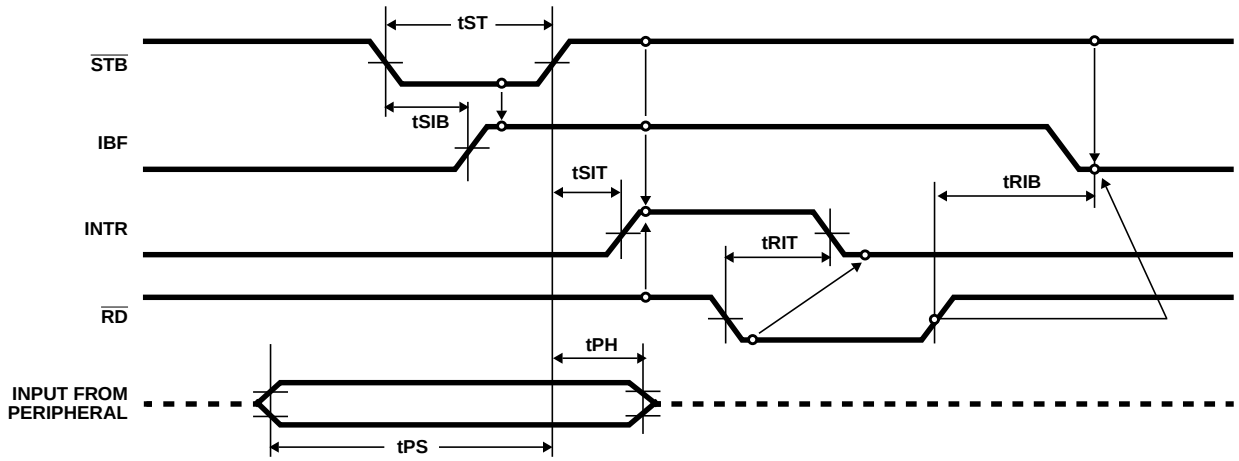


FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A “high” on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a “one”, IBF is a “one” and INTE is a “one”. It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

$\overline{OBF}$ - Output Buffer Full F/F). The $\overline{OBF}$ output will go “low” to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$, (See Note 1). The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ - Acknowledge Input). A “low” on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A “high” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a “one”, OBF is a “one” and INTE is a “one”. It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generates an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

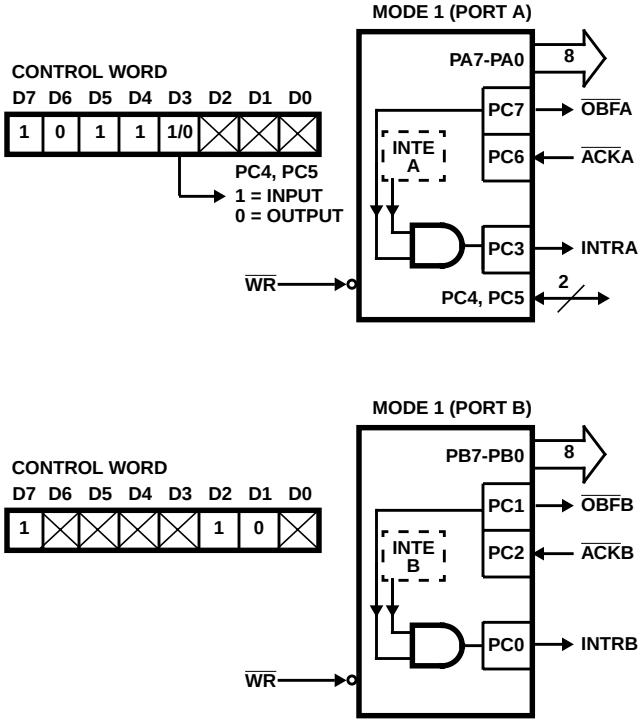


FIGURE 8. MODE 1 OUTPUT

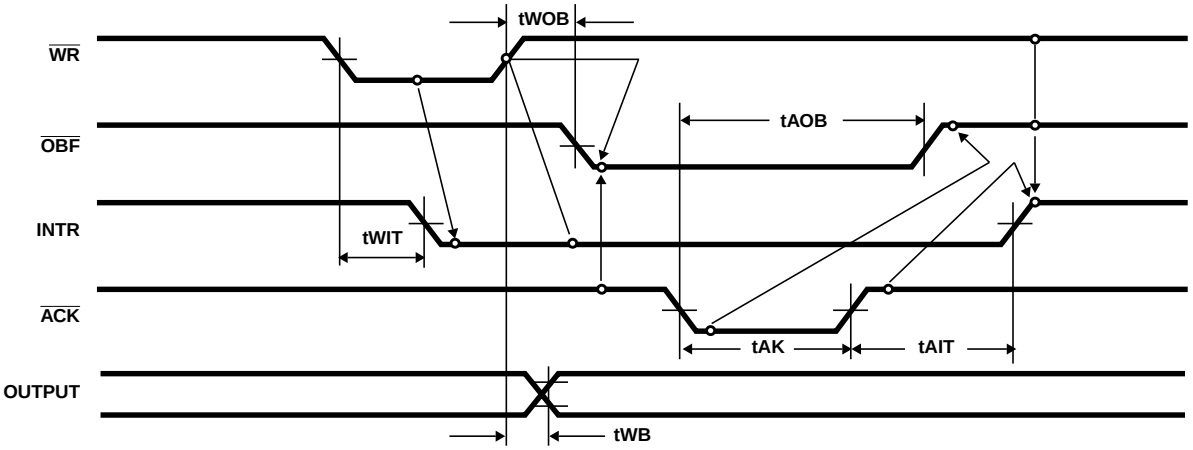
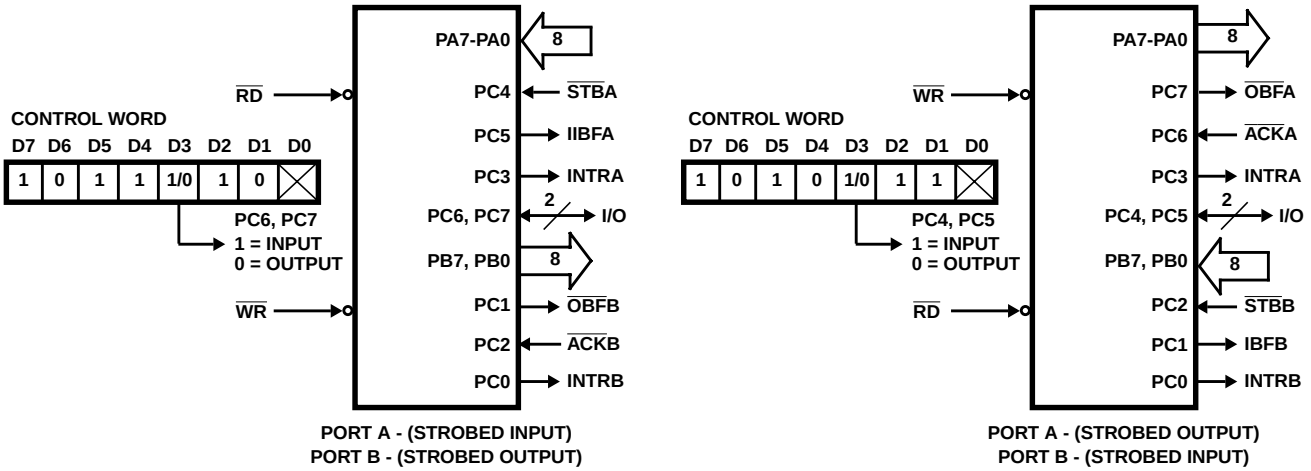


FIGURE 9. MODE 1 (STROBED OUTPUT)



Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). “Hand shaking” signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{\text{OBF}}$ - (Output Buffer Full). The $\overline{\text{OBF}}$ output will go “low” to indicate that the CPU has written data out to port A.

$\overline{\text{ACK}}$ - (Acknowledge). A “low” on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with $\overline{\text{OBF}}$). Controlled by bit set/reset of PC4.

Input Operations

$\overline{\text{STB}}$ - (Strobe Input). A “low” on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A “high” on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

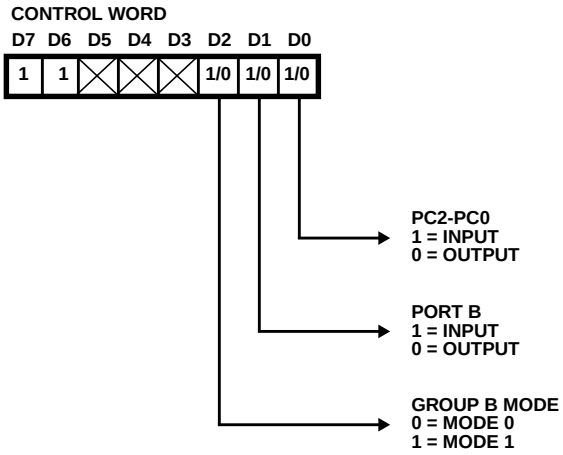


FIGURE 11. MODE CONTROL WORD

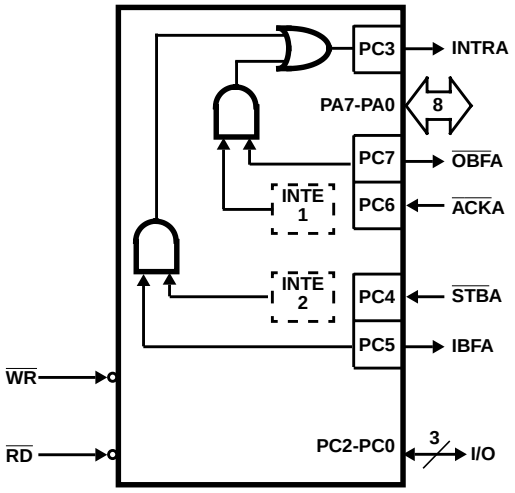
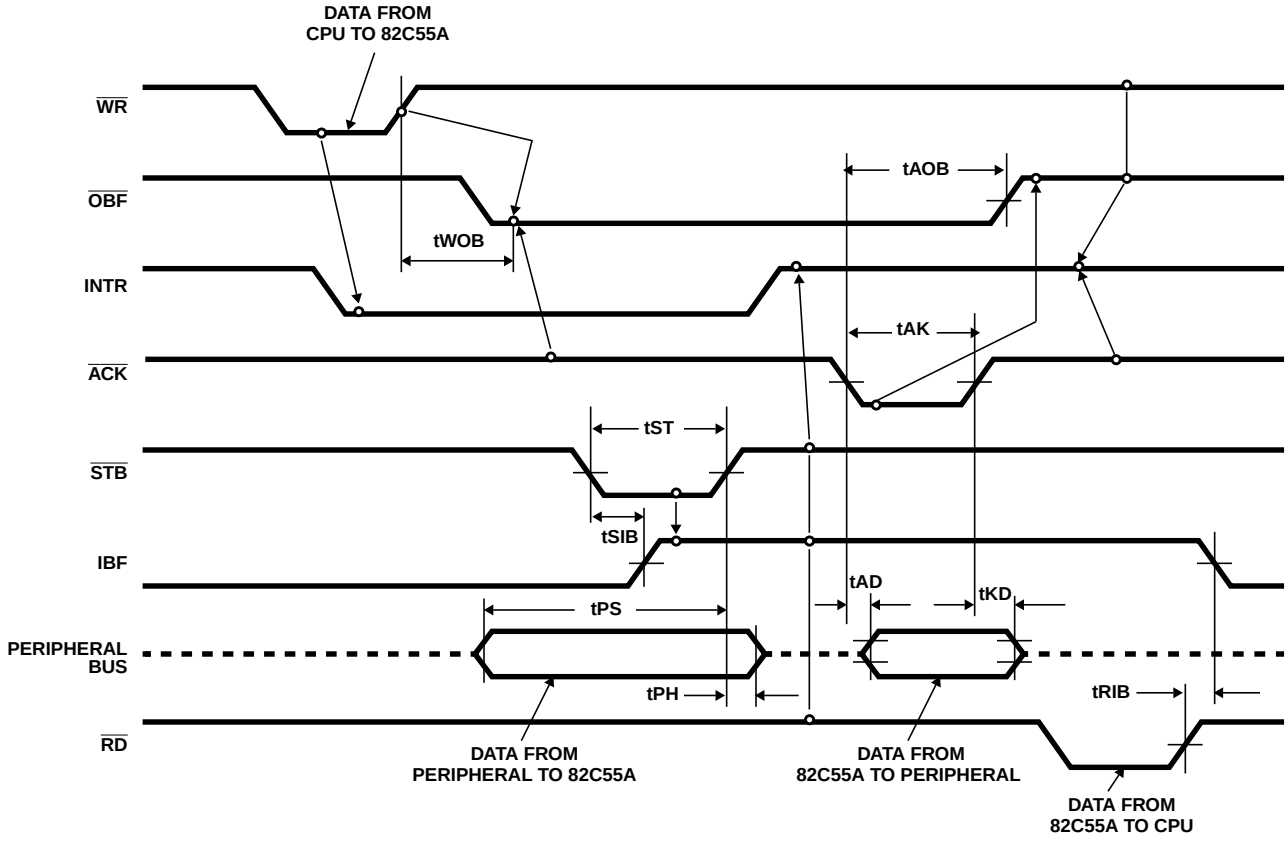


FIGURE 12. MODE 2



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ ÷ $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

FIGURE 13. MODE 2 (BI-DIRECTIONAL)

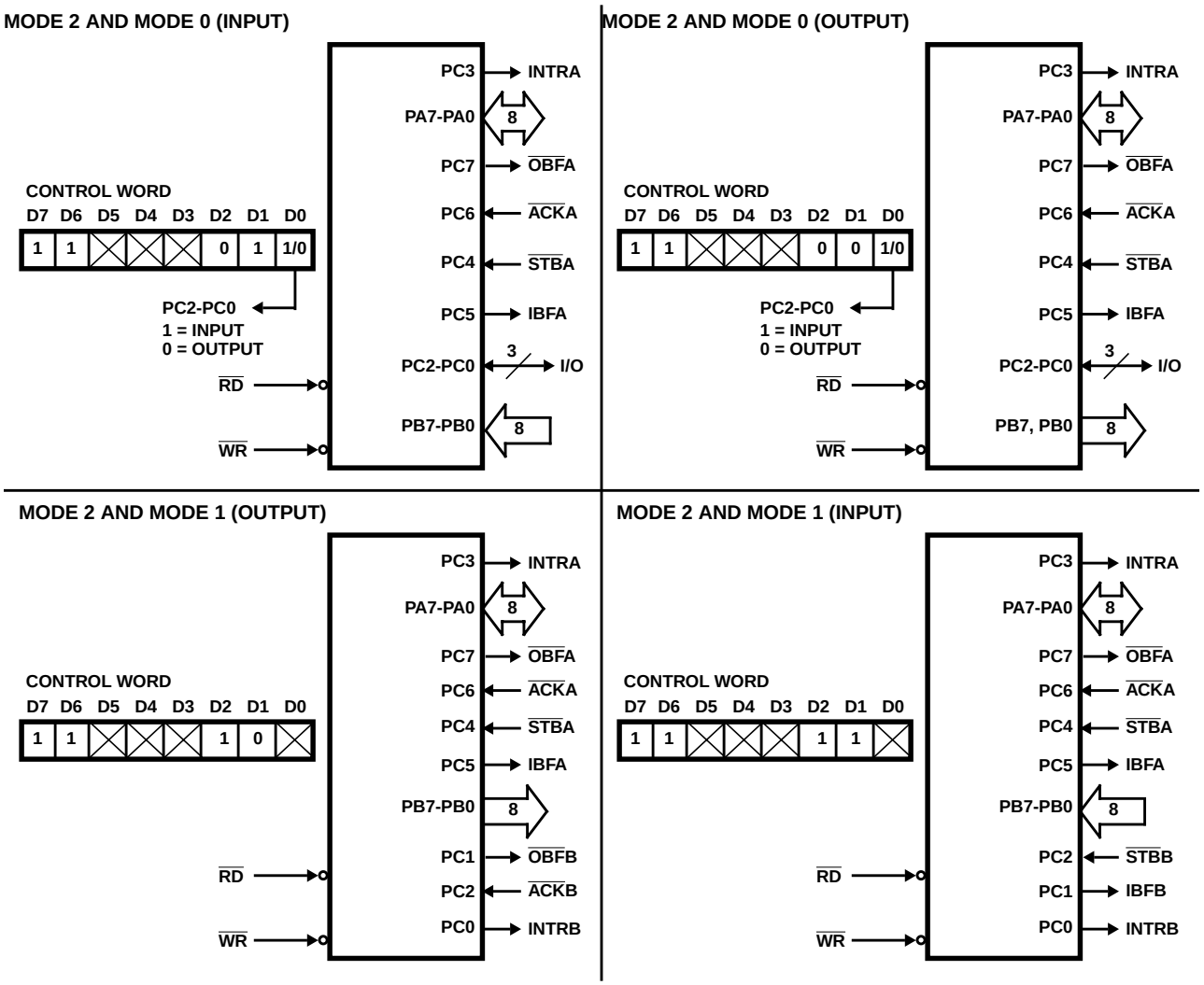


FIGURE 14. MODE 2 COMBINATIONS

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	↔	
PA1	In	Out	In	Out	↔	
PA2	In	Out	In	Out	↔	
PA3	In	Out	In	Out	↔	
PA4	In	Out	In	Out	↔	
PA5	In	Out	In	Out	↔	
PA6	In	Out	In	Out	↔	
PA7	In	Out	In	Out	↔	
PB0	In	Out	In	Out		Mode 0 or Mode 1 Only
PB1	In	Out	In	Out		
PB2	In	Out	In	Out		
PB3	In	Out	In	Out		
PB4	In	Out	In	Out		
PB5	In	Out	In	Out		
PB6	In	Out	In	Out		
PB7	In	Out	In	Out		
PC0	In	Out	INTRB	INTRB	I/O	
PC1	In	Out	IBFB	$\overline{OBF}$B	I/O	
PC2	In	Out	$\overline{STB}$B	$\overline{ACK}$B	I/O	
PC3	In	Out	INTRA	INTRA	INTRA	
PC4	In	Out	$\overline{STB}$A	I/O	$\overline{STB}$A	
PC5	In	Out	IBFA	I/O	IBFA	
PC6	In	Out	I/O	$\overline{ACK}$A	$\overline{ACK}$A	
PC7	In	Out	I/O	$\overline{OBF}$A	$\overline{OBF}$A	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a “Set Mode” command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a “Write Port C” command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a “Write Port C” command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in Mode 1 group or to change an interrupt enable flag, the “Set/Reset Port C Bit” command must be used.

With a “Set/Reset Port Cea Bit” command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a “Set/Reset Port C Bit” command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the “Set Reset Port C Bit” command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTEA	I/O	I/O	INTRA	INTEB	OBFB	INTRB
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

(Defined by Mode 0 or Mode 1 Selection)

FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts “hand shaking” signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the “status” of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or $\overline{STB}$B (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a “service routine” associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly “fit” the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

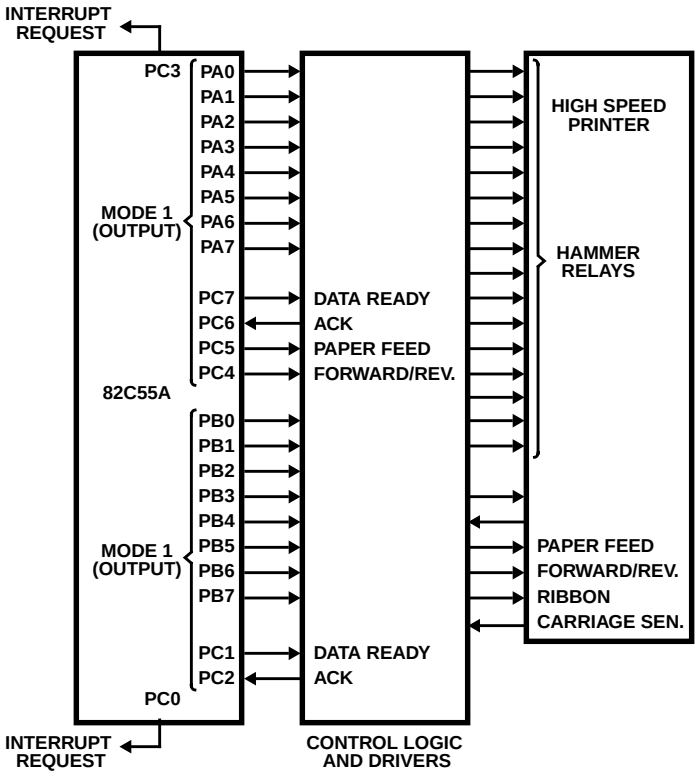


FIGURE 18. PRINTER INTERFACE