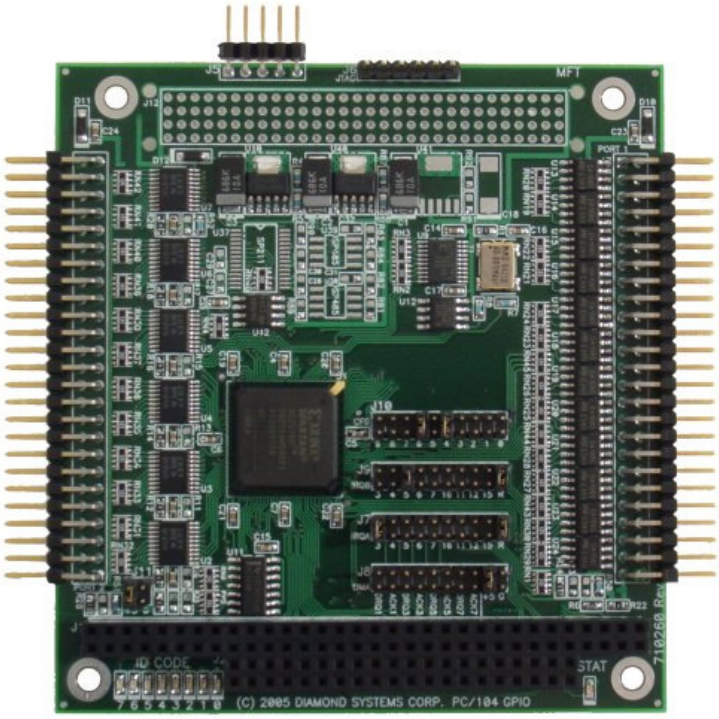
DIAMOND SYSTEMS CORPORATION

GPIO-MM

FPGA-based PC/104

FPGA Pinout Guide V1.01



Diamond Systems Corporation
1255 Terra Bella Ave.
Mountain View, CA 94043
Tel (650) 810-2500
Fax (650) 810-2525
www.diamondsystems.com

TABLE OF CONTENTS

1 GENERAL DESCRIPTION

The FPGA on the GPIO-MM is connected to the following devices:

1.1 PC/104 connectors J1 and J2

The FPGA connects directly to the PC/104 signals:

Address bus: SA<19:0>

Data bus: SD<15:0>

Control lines: AEN, IOR#, IOW#, SMEMRD#, SMEMWR#, MEMRD#, MEMWR#, TC, RESET

16-bit control: IOCS16#, MEMCS16#, SBHE#

IRQ and DMA signals are routed through configuration blocks J7-J9.

1.2 External I/O connectors J3, J4, J5 and J6

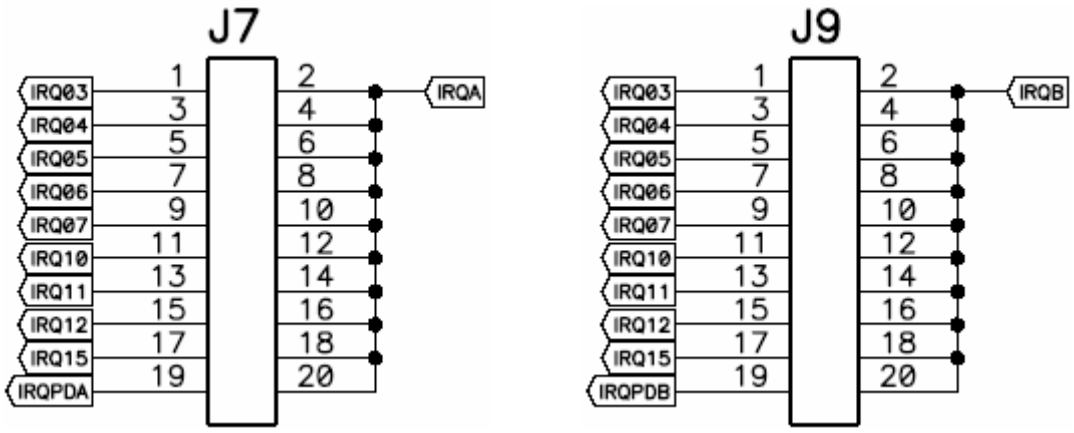
The FPGA I/O lines are connected directly to J3, J5 and J6. DA108S1 chips provide ESD and overvoltage protection for these lines.

The FPGA I/O lines are connected to J4 through 74XX245 buffers, described below.

J6 is the JTAG port used to program the FPGA and the configuration PROM.

1.3 Jumper configuration blocks J7, J8, J9 and J10

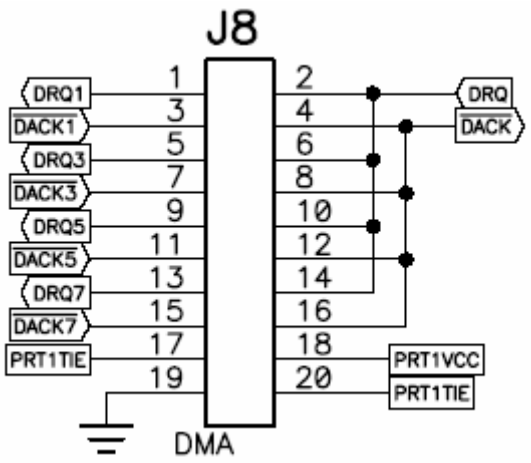
J7 and J9 route IRQs as shown below:



The IRQA and IRQB signals connect to the FPGA and can be routed through jumpers to the IRQx signals on the PC/104 bus.

The IRQPDA and IRQPDB positions allow the IRQ signals to be used in the IRQ-sharing configuration outlined by the PC/104 specification. By installing a jumper on these positions, the corresponding IRQ line is pulled down to ground through a 1Kohm resistor. In this configuration, the FPGA should either place the IRQ signal in input mode (to indicate an idle IRQ status) or drive the line to the high logic state (to indicate active IRQ status).

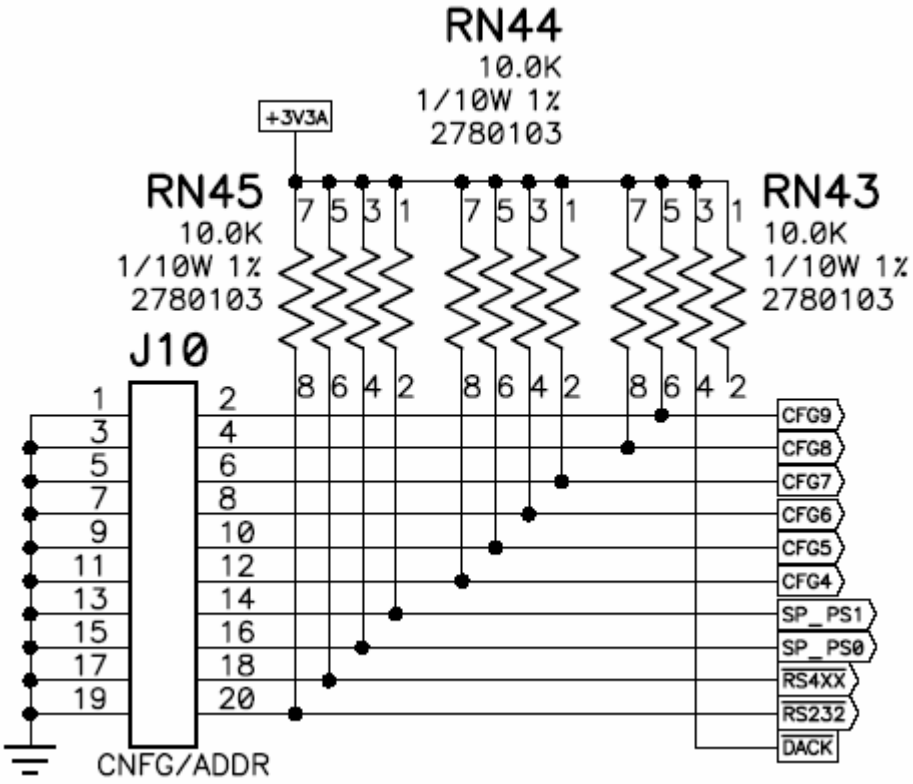
The DMA signals routed through J8 as shown below:



The signals DRQ and DACK# connect to the FPGA. Jumpers determine which PC/104 bus DMA channel is connected to the FPGA.

The PRT1TIE signal determines the bias level for the I/O on J3 and is not related to the FPGA pinout.

J10 provides user-defined configuration jumpers:



In the drawing above, SP_PS1 = CFG3, SP_PS0 = CFG2, RS4XX# = CFG1 and RS232# = CFG0.

Each of the CFG<9:0> signals are connected to an FPGA input pin. If the jumper is not present on J10, the signal will be pulled up to +3.3V. If the jumper is present, the signal is pulled low to 0V.

These inputs can be used for any kind of binary user configuration. One common use is for I/O address selection.

1.4 40MHz oscillator, Y1

The 40MHz oscillator is fed to a FPGA global clock pin.

1.5 Status LED, D1

The FPGA IO pin C15 is connected to the anode of the LED through a 475 ohm resistor. The cathode of the LED is connected to ground. The LED can be activated by driving the FPGA output high and deactivated by driving the output low.

1.6 XCF02S configuration PROM, U9

The XCF02S holds the FPGA logic and programs the FPGA during each power-on cycle.

1.7 256-byte 24C04 EEPROM, U12

The 24C04 EEPROM connects to the FPGA through a 2-wire I^2C bus.

1.8 74XX164 shift register, U11

The eight outputs lines of the 74XX164 each drive one LED on the lower left side of the board. This is used in the standard logic to display the current "personality ID", but can be used for any purpose in a custom FPGA design. It is connected to the FPGA through 2 wires.

1.9 74XX245 buffers, U2-U7

These buffers sit between J4 and the FPGA and provide higher I/O current capability to J4 than the FPGA could provide alone.

The buffers are situated such that side "A" is connected to the FPGA and side "B" is connected to J4. The direction control signal is also controlled by the FPGA. When the direction signal is high, the buffers drive port B with the data on port A (i.e. use this to output data from the FPGA to J4). When the direction signal is low, the buffers drive port A with the data on port B (i.e. use this to input data from J4 to the FPGA).

2 PIN DEFINITIONS

Signal	FPGA Pin	FPGA Pin Dir.	End Point	Function
J3 EXTERNAL SIGNAL GROUP				
DIO_J3_1	J3	I/O	J3 pin 1	Digital I/O
DIO_J3_2	H3	I/O	J3 pin 2	Digital I/O
DIO_J3_3	H4	I/O	J3 pin 3	Digital I/O
DIO_J3_4	H1	I/O	J3 pin 4	Digital I/O
DIO_J3_5	H2	I/O	J3 pin 5	Digital I/O
DIO_J3_6	G1	I/O	J3 pin 6	Digital I/O
DIO_J3_7	G2	I/O	J3 pin 7	Digital I/O
DIO_J3_8	G3	I/O	J3 pin 8	Digital I/O
DIO_J3_9	G4	I/O	J3 pin 9	Digital I/O
DIO_J3_10	G5	I/O	J3 pin 10	Digital I/O
DIO_J3_11	F5	I/O	J3 pin 11	Digital I/O
DIO_J3_12	F3	I/O	J3 pin 12	Digital I/O
DIO_J3_13	F4	I/O	J3 pin 13	Digital I/O
DIO_J3_14	F1	I/O	J3 pin 14	Digital I/O
DIO_J3_15	F2	I/O	J3 pin 15	Digital I/O
DIO_J3_16	E1	I/O	J3 pin 16	Digital I/O
DIO_J3_17	E2	I/O	J3 pin 17	Digital I/O
DIO_J3_18	E3	I/O	J3 pin 18	Digital I/O
DIO_J3_19	E4	I/O	J3 pin 19	Digital I/O
DIO_J3_20	D1	I/O	J3 pin 20	Digital I/O
DIO_J3_21	D2	I/O	J3 pin 21	Digital I/O
DIO_J3_22	C1	I/O	J3 pin 22	Digital I/O
DIO_J3_23	C2	I/O	J3 pin 23	Digital I/O
DIO_J3_24	B1	I/O	J3 pin 24	Digital I/O
DIO_J3_25	A2	I/O	J3 pin 25	Digital I/O
DIO_J3_26	B3	I/O	J3 pin 26	Digital I/O
DIO_J3_27	A3	I/O	J3 pin 27	Digital I/O
DIO_J3_28	B4	I/O	J3 pin 28	Digital I/O
DIO_J3_29	A4	I/O	J3 pin 29	Digital I/O
DIO_J3_30	D5	I/O	J3 pin 30	Digital I/O
DIO_J3_31	C5	I/O	J3 pin 31	Digital I/O
DIO_J3_32	B5	I/O	J3 pin 32	Digital I/O
DIO_J3_33	A5	I/O	J3 pin 33	Digital I/O
DIO_J3_34	B6	I/O	J3 pin 34	Digital I/O
DIO_J3_35	A6	I/O	J3 pin 35	Digital I/O
DIO_J3_36	D6	I/O	J3 pin 36	Digital I/O
DIO_J3_37	C6	I/O	J3 pin 37	Digital I/O
DIO_J3_38	E6	I/O	J3 pin 38	Digital I/O
DIO_J3_39	E7	I/O	J3 pin 39	Digital I/O
DIO_J3_40	D7	I/O	J3 pin 40	Digital I/O
DIO_J3_41	C7	I/O	J3 pin 41	Digital I/O
DIO_J3_42	B7	I/O	J3 pin 42	Digital I/O
DIO_J3_43	A7	I/O	J3 pin 43	Digital I/O
DIO_J3_44	A8	I/O	J3 pin 44	Digital I/O

DIO_J3_45	D8	I/O	J3 pin 45	Digital I/O
DIO_J3_46	C8	I/O	J3 pin 46	Digital I/O
DIO_J3_47	D9	I/O	J3 pin 47	Digital I/O
DIO_J3_48	D10	I/O	J3 pin 48	Digital I/O
J4 EXTERNAL SIGNAL GROUP				
DIO_J4_1	T14	I/O	J4 pin 1 (U2)	Digital I/O
DIO_J4_2	R11	I/O	J4 pin 2 (U3)	Digital I/O
DIO_J4_3	R13	I/O	J4 pin 3 (U2)	Digital I/O
DIO_J4_4	T11	I/O	J4 pin 4 (U3)	Digital I/O
DIO_J4_5	T13	I/O	J4 pin 5 (U2)	Digital I/O
DIO_J4_6	N11	I/O	J4 pin 6 (U3)	Digital I/O
DIO_J4_7	P13	I/O	J4 pin 7 (U2)	Digital I/O
DIO_J4_8	P11	I/O	J4 pin 8 (U3)	Digital I/O
DIO_J4_9	N12	I/O	J4 pin 9 (U2)	Digital I/O
DIO_J4_10	M11	I/O	J4 pin 10 (U3)	Digital I/O
DIO_J4_11	P12	I/O	J4 pin 11 (U2)	Digital I/O
DIO_J4_12	M10	I/O	J4 pin 12 (U3)	Digital I/O
DIO_J4_13	R12	I/O	J4 pin 13 (U2)	Digital I/O
DIO_J4_14	N10	I/O	J4 pin 14 (U3)	Digital I/O
DIO_J4_15	T12	I/O	J4 pin 15 (U2)	Digital I/O
DIO_J4_16	P10	I/O	J4 pin 16 (U3)	Digital I/O
DIO_J4_17	T9	I/O	J4 pin 17 (U4)	Digital I/O
DIO_J4_18	R7	I/O	J4 pin 18 (U5)	Digital I/O
DIO_J4_19	R9	I/O	J4 pin 19 (U4)	Digital I/O
DIO_J4_20	T7	I/O	J4 pin 20 (U5)	Digital I/O
DIO_J4_21	T10	I/O	J4 pin 21 (U4)	Digital I/O
DIO_J4_22	P7	I/O	J4 pin 22 (U5)	Digital I/O
DIO_J4_23	R10	I/O	J4 pin 23 (U4)	Digital I/O
DIO_J4_24	N7	I/O	J4 pin 24 (U5)	Digital I/O
DIO_J4_25	N9	I/O	J4 pin 25 (U4)	Digital I/O
DIO_J4_26	M7	I/O	J4 pin 26 (U5)	Digital I/O
DIO_J4_27	P9	I/O	J4 pin 27 (U4)	Digital I/O
DIO_J4_28	M6	I/O	J4 pin 28 (U5)	Digital I/O
DIO_J4_29	P8	I/O	J4 pin 29 (U4)	Digital I/O
DIO_J4_30	P6	I/O	J4 pin 30 (U5)	Digital I/O
DIO_J4_31	T8	I/O	J4 pin 31 (U4)	Digital I/O
DIO_J4_32	N6	I/O	J4 pin 32 (U5)	Digital I/O
DIO_J4_33	T6	I/O	J4 pin 33 (U6)	Digital I/O
DIO_J4_34	T2	I/O	J4 pin 34 (U7)	Digital I/O
DIO_J4_35	R6	I/O	J4 pin 35 (U6)	Digital I/O
DIO_J4_36	R1	I/O	J4 pin 36 (U7)	Digital I/O
DIO_J4_37	T5	I/O	J4 pin 37 (U6)	Digital I/O
DIO_J4_38	P1	I/O	J4 pin 38 (U7)	Digital I/O
DIO_J4_39	R5	I/O	J4 pin 39 (U6)	Digital I/O
DIO_J4_40	N2	I/O	J4 pin 40 (U7)	Digital I/O
DIO_J4_41	P5	I/O	J4 pin 41 (U6)	Digital I/O
DIO_J4_42	N1	I/O	J4 pin 42 (U7)	Digital I/O

DIO_J4_43	N5	I/O	J4 pin 43 (U6)	Digital I/O
DIO_J4_44	M4	I/O	J4 pin 44 (U7)	Digital I/O
DIO_J4_45	T4	I/O	J4 pin 45 (U6)	Digital I/O
DIO_J4_46	M3	I/O	J4 pin 46 (U7)	Digital I/O
DIO_J4_47	T3	I/O	J4 pin 47 (U6)	Digital I/O
DIO_J4_48	M2	I/O	J4 pin 48 (U7)	Digital I/O
U2 DIR Control	K3	Out	U2	Buffer DIR Control
U3 DIR Control	K2	Out	U3	Buffer DIR Control
U4 DIR Control	K1	Out	U4	Buffer DIR Control
U5 DIR Control	J2	Out	U5	Buffer DIR Control
U6 DIR Control	J1	Out	U6	Buffer DIR Control
U7 DIR Control	J4	Out	U7	Buffer DIR Control
J5 EXTERNAL SIGNAL GROUP				
AUXDIO0	K5	I/O	J5 pin 1	Auxiliary DIO
AUXDIO1	L5	I/O	J5 pin 2	Auxiliary DIO
AUXDIO2	K4	I/O	J5 pin 3	Auxiliary DIO
AUXDIO3	L4	I/O	J5 pin 4	Auxiliary DIO
CLOCKS				
FPCLK	N8	In	Y1	40MHz Oscillator Input
SYSCLK	R8	In	PC/104 B20	PC/104 Bus Clock
PC/104 BUS AND CONFIGURATION GROUP				
IOW#	C13	In	PC/104 B13	I/O Write Strobe
IOR#	B13	In	PC/104 B14	I/O Read Strobe
IOCS16#	A14	I/O	PC/104 D2	16-bit I/O Access
AEN	H16	In	PC/104 A11	Address Enable
SMEMWR#	D12	In	PC/104 B11	Memory Write (<1MB)
SMEMRD#	C12	In	PC/104 B12	Memory Read (<1MB)
MEMWR#	B12	In	PC/104 C10	Memory Write
MEMRD#	A12	In	PC/104 C9	Memory Read
MEMCS16#	A13	I/O	PC/104 D1	16-bit Memory Access
SBHE#	J13	I/O	PC/104 C1	System Byte High Enable
TC	A9	I/O	PC/104 B27	Terminal Count
DRQ	T15	Out	J8	DMA Request
DACK#	L12	In	J8	DMA Acknowledge
SA19	H15	In	PC/104 A12	Address Bus
SA18	H14	In	PC/104 A13	Address Bus
SA17	H13	In	PC/104 A14	Address Bus
SA16	G12	In	PC/104 A15	Address Bus
SA15	G14	In	PC/104 A16	Address Bus
SA14	G13	In	PC/104 A17	Address Bus
SA13	G16	In	PC/104 A18	Address Bus
SA12	G15	In	PC/104 A19	Address Bus
SA11	F16	In	PC/104 A20	Address Bus
SA10	F15	In	PC/104 A21	Address Bus
SA9	F14	In	PC/104 A22	Address Bus
SA8	F13	In	PC/104 A23	Address Bus
SA7	F12	In	PC/104 A24	Address Bus
SA6	E14	In	PC/104 A25	Address Bus

SA5	E13	In	PC/104 A26	Address Bus
SA4	E16	In	PC/104 A27	Address Bus
SA3	E15	In	PC/104 A28	Address Bus
SA2	D16	In	PC/104 A29	Address Bus
SA1	C16	In	PC/104 A30	Address Bus
SA0	B16	In	PC/104 A31	Address Bus
SD15	M16	I/O	PC/104 C18	Data Bus
SD14	M15	I/O	PC/104 C17	Data Bus
SD13	M14	I/O	PC/104 C16	Data Bus
SD12	M13	I/O	PC/104 C15	Data Bus
SD11	N14	I/O	PC/104 C14	Data Bus
SD10	N16	I/O	PC/104 C13	Data Bus
SD9	P16	I/O	PC/104 C12	Data Bus
SD8	R16	I/O	PC/104 C11	Data Bus
SD7	K15	I/O	PC/104 A2	Data Bus
SD6	K16	I/O	PC/104 A3	Data Bus
SD5	K13	I/O	PC/104 A4	Data Bus
SD4	K14	I/O	PC/104 A5	Data Bus
SD3	K12	I/O	PC/104 A6	Data Bus
SD2	J14	I/O	PC/104 A7	Data Bus
SD1	J15	I/O	PC/104 A8	Data Bus
SD0	J16	I/O	PC/104 A9	Data Bus
IRQB	L15	Out	J9	IRQB Output
IRQA	L16	Out	J7	IRQA Output
CFG9	D11	In	J10	Configuration Input
CFG8	C11	In	J10	Configuration Input
CFG7	E11	In	J10	Configuration Input
CFG6	B11	In	J10	Configuration Input
CFG5	A11	In	J10	Configuration Input
CFG4	C10	In	J10	Configuration Input
CFG3	B10	In	J10	Configuration Input
CFG2	A10	In	J10	Configuration Input
CFG1	B8	In	J10	Configuration Input
CFG0	C9	In	J10	Configuration Input
RESET	B9	In	PC/104 B2	PC/104 Reset Line
EEPROM GROUP				
EEP_SDL	L1	I/O	U12 pin 5	EEPROM Data Line
EEP_SCL	M1	Out	U12 pin 6	EEPROM Clock Line
74HC164 GROUP				
IDCLK	L14	Out	U11 pin 8	74HC164 Data
IDDAT	L13	Out	U11 pin 1 and 2	74HC164 Clock

.